RCA

Solid State

MOS Memories • COS/MOS Memories • COS/MOS Mem

MAC Microprocessors • COSMAC Microprocessors • COSMAC M

oboard Computer Systems • Microboard Computer Systems •

ort Systems • Support Systems • Support Systems • Support

COS/MOS Memories, Microprocessors, and Support Systems

RCA COS/MOS Memories, Microprocessors, and Support Systems

This DATABOOK contains complete technical information on the full line of COS/MOS memory and microprocessor integrated circuits, COSMAC microboard computer systems, and COSMAC microprocessor support systems available from RCA Solid State Division. An Index to Devices provides a complete listing of types.

The Index to Devices is followed by several pages of general product information that includes photographs showing the package options available for RCA COS/MOS memory and microprocessor integrated circuits, a Product Overview that summarizes the basic features and complement of each category of products, and a Product Classification Chart that groups integrated circuits and systems according to product type and intended function. Next, a Cross-Reference Guide lists popular memory integrated circuits supplied by other manufacturers together with a recommended RCA replacement type. The DATABOOK then includes a general discussion of Operating and Handling Considerations for COS/MOS Integrated Circuits.

Four separate data sections provide definitive ratings, electrical characteristics, and user information for (1) the CDP1800 series of COSMAC microprocessors and associated memory and peripheral circuits, (2) the MWS5000 and CD4000 series of general-purpose memories, (3) the CDP18S600 series of COSMAC microboard computer systems, and (4) the CDP18S series of COSMAC microprocessor support and development systems. Within each data section, the data pages for individual integrated circuits or systems are grouped in alphanumerical sequence of type numbers.

The DATABOOK also contains selected application notes on RCA memories, microprocessors, and development systems and dimensional outlines of all packages in which RCA memory and microprocessor integrated circuits are supplied.

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The device data shown for some types are indicated as preliminary, advance, or objective. **Preliminary data** are intended for guidance purposes in evaluating devices for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. **Advance** or **Objective data** are intended for engineering evaluation of types in the initial stages of design. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change of future manufacture of these devices. For current information on the status of preliminary or objective programs, please contact your local RCA sales office.

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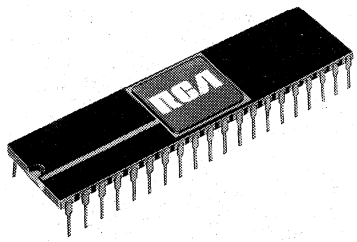
Packages and Ordering Information

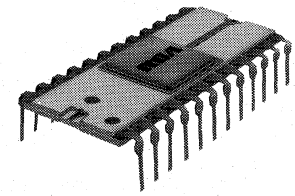
Packages

D Suffix
Dual-In-Line Size-Brazed Ceramic Packages



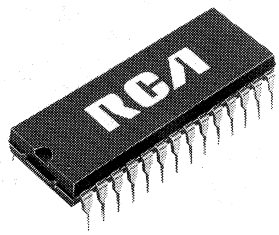
16-, 18-, 22-, 24-, 28-, and 40-lead versions

D Suffix
Dual-In-Line Welded-Seal Ceramic Packages



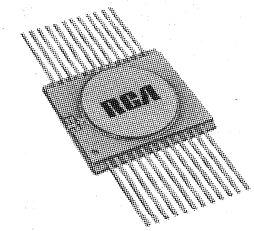
16- and 24-lead versions

E Suffix
Plastic Dual-In-Line Packages



16-, 18-, 22-, 24-, 28-, and 40-lead versions

K Suffix
24-Lead Ceramic Flat Pack



CD4036A and CD4039A only

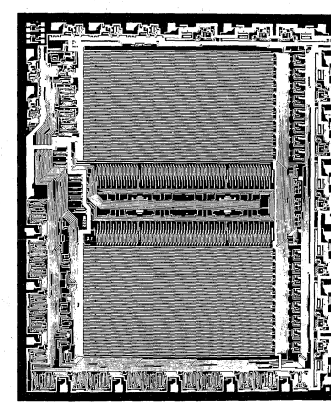
Ordering Information

RCA COS/MOS microprocessor and memory integrated circuits are available in one or more of the following package styles and are identified by the Suffix Letters indicated: dual-in-line size-brazed ceramic, dual-in-line welded-seal ceramic, dual-in-line plastic, and in chip form. The available package styles for any specific type are given in the technical data for that type.

When ordering COS/MOS devices, it is important that the appropriate suffix letter be affixed to the type number of the device required. For example, a CDP1802 in a dual-in-line ceramic package will be identified as the CDP1802D.

PACKAGE	SUFFIX LETTERS
Dual-In-Line Welded-Seal or Side-Brazed Ceramic	D
Dual-In-Line Plastic	E
Ceramic Flat Pack (CD4036A and CD4039A only)	K
Chip	H

H Suffix
Chip



Product Overview

RCA offers an all-COS/MOS line of memory, microprocessor and peripheral integrated circuits for use in a broad range of diverse industrial, consumer, and military applications. These devices offer the user all the advantages unique to COS/MOS technology, including:

- **Low power drain**—makes COS/MOS integrated circuits a natural choice for battery-operated systems, battery backed-up systems, and systems in which heat dissipation is a prime consideration.
- **High noise immunity and wide operating temperature range (−55 °C to +125 °C)**—allows COS/MOS integrated circuits to be used in the most demanding industrial environments.
- **Wide operating voltage range**—reduces the need for expensive regulated power supplies and thereby allows the design engineer greater freedom to concentrate on other aspects of system design.

In addition, the cost competitiveness of RCA COS/MOS integrated circuits is maintained through continued innovative advances in design technology. For example, the inherently larger number of transistors in COS/MOS integrated circuits (in comparision to equivalent NMOS types) is compensated for through the use of increased packing densities made possible by C^2L and SOS technologies. C^2L (closed-cell logic) is a high-density technology that eliminates the need for guard bands through the use of closed-cell transistors. SOS technology, in which silicon-transistor islands are forms on a sea of insulating sapphire, can improve packing densities ten-fold in comparison to standard metal-gate logic with a simultaneous increase in operating speed.

CDP1800 Series

The RCA CDP1800 series offers the most complete line of COS/MOS microprocessor and associated memory and peripheral devices in the industry. The heart of the series is the CDP1802 central processing unit (CPU). This unit, which features COSMAC register-based architecture, offers 16 internal registers to facilitate data manipulation and to reduce the need for additional devices. The need for external devices is even further reduced by use of an on-chip clock, DMA, and single-phase operation.

RCA's large and expanding CDP1800-series product line offers the system designer exceptional flexibility in hardware/software tradeoffs. In addition to the CDP1802, this product line includes a hardware multiply/divide unit (MDU), a programmable I/O, video and keyboard interface circuits, latches and decoders, a universal asynchronous receiver-transmitter (UART), buffers, separators, and a broad complement of directly interfaceable random-access memories (RAM's) and read-only memories (ROM's).

RCA also has under development a new microcomputer, the CDP1804. This microcomputer incorporates all the features of the CDP1802 augmented by additional hardware and increased performance capabilties. The additional hardware includes 2K bytes of ROM, 64 bytes of RAM, and a counter/timer. With respect to the CDP1802, the CDP1804 features increased operating speed (up to 8 MHz over the operating temperature range) and an expanded instruction set to improve programming flexibility and compactness. This computer on a chip employs the latest SOS technology to pack more than 30,000 transistors on a single chip while simultaneously maintaining the low power drain inherent with COS/MOS technology.

General-Purpose Memories

In addition to the memories designed to interface directly with CDP1800-series microprocessors, RCA also offers a line of general-purpose memories. These memories include types from the RCA CD4000 series of COS/MOS integrated circuits and types from the MWS5000 series of high-speed SOS products.

COSMAC Microprocessor Support and Development Systems

For the designers of microprocessor-based equipment and in support of the CDP1800-series microprocessors and associated memory and peripheral circuits, RCA provides a strong and extensive line of systems, system support components, system support software, system modules (including the new COSMAC microboard milliwatt computer systems), and other development aids. The support-system line includes development systems ranging from a minimum tape-based system to a full development system having floppy-disk mass memory storage and operating system software. This line also includes two evaluation systems that serve as convenient learning tools for design, hardware interfacing, and programming of microcomputer systems. These systems can also be used as the basis for breadboarding and prototyping user-designed microcomputer systems.

COSMAC Microboard Computer Systems

The new RCA COSMAC microboard milliwatt computer systems form an extensive line of fully coordinated products based on a standard, simple-to-use 4.5-by-7.5 inch module. These modules feature the inherent CMOS advantages of low power consumption, wide operating voltage range, and excellent noise immunity. The microboard systems are all designed with the

microboard universal backplane and are compatible with RCA COSMAC Development Systems. User-developed systems, therefore, can be readily developed and easily modified.

As a convenient starting point for the user, two microboard prototyping systems are available. These systems, include an expandable 5-card chassis, a microboard computer-system module, a microboard control-and-display module, ROM-based utility software, and ample room for user-designed expansion. These prototyping systems enable the user to reduce his hardware concerns to a minimum and to maximize his efforts in custom design and software development to meet the specific requirements of his application.

Product Classification Chart

CDP1800-Series IC Products

General-Purpose Memories

COSMAC Microboard Computer Systems

Product Classification Chart

Cross-Reference Guide

Note: RCA functionally equivalent type may not be identical with other manufacturer's type in every detail. Refer to published data for further information.

Type	Description	RCA Functionally Equivalent Type
AMI		
S4025	1024 x 1 RAM	CDP1821
S6508	1024 x 1 RAM	CDP1821*
S5101	256 x 4 RAM	CDP1822*
		MWS5101*
S6810-1	128 x 8 RAM	CDP1823
S3514	512 x 8 ROM	CDP1831
		CDP1832
S6830	1024 x 8 ROM	CDP1833
		CDP1834
S1883	UART	CDP1854
Fairchild		
MK3514	512 x 8 ROM	CDP1831
		CDP1832
MK386k	I/O	CDP1852
MK35342	1024 x 1 RAM	CDP1821
MK35345	1024 x 1 RAM	CDP1821
MK93415	1024 x 1 RAM	CDP1821
MK93425	1024 x 1 RAM	CDP1821
General Instruments		
RA-3-4256	256 x 4 RAM	CDP1822
RO-3-4096	512 x 8 ROM	CDP1831
		CDP1832
AY-3-1013		
AY-3-1014	UART	CDP1854*
AY-3-1015		
Harris		
HM6551	256 x 4 RAM	CDP1822*
HM6501		MWS5101*
HM6514	1024 x 4 RAM	MWS5114
Hughes		
HMPS1802	CPU	CDP1802*
HMPS1824	32 x 8 RAM	CDP1824
HMPS1822	256 x 4 RAM	CDP1822*
HMPS1852	I/O Port	CDP1852*
Intel		
2102	1024 x 1 RAM	CDP1821*
2101	256 x 4 RAM	CDP1822*
		MWS5101*
2111	256 x 4 RAM	CDP1822
2112	256 x 4 RAM	CDP1822
4101	256 x 4 RAM	CDP1822
5101	256 x 4 RAM	CDP1822*
		MWS5101*
2114	1024 x 4 RAM	MWS5114
8101	256 x 4 RAM	CDP1822
2308	1024 x 8 ROM	CDP1833
		CDP1834
8308	1024 x 8 ROM	CDP1833
		CDP1834
2704	512 x 8 PROM	CDP1831
		CDP1832*
2708	1024 x 8 PROM	CDP1833
		CDP1834
8708	1024 x 8 PROM	CDP1833
		CDP1834*
8212	Byte I/O	CDP1852
8212	Byte I/O	CDP1852
Intersil		
IM6508	1024 x 1 RAM	CDP1821*
IM6551	256 x 4 RAM	CDP1822*
		MWS5101*
IM6402/6403	UART	CDP1854*
Mostek		
MK4009-9	1024 x 1 RAM	CDP1821
MK4102P-1	1024 x 1 RAM	CDP1821*
MK4102N-1	1024 x 1 RAM	CDP1821*
MK2500P	512 x 8 ROM	CDP1831
		CDP1832
MK2600P	512 x 8 ROM	CDP1831
		CDP1832
Motorola		
MCM2102	1024 x 1 RAM	CDP1821*
MCM6810A	128 x 8 RAM	CDP1823
MCM6830		
MCM65308	1024 x 8 ROM	CDP1833
MCM68308		CDP1834
MCM145101	256 x 4 RAM	CDP1822*
		MWS5101*
MCM2114	1024 x 4 RAM	MWS5114
National		
INSB212	I/O	CDP1852
MM74C930	1024 x 1 RAM	CDP1821
MM87S295/6	512 x 8 EAROM	CDP1831
		CDP1832
MM2102	1024 x 1 RAM	CDP1821*
MM5204C	512 x 8 PROM	CDP1831
		CDP1832
MM5232	512 x 8 ROM	CDP1831
		CDP1832
MM5233	512 x 8 ROM	CDP1831
		CDP1832
MM2101	256 x 4 RAM	CDP1822*
		MWS5101*

*Pin-for-pin compatible.

Cross-Reference Guide

Type	Description	RCA Functionally Equivalent Type
NEC		
μPD6508	1024 x 1 RAM	CDP1821*
μPD2114	1024 x 4 RAM	MWS5114
Signetics		
2101	256 x 4 RAM	CDP1822* MWS5101*
Synertek		
SY2101	256 x 4 RAM	CDP1822* MWS5101*
SY2114	1024 x 4 RAM	MWS5114

*Pin-for-pin compatible.

Type	Description	RCA Functionally Equivalent Type
Texas Instruments		
2101	256 x 4 RAM	CDP1822* MWS5101*
TMS4045	1024 x 4 RAM	MWS5114
TMS4039	256 x 4 RAM	CDP1822
TMS6011	UART	CDP1854*
SN54S/74S474	512 x 8 ROM	CDP1831 CDP1832
SN54S/74S475	512 x 8 ROM	CDP1831 CDP1832
Western Digital		
TR1602A	UART	CDP1854*

Operating Considerations

RCA COS/MOS Integrated Circuits

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

> Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

General Considerations

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

The metal shells of the TO-5 style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar■ leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress.

■Trade Name: Westinghouse Corp.

*Mil-M-38510A, paragraph 3.5.6.1(a), lead material

The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

Handling

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handing considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated circuits".

IC Chips

Integrated-circuit chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the

Operating Considerations

shipping container is opened, the chip must be stored under the following conditions:

A. Storage temperature, 40 °C

B. Relative humidity, 50% max.

C. Clean, dust-free environment.

2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.

3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.

4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the realtively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

CDP1800-Series IC Products

Technical Data

Features and Functional Classifications

The RCA CDP1800 series of integrated circuits includes all the circuit elements needed for an efficient microprocessor system. This comprehensive series offers the user a wide variety of integrated circuits from which he can build his system. In addition to the CDP1802 microprocessor or the soon-to-be-available CDP1804 microcomputer, this series includes:

- A wide complement of RAM's
- ROM's, both custom and standard
- Input/Output (I/O) circuits
- Systems expanders
- RAM decoder latches
- Video interface circuits

This versatile all-COS/MOS series provides the following significant advantages:

- Minimal power-supply requirements
- Completely static circuitry
- High noise immunity
- Wide operating temperature range (−55 °C to +125 °C)
- COS/MOS, TTL, and NMOS compatibility

CDP1800-series integrated circuits are available in two performance selections:

A type without a "C" suffix is the high-performance device. For example, the CDP1802 has:

- 4 V to 10.5 V operating voltage range
- 2.5- or 3.75-μs instruction time (at 25 °C)
- 100-mW power dissipation (typical operating conditions)
- 6.4-MHz maximum clock input frequency at 10 V (at 25 °C)

A type with a "C" suffix, for example, the CDP1802C has:

- 4 V to 6.5 V recommended operating voltage range
- 5- or 7.5-μs instruction time (at 25 °C)
- 10-mW power dissipation (typical operating conditions)
- 3.2-MHz maximum clock input frequency at 5 V (at 25 °C)

Function Classification Chart

Microprocessor and Microcomputer

CDP1802	COSMAC CPU
CDP1804	COSMAC Microcomputer

ROM's (custom)

CDP1831	512 x 8
CDP1832	512 x 8
CDP1833	1024 x 8
CDP1834	1024 x 8

ROM's (standard)

CDPR512	UT4 Utility Program
CDPR522	Microterminal Controller
CDPR582	Fixed-Point Arithmetic

EEPROM

CDP1842	256 x 8

RAM's

CDP1821	1024 x 1
CDP1822	256 x 4
CDP1823	128 x 8
CDP1824	32 x 8
MWS5114*	32 x 8

System Expanders

CDP1856	Bus Buffer (memory)
CDP1858	Address Latch
CDP1859	Address Latch

I/O Circuits

CDP1851	Programmable Interface
CDP1852	Byte I/O
CDP1853	N-Bit Decoder
CDP1854	UART
CDP1855	Multiply-Divide Unit
CDP1857	Bus Buffer (I/O)

RAM Decoder Latches

CDP1866	4-Bit Latch and Decoder Memory Interface
CDP1867	4-Bit Latch and Decoder Memory Interface
CDP1868	4-Bit Latch and Decoder Memory Interface

Video Interface Circuits

CDP1861	Video Display Controller
CDP1862	Color Generator
CDP1863	Tone Generator
CDP1864	PAL-Compatible TV Interface
CDP1869	Address and Sound Generator
CDP1870	Video Generator

*Descriptive data for this type are shown in the section on **General-Purpose Memories**.

CDP1802, CDP1802C Types

COSMAC Microprocessor

Features:

- Typical instruction fetch-execute time of 2.5 or 3.75 μs at V_{DD} = 10 V; 5.0 or 7.5 μs at V_{DD} = 5 V
- Static silicon-gate CMOS circuitry — no minimum clock frequency
- Operating temperature range: — 55 to +125°C (CDP1802D, CDP1802CD); —40 to +85°C (CDP1802E, CDP1802CE)
- High noise immunity, wide operating-voltage range
- Single voltage supply
- Low power
- Single-phase clock; optional on-chip crystal-controlled oscillator
- TTL compatible
- On-chip DMA
- Simple control of reset, run, and pause
- 8-bit parallel organization with bidirectional data bus
- Any combination of standard RAM and ROM
- Memory addressing up to 65,536 bytes
- Flexible programmed I/O mode
- Program interrupt mode
- Four I/O flag inputs directly tested by branch instructions
- Programmable output port
- 91 easy-to-use instructions
- 16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers

The RCA-CDP1802 is an LSI COS/MOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802 includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The COSMAC architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The COSMAC CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802 and CDP1802C are functionally identical. They differ in that the CDP 1802 has a recommended operating voltage range of 4-10.5 volts, and the CDP1802C, a recommended operating voltage range of 4-6.5 volts. These types are supplied in 40-lead dual-in-line ceramic packages (D-suffix), and 40-lead dual-in-line plastic packages (E suffix).

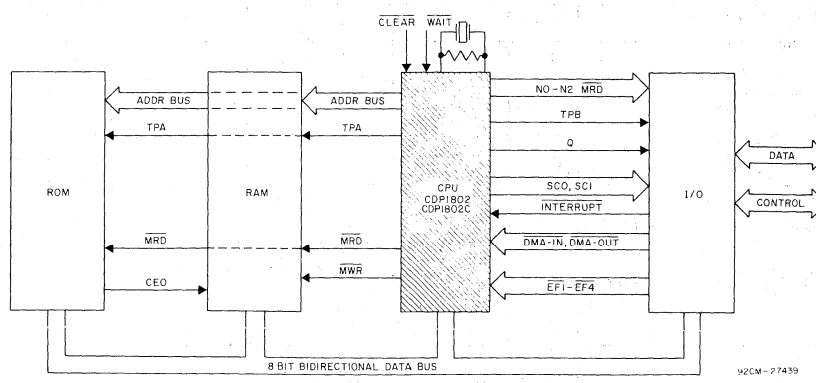


Fig. 1 — Typical CDP1802 microprocessor system.

CDP1802, CDP1802C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltage referenced to V_{SS} Terminal)

CDP1802 . . . . . −0.5 to +11 V

CDP1802C . . . . . −0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW

For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE D) Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE D . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1802D CDP1802E			CDP1802CD CDP1802CE			
	V_O (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	–	5	–	0.01	50	–	0.02	200	µA
	–	–	10	–	1	200	–	–	–	
Output Low Drive (Sink) Current, I_{OL} (Except $\overline{XTAL}$)	0.4	0,5	5	1.1	2.2	–	1.1	2.2	–	mA
	0.5	0,10	10	2.2	4.4	–	–	–	–	
$\overline{XTAL}$ Output I_{OL}	0.4	5	5	75	150	–	75	150	–	µA
Output High Drive (Source) Current I_{OH} (Except $\overline{XTAL}$)	4.6	0,5	5	-0.27	-0.55	–	-0.27	-0.55	–	mA
	9.5	0,10	10	-0.55	-1.1	–	–	–	–	
$\overline{XTAL}$ Output I_{OH}	4.6	0	5	-38	-75	–	-38	-75	–	µA
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05	–	0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,4.5	–	5,10	–	–	1	–	–	1	
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,4.5	–	5,10	4	–	–	4	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	µA
		0,10	10	–	$\pm 10^{-4}$	±1	–	–	–	

*Typical values are for T_A = 25°C.

CDP1802, CDP1802C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1802D CDP1802E			CDP1802CD CDP1802CE			
	V_O (V)	V_{IN} (V)	V_{CC}, V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	μA
	0,10	0,10	10	–	$\pm 10^{-4}$	±1	–	–	–	
Minimum Data Retention Voltage, V_{DR}	$V_{DD} = V_{DR}$			–	2	2.4	–	2	2.4	V
Data Retention Current, I_{DR}	V_{DD} = 2.4 V			–	0.01	1	–	0.5	5	μA

*Typical values are for T_A = 25°C.

RECOMMENDED OPERATING CONDITIONS at T_A = −40 to + 85° C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D CDP1802E	CDP1802CD CDP1802CE	
Supply-Voltage Range	–	–	4 to 10.5	4 to 6.5	V
Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Maximum Clock Input Rise or Fall Time, t_r or t_f	4–10.5	4–10.5	1	1	μs
Instruction Time[2] (See Fig. 8)	5	5	6.4	6.4	μs
	5	10	5.1	–	
	10	10	3.2	–	
Maximum DMA Transfer Rate	5	5	312	312	KBytes/sec
	5	10	390	–	
	10	10	625	–	
Maximum Clock Input Frequency, f_{CLOCK}[3]	5	5	DC – 2.5	DC – 2.5	MHz
	5	10	DC – 3.1	–	
	10	10	DC – 5	–	

NOTES:
1: $V_{CC} \leqslant V_{DD}$; for CDP1802C, $V_{DD} = V_{CC}$ = 5 volts.
2. Equals 2 machine cycles – one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles – one Fetch and two Execute operations.
3. Load Capacitance (C_L) = 50 pF.

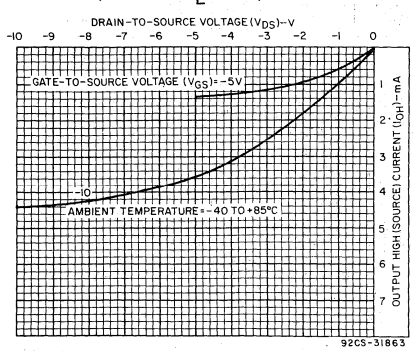


Fig. 2 – Minimum output high (source) current characteristics.

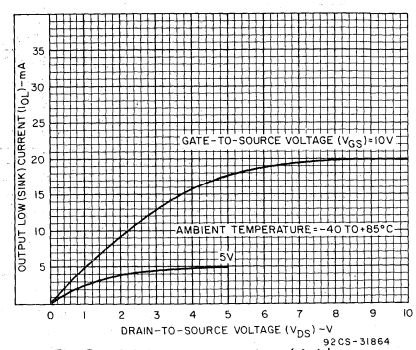


Fig. 3 – Minimum output low (sink) current characteristics.

CDP1802, CDP1802C Types

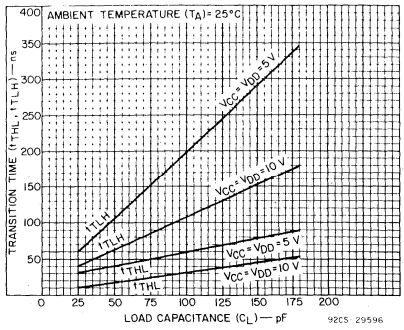


Fig. 4 — Typical transistion time vs. load capacitance.

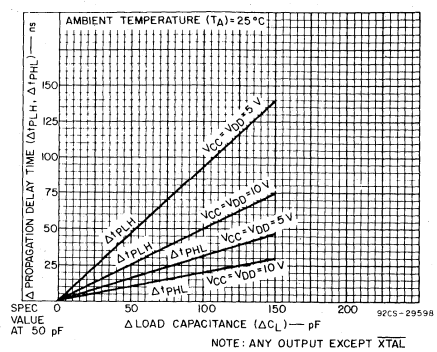


Fig. 5 — Typical change in propagation delay as a function of a change in load capacitance.

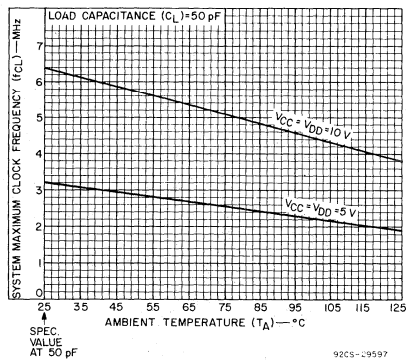
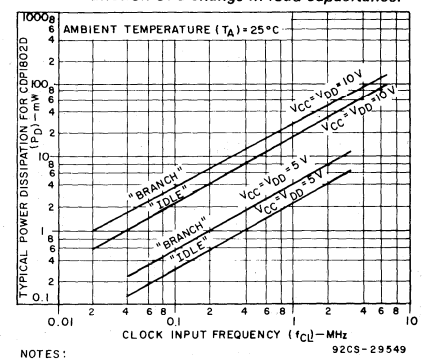


Fig. 6 — Typical maximum clock frequency as a function of temperature.



NOTES:
IDLE = "00" AT M(0000) BRANCH = "3707" AT M(8107) ; C_L = 50 pF

Fig. 7 — Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction for CDP1802.

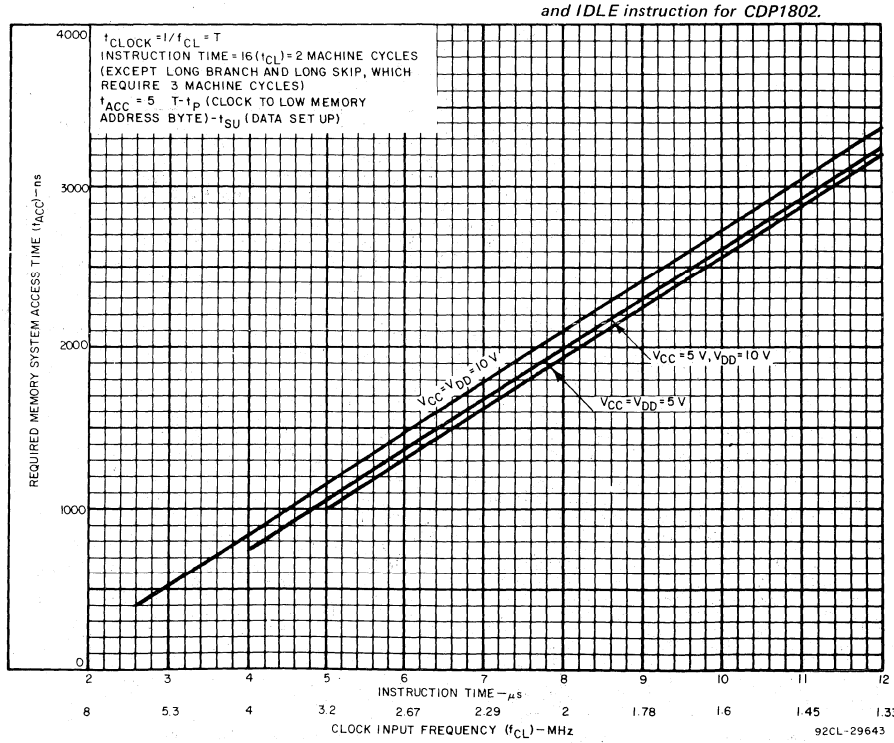


Fig. 8 — Required memory system address time as a function of instruction time.

CDP1802, CDP1802C Types

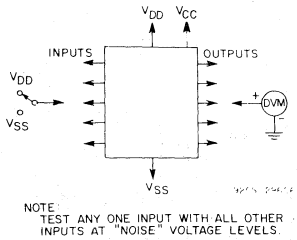


Fig. 9 – Noise immunity test circuit.

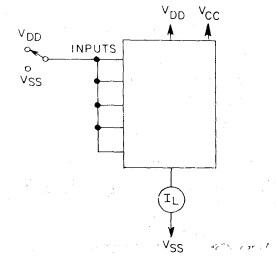


Fig. 10 – Quiescent-device leakage current test circuit.

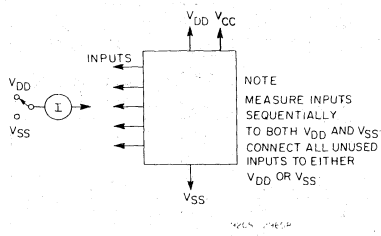


Fig. 11 – Input leakage current test circuit.

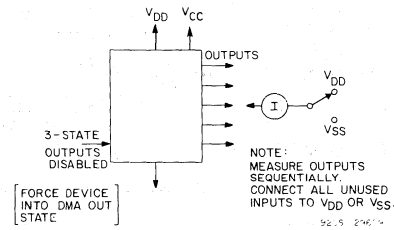
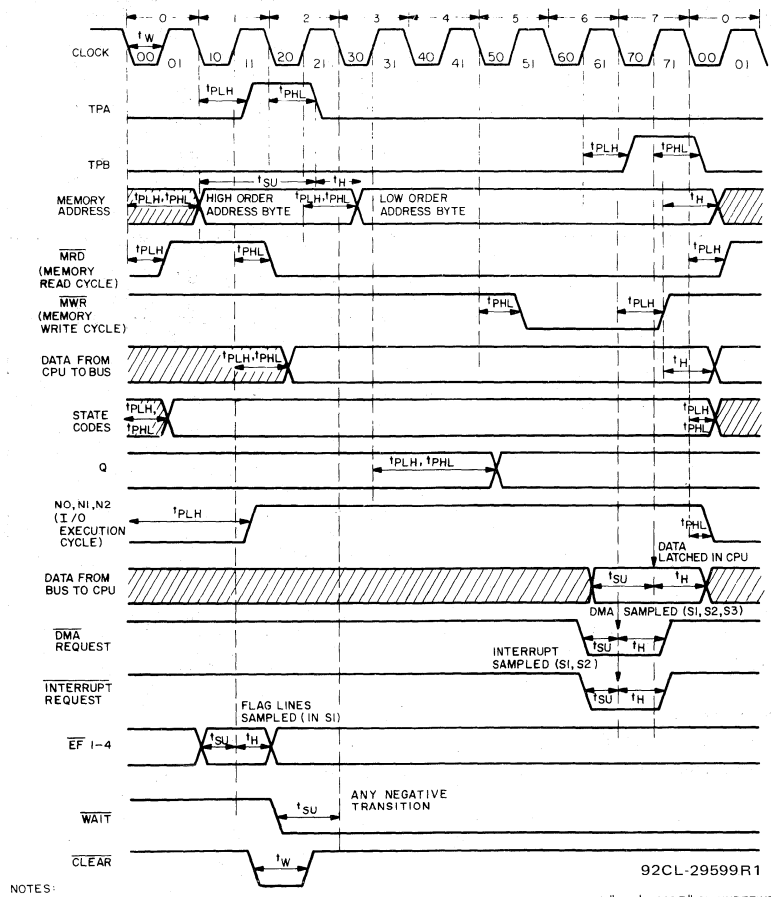


Fig. 12 – Three-state output leakage (data bus) test circuit.



NOTES:
1. THIS TIMING DIAGRAM IS USED TO SHOW SIGNAL RELATIONSHIPS ONLY AND DOES NOT REPRESENT ANY SPECIFIC MACHINE CYCLE
2. ALL MEASUREMENTS ARE REFERENCED TO 50% POINT OF THE WAVEFORMS
3. SHADED AREAS INDICATE "DON'T CARE" OR UNDEFINED STATE; MULTIPLE TRANSITIONS MAY OCCUR DURING THIS PERIOD

Fig. 13 – Timing waveforms.

CDP1802, CDP1802C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, C_L = 50 pF, V_{DD} ±5%, except as noted.

CHARACTERISTIC	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.•	LIMITS Max.	UNITS
Propagation Delay Time, t_{PLH}, t_{PHL}: Clock to TPA, TPB	5	5	300	450	ns
	5	10	250	350	
	10	10	150	200	
Clock-to-Memory High-Address Byte	5	5	900	1350	ns
	5	10	500	750	
	10	10	400	600	
Clock-to-Memory Low-Address Byte	5	5	350	500	ns
	5	10	250	375	
	10	10	150	250	
Clock to $\overline{MRD}$, t_{PLH}	5	5	300	450	ns
	5	10	250	350	
	10	10	150	200	
Clock to $\overline{MRD}$, t_{PHL}	5	5	300	450	ns
	5	10	250	350	
	10	10	150	200	
Clock to $\overline{MWR}$, t_{PLH}, t_{PHL}	5	5	300	450	ns
	5	10	250	350	
	10	10	150	200	
Clock to (CPU DATA to BUS)	5	5	450	650	ns
	5	10	350	450	
	10	10	200	300	
Clock to State Code	5	5	500	750	ns
	5	10	350	450	
	10	10	250	300	
Clock to Q	5	5	350	550	ns
	5	10	250	400	
	10	10	150	250	
Clock to N(0-2), t_{PLH}	5	5	550	800	ns
	5	10	350	500	
	10	10	250	350	
Minimum Setup and Hold Times, t_{SU}, t_H▼ Data Set Up	5	5	-30	0	ns
	5	10	-25	10	
	10	10	-10	20	
Data Hold	5	5	200	300	
	5	10	125	200	
	10	10	100	150	
$\overline{DMA}$ Setup	5	5	-75	0	ns
	5	10	-50	0	
	10	10	-25	0	
$\overline{DMA}$ Hold	5	5	150	250	
	5	10	100	200	
	10	10	75	125	

•Typical values are for T_A = 25°C and nominal V_{DD}.

▼Maximum limits of minimum characteristics are the values above which all devices function.

CDP1802, CDP1802C Types

DYNAMIC ELECTRICAL CHARACTERISTICS (cont'd)

CHARACTERISTIC	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Minimum Setup and Hold Times, t_{SU}, t_H▼					
Interrupt Setup	5	5	-75	0	ns
	5	10	-50	0	
	10	10	-25	0	
Interrupt Hold	5	5	150	250	ns
	5	10	100	200	
	10	10	75	125	
$\overline{WAIT}$ Setup	5	5	-15	0	ns
	5	10	-25	25	
	10	10	0	50	
$\overline{EF1\text{-}4}$ Setup	5	5	-30	0	ns
	5	10	-20	0	
	10	10	-10	0	
$\overline{EF1\text{-}4}$ Hold	5	5	150	250	ns
	5	10	100	200	
	10	10	75	125	
Minimum Pulse Width, t_{WL}▼					
$\overline{CLEAR}$ Pulse Width	5	5	300	600	ns
	5	10	200	400	
	10	10	150	300	
$\overline{CLOCK}$ Pulse Width, t_{WL}	5	5	150	200	ns
	5	10	120	160	
	10	10	75	100	
Typical Total Power Dissipation f = 2 MHz	5	5	4	—	mW
Idle "00" at M(0000), C_L = 50 pF f = 4 MHz	10	10	30	—	
Effective Input Capacitance, C_{IN} Any Input			5	—	pF
Effective 3-State Terminal Capacitance DATA BUS			7.5	—	pF

•Typical values are for T_A = 25°C and nominal V_{DD}.

▼Maximum limits of minimum characteristics are the values above which all devices function.

TIMING SPECIFICATIONS as a function of T ($T=1/f_{CLOCK}$) at T_A = −40 to +85°C.

CHARACTERISTIC	V_{CC} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Typ.•	UNITS
High-Order Memory-Address Byte Setup to $\overline{TPA}$ Time, t_{SU}	5	5	2T-800	2T-600	ns
	5	10	2T-635	2T-475	
	10	10	2T-400	2T-300	
High-Order Memory-Address Byte Hold after TPA Time, t_H	5	5	T/2+0	T/2+30	
	5	10	T/2+0	T/2+20	
	10	10	T/2+0	T/2+10	
Low-Order Memory-Address Byte Hold after WR Time, t_H	5	5	T+0	T+30	
	5	10	T+0	T+20	
	10	10	T+0	T+10	
CPU Data to Bus Hold after WR Time, t_H	5	5	T+25	T+120	
	5	10	T+10	T+75	
	10	10	T+0	T+50	

•Typical values are for T_A = 25°C.

CDP1802, CDP1802C Types

ARCHITECTURE

The COSMAC block diagram is shown in Fig. 14. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, COSMAC instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third, if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);

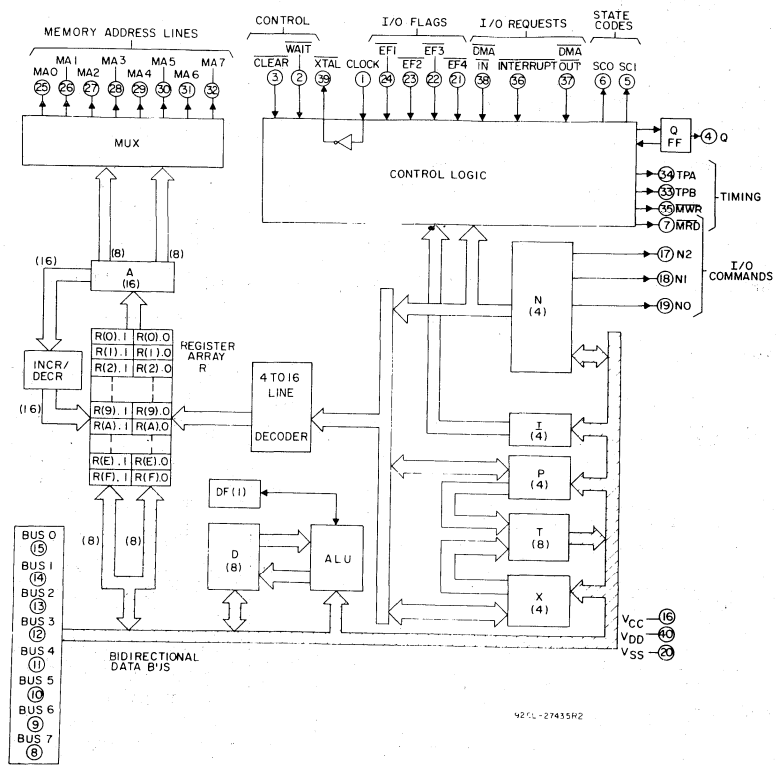


Fig. 14 – CDP1802 block diagram.

5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R (0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions—70-73, 78,60, FO.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the COSMAC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

A program load facility, using the DMA-In channel, is provided to enable users to load programs into the memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized "bootstrap" ROM's.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R (X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer

N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high nybble)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip Flop

CDP1802, CDP1802C Types

INSTRUCTION SET

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
Operation Notation
M(R(N)) →D; R(N) + 1 →R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I – INSTRUCTION SUMMARY

(For Notes, see page 13)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N)) → D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N)) → D; R(N) +1 → R(N)
LOAD VIA X	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X)) → D; R(X) +1 → R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P)) → D; R(P) +1 → R(P)
STORE VIA N	STR	5N	D → M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D → M(R(X)); R(X) –1 → R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1 → R(N)
DECREMENT REG N	DEC	2N	R(N) –1 → R(N)
INCREMENT REG X	IRX	60	R(X) +1 → R(X)
GET LOW REG N	GLO	8N	R(N).0 → D
PUT LOW REG N	PLO	AN	D → R(N).0
GET HIGH REG N	GHI	9N	R(N).1 → D
PUT HIGH REG N	PHI	BN	D → R(N).1
LOGIC OPERATIONS◆◆			
OR	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D → D; R(P) +1 → R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D → D; R(P) +1 → R(P)
AND	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D → D; R(P) +1 → R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR	76◆	
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL	7E◆	

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "–(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

CDP1802, CDP1802C Types

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS♦♦			
ADD	ADD	F4	M(R(X)) + D → DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) + D → DF, D; R(P) +1 → R(P)
ADD WITH CARRY	ADC	74	M(R(X)) + D + DF → DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) + D + DF → DF, D R(P) +1 → R(P)
SUBTRACT D	SD	F5	M(R(X)) – D → DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) – D → DF, D; R(P) +1 → R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X)) – D – (NOT DF) → DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P)) – D – (NOT DF) → DF, D; R(P) +1 → R(P)
SUBTRACT MEMORY	SM	F7	D – M(R(X)) → DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D – M(R(P)) → DF, D; R(P) +1 → R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D – M(R(X)) – (NOT DF) → DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D – M(R(P)) – (NOT DF) → DF, D R(P) +1 → R(P)
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P)) → R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38♦	R(P) +1 → R(P)
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF DF=1	BDF	33♦	IF DF=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B♦	IF DF=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF1=1 ($\overline{EF1}$ = VSS)	B1	34	IF EF1=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF1=0 ($\overline{EF1}$ = VCC)	BN1	3C	IF EF1=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF2=1 ($\overline{EF2}$ = VSS)	B2	35	IF EF2=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF2=0 ($\overline{EF2}$ = VCC)	BN2	3D	IF EF2=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF3=1 ($\overline{EF3}$ = VSS)	B3	36	IF EF3=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF3=0 ($\overline{EF3}$ = VCC)	BN3	3E	IF EF3=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF4=1 ($\overline{EF4}$ = VSS)	B4	37	IF EF4=1, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)
SHORT BRANCH IF EF4=0 ($\overline{EF4}$ = VCC)	BN4	3F	IF EF4=0, M(R(P)) → R(P).0 ELSE R(P) +1 → R(P)

♦NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

♦♦NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
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AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "–(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

CDP1802, CDP1802C Types

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P)) → R(P).1 M(R(P) +1) → R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8◆	R(P) +2 → R(P)
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P)) → R(P).1 M(R(P) +1) → R(P).0 ELSE R(P) +2 → R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38◆	R(P) +1 → R(P)
LONG SKIP (SEE NLBR)	LSKP	C8◆	R(P) +2 → R(P)
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 → R(P) ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 → R(P) ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0) → BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N → P
SET X	SEX	EN	N → X
SET Q	SEQ	7B	1 → Q
RESET Q	REQ	7A	0 → Q
SAVE	SAV	78	T → M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P) → T; (X,P) → M(R(2)) THEN P → X; R(2)–1 → R(2)
RETURN	RET	70	M(R(X)) → (X,P); R(X) +1 → R(X) 1 → IE
DISABLE	DIS	71	M(R(X)) → (X,P); R(X) +1 → R(X) 0 → IE

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA-OUT}}$) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1→R(X); N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1→R(X); N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1→R(X); N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1→R(X); N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1→R(X); N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1→R(X); N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1→R(X); N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR)

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

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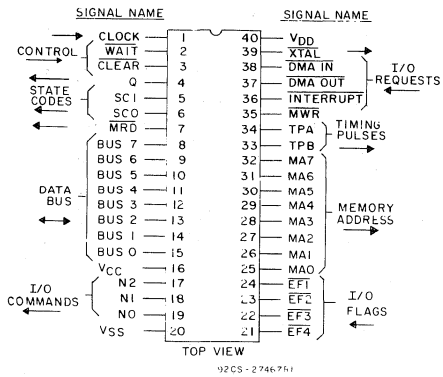
TERMINAL ASSIGNMENT



SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus):

8-bit directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Lines):

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{MRD}$ = VCC: Data from I/O to CPU and Memory

$\overline{MRD}$ = VSS: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags):

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests):

These inputs are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT

SC0, SC1, (2 State Code Lines):

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H=VCC, L=VSS.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses):

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines):

In each cycle, the higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{MWR}$ (Write Pulse):

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level):

A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory **does** not have a three-state high-impedance output, $\overline{MRD}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q:

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK:

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at VCC=VDD=10 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$:

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information see ICAN-6565.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$ (2 Control Lines):

Provide four control modes as listed in the following truth table.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (VSS) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Powerup reset can be realized by connecting a buffered RC network to $\overline{\text{CLEAR}}$. For additional information see ICAN-6581.

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

V_{DD}, V_{SS}, V_{CC} (Power Levels):

The internal voltage supply VDD is isolated from the Input/Output voltage supply VCC so that the processor may operate at maximum speed while interfacing with various external circuit technologies, including T2L at 5 volts. VCC must be less than or equal to VDD. All outputs swing from VSS to VCC. The recommended input voltage swing is VSS to VCC.

RUN-MODE STATE TRANSITIONS

The CDP1802 and CDP1802C CPU state transitions when in the RUN, RESET, and LOAD modes are shown in Fig. 15. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle, which requires 9 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response. Table II shows the conditions on Data Bus and Memory-Address lines during all machine states.

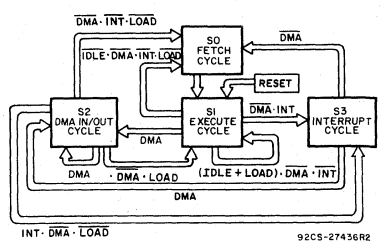


Fig. 15 – CDP1802 microprocessor state transistions.

CDP1802, CDP1802C Types

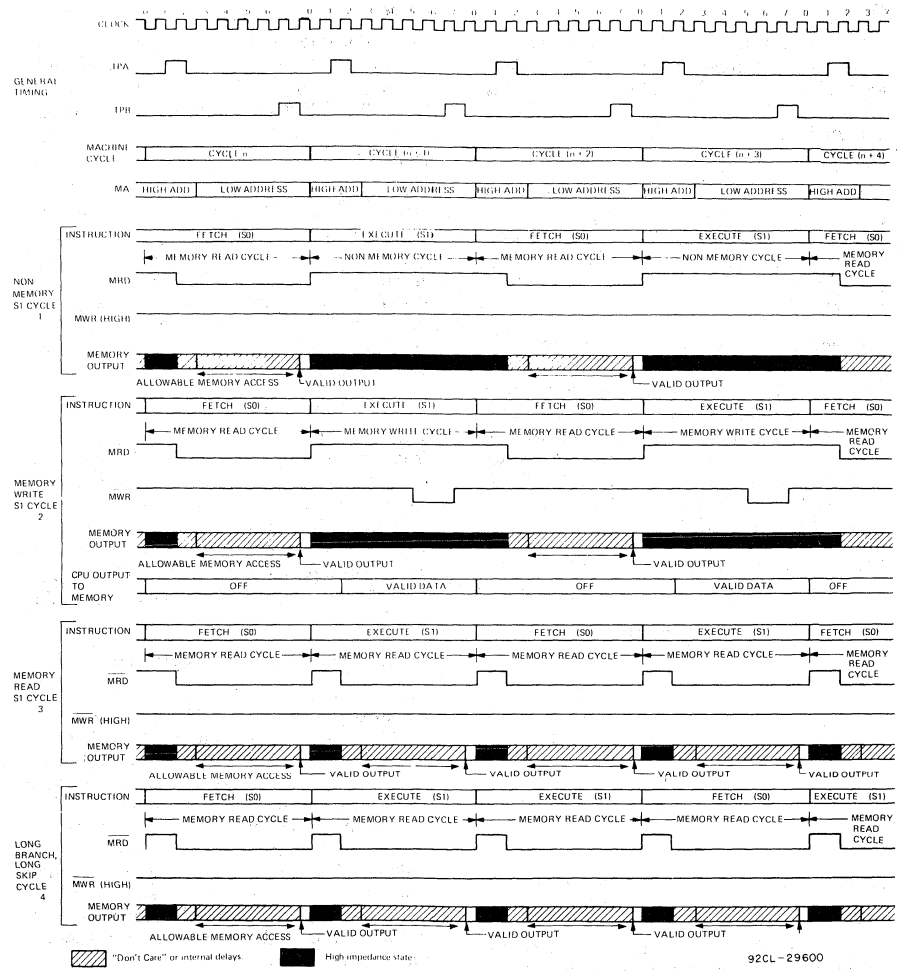


Fig. 16- Timing diagram for machine cycle type Nos. 1, 2, 3, and 4 (propagation delays not shown).

CDP1802, CDP1802C Types

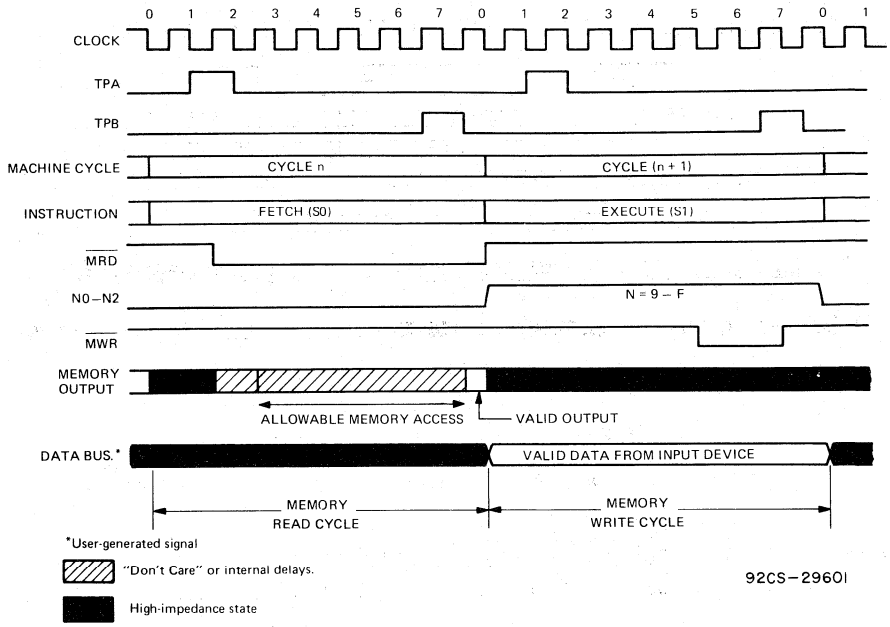


Fig. 17 – Timing diagram for machine cycle type No. 5 (propagation delays not shown).

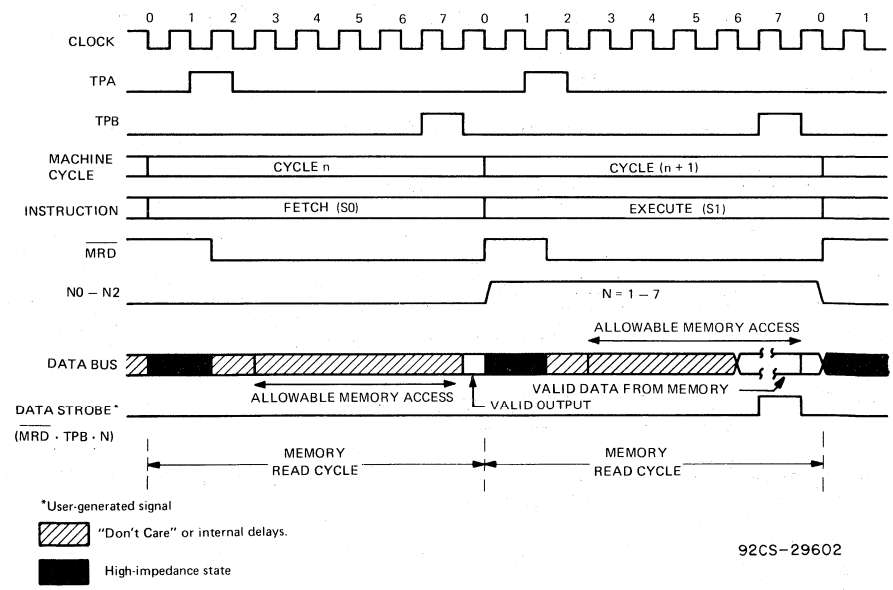


Fig. 18 – Timing diagram for machine cycle type No. 6 (propagation delays not shown).

CDP1802, CDP1802C Types

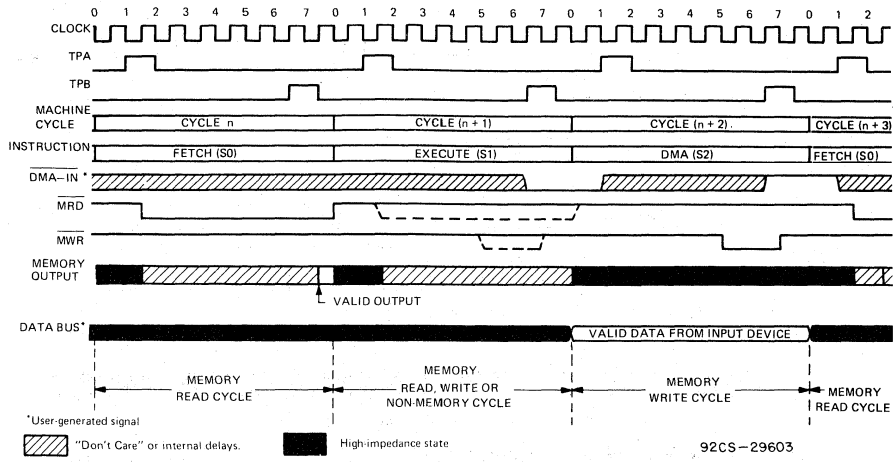


Fig. 19 – Timing diagram for machine cycle type No. 7 (propagation delays not shown).

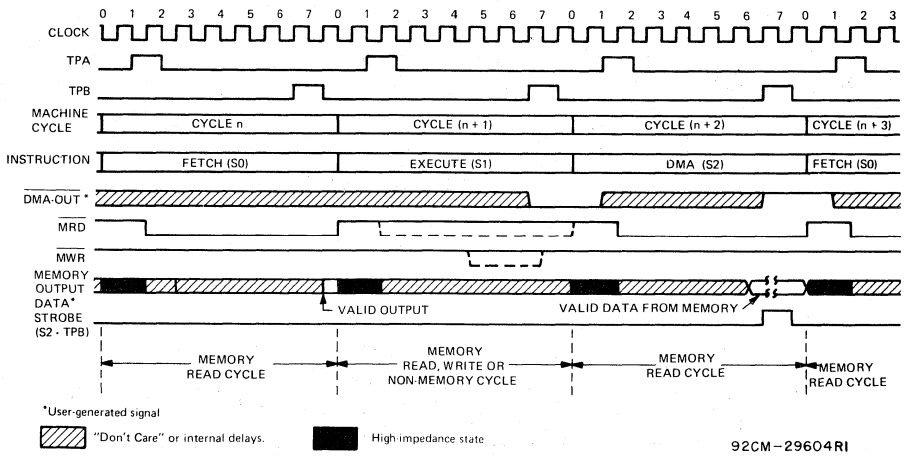


Fig. 20 – Timing diagram for machine cycle type No. 8 (propagation delays not shown).

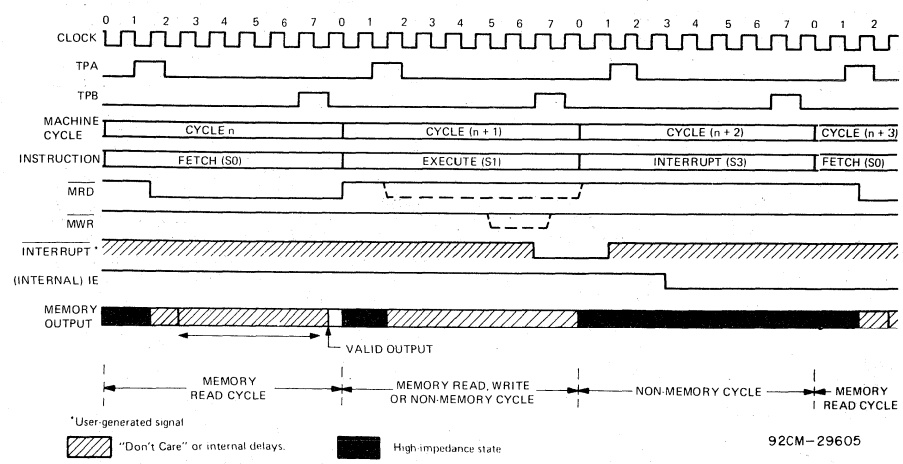


Fig. 21 – Timing diagram for machine cycle type No. 9 (propagation delays not shown).

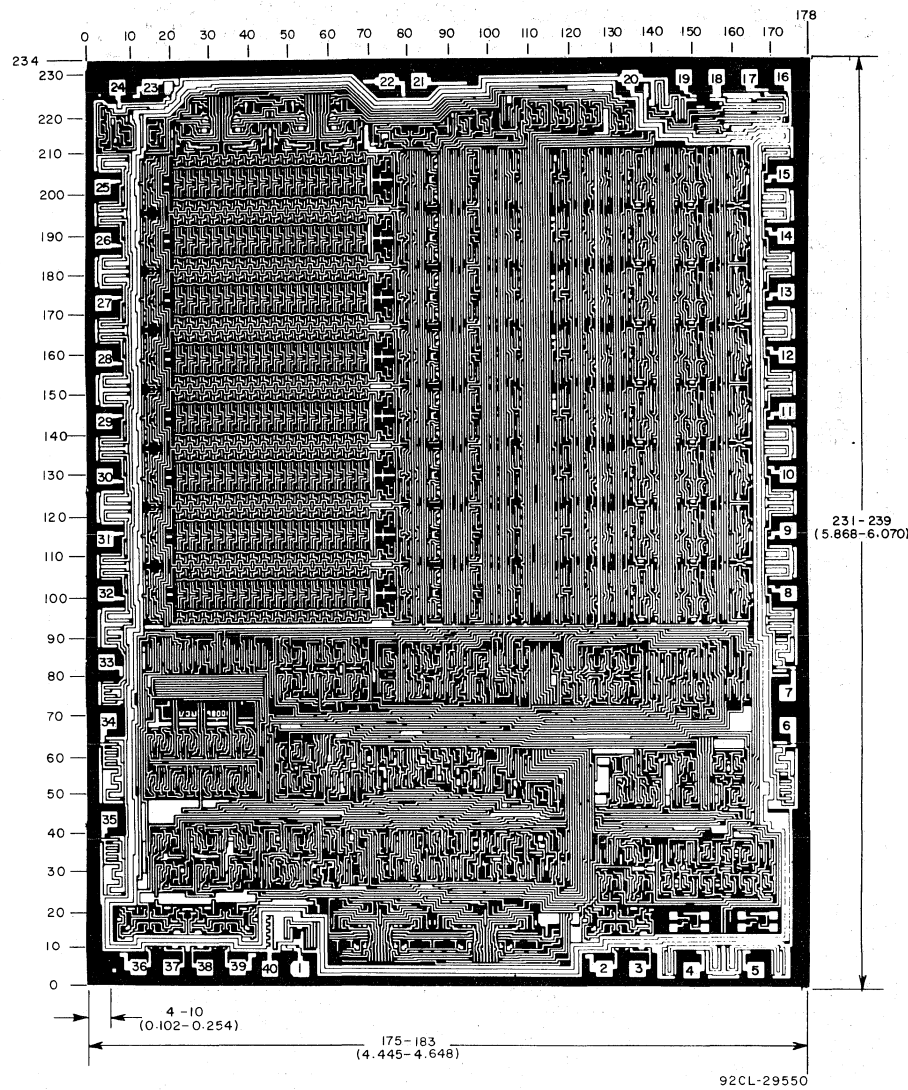
CDP1802, CDP1802C Types

TABLE II. CONDITIONS ON DATA BUS AND MEMORY ADDRESS LINES DURING ALL MACHINE STATES

STATE	I	N	MNEMONIC	INSTRUCTION	OPERATION	DATA BUS	MEMORY ADDRESS	$\overline{MRD}$	NOTES[G]
S1	RESET				JAM: I,N,Q,X,P = 0 IE = 1	0	R (0) UNDEFINED	1	A
	FIRST CYCLE AFTER RESET NOT PROGRAMMER ACCESSIBLE				INITIALIZE: R(0)←0	0	R (0) UNDEFINED	1	B
S0	FETCH				M(R(P))→I.N R(P)+1	M(R(P))	R(P)	0	C
S1 (Execute)	0	0	IDL	IDLE	[Load = 0 (Program Idle)]	M (R(0))	R (0)	0	D,3
					[Load = 1 (Load Mode)]	M(R(0))	PREVIOUS ADDRESS	0	E,3
		N≠0	LDN	LOAD D VIA N	M(R(N))→D	M(R(N))	R(N)	0	3
	1	N	INC	INCREMENT	R(N)+1	FLOAT	R(N)	1	1
	2	N	DEC	DECREMENT	R(N)−1	FLOAT	R(N)	1	1
	3	N	–	SHORT BRANCH	[BRANCH NOT TAKEN]	M(R(P))	R(P)	0	3
					[BRANCH TAKEN]	M(R(P))	R(P)	0	
	4	N	LDA	LOAD ADVANCE	M(R(N))→D R(N)+1	M(R(N))	R(N)	0	3
	5	N	STR	STORE VIA N	D→M(R(N))	D	R(N)	1	3
	6	0	IRX	INC REG X	R(X)+1	M(R(X))	R(X)	0	3
		N=1–7	OUT N	OUTPUT	M(R(X))→BUS R(X)+1	M(R(X))	R(X)	0	6
		N=9–F	INP N	INPUT	BUS→M(R(X)), D	I/O DEVICE	R(X)	1	5
	7	0	RET	RETURN	M(R(X))→(X,P) R(X)+1; 1→IE	M(R(X))	R(X)	0	3
		1	DIS	DISABLE	M(R(X))→(X,P) R(X)+1; 0→IE	M(R(X))	R(X)	0	3
		2	LDXA	LOAD VIA X AND ADVANCE	M(R(X))→D R(X)+1	M(R(X))	R(X)	0	3
		3	STXD	STORE VIA X AND DECREMENT	D→M(R(X)) R(X)−1	D	R(X)	1	2
		4,5,7	–		ALU OPERATION	M(R(X))	R(X)	0	3
		6	–		ALU OPERATION	FLOAT	R(X)	1	1
		8	SAV	SAVE	T→M(R(X))	T	R(X)	1	2
		9	MARK	MARK	(X,P)→T, M(R(2)) P→X; R(2)−1	T	R(2)	1	2
		A	REQ	RESET Q	Q = 0	FLOAT	R(P)	1	1
		B	SEQ	SET Q	Q = 1	FLOAT	R(P)	1	1
		C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	3
		E			ALU OPERATION	FLOAT	R(P)	1	1
	8	N	GLO	GET LOW	R(N) .0→D	R(N) .0	R(N)	1	1
	9	N	GHI	GET HIGH	R(N) .1→D	R(N) .1	R(N)	1	1
	A	N	PLO	PUT LOW	D→R(N).0	D	R(N)	1	1
	B	N	PHI	PUT HIGH	D→R(N) .1	D	R(N)	1	1
	C	0,1,2 3,8,9 A,B		LONG BRANCH	[BRANCH NOT TAKEN]	M(R(P))	R(P)	0	4
					[BRANCH TAKEN]	M(R(P))	R(P)	0	4
		5,6,7 C,D,E F		LONG SKIP	[SKIP NOT TAKEN]	M(R(P))	R(P)	0	4
					[SKIP TAKEN]	M(R(P))	R(P)	0	4
		4	NOP	NO OPERATION	NO OPERATION	M(R(P))	R(P)	0	4
	D	N	SEP	SET P	N→P	N N	R(N)	1	1
	E	N	SEX	SET X	N→X	N N	R(N)	1	1
	F	0	LDX	LOAD VIA X	M(R(X))→D	M(R(X))	R(X)	0	3
		1,2,3 4,5,7			ALU OPERATION	M(R(X))	R(X)	0	3
		6	SHR	SHIFT RIGHT	SHIFT D RIGHT LSB(D)→DF 0→MSB(D)	FLOAT	R(X)	1	1
		8	LDI	LOAD IMMEDIATE	M(R(P))→D R(P)+1	M(R(P))	R(P)	0	3
		9,A,B C,D,F			ALU OPERATION IMMEDIATE	M(R(P))	R(P)	0	3
		E	SHL	SHIFT LEFT	ALU OPERATION	FLOAT	R(P)	1	1
S2	IN REQUEST			DMA IN	BUS→M(R(0))	I/O DEVICE	R (0)	1	F,7
	OUT REQUEST			DMA OUT	M(R(0))→BUS	M(R(0))	R (0)	0	F,8
S3	INTERRUPT				X,P→T, 0→IE 2→X, 1→P	FLOAT	R(N)	1	9

NOTES:
A. IE = 1; TPA, TPB suppressed, state = S1
B. BUS = 0 for entire cycle
C. Next state always S1
D. Wait for DMA or INTERRUPT
E. Suppress TPA, wait for DMA
F. IN REQUEST has priority over OUT REQUEST
G. Numbers refer to machine cycles types — refer to timing diagrams, Figs. 16 through 20.

CDP1802, CDP1802C Types



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

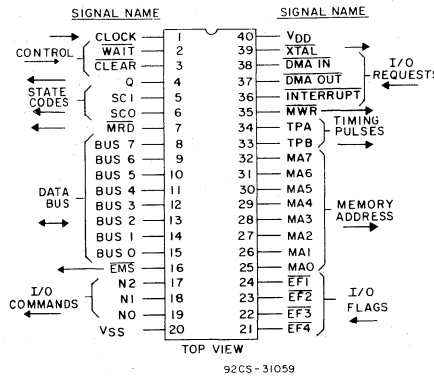
Dimensions and pad layout for CDP1802.

CDP1804, CDP1804C Types
Objective Data

COSMAC Microcomputer

Features:

- **Typical instruction fetch-execute time of 2.5 or 3.75 μs at V_{DD} = 5 V**
- **Static CMOS circuitry — no minimum clock frequency**
- **Single voltage supply**
- **High noise immunity, wide operating voltage range**
- **Low power**
- **Operating temperature range:**
  −55 to +125°C (CDP1804D, CDP1804CD)
  −40 to +85°C (CDP1804E, CDP1804CE)
- **8-Bit parallel organization**
- **Pinout same as CDP1802 except for V_{CC} terminal**
- **Contains ROM, RAM, I/O, and Timer/Counter**
- **Expandable in memory and I/O**
- **On-chip oscillator controlled by crystal or RC network; single phase clock**
- **Upwards software compatible with CDP1802**
- **113 easy-to-use instructions**
- **16 x 16 matrix of registers for use as multiple program counters, data pointers or data registers**
- **Test mode allows prototyping with external memory**



TERMINAL ASSIGNMENT

The RCA-CDP1804 and CDP1804C are LSI CMOS 8-bit register-oriented microcomputers designed for use in a wide variety of general-purpose computing and control applications. They can provide an effective cost and minimum chip-count solution for many low-level applications.

The CDP1804 contains a 2048-byte mask-programmable ROM, 64 bytes of executable RAM, and an 8-bit presettable down-counter with a conditional ÷ 32 prescaler, in addition to the standard architecture of the CDP1802 microprocessor. This includes a bank of 16 registers of 16 bits each that can be used as multiple program counters, pointers to data in memory, or as data storage registers and a complement of Input/Output lines including 3 "N-bit" selection lines, four flag-input lines, one serial-output line and the DMA and Interrupt Request inputs. Upwards software compatibility is maintained since the CDP1804 contains the entire instruction set of the CDP1802 plus 22 added instructions. The terminal arrangements of the two devices are identical except that the V_{CC} terminal is eliminated, and an External Memory Select ($\overline{EMS}$) terminal is substituted. This output is at a low level whenever external memory is being addressed, allowing simple add-on external memory expansion. The starting address for the internal ROM is programmable in increments of 2K bytes. The starting address for the RAM is programmable in increments of 64 bytes. The CDP1804 performs the same functions as the CDP1802, except that the Load Mode of the CDP1802 is replaced with a Test Mode in the CDP1804. The Test Mode disables both internal ROM and RAM, and enables external memory. The new instructions are all 3 or more-cycle instructions. Timing for the CDP1804 is the same as the CDP1802, except 4.5 clock pulses are provided for memory access, Q changes 1/2 cycle earlier during SEQ and REQ instructions, and flag lines are sampled at the end of the S0 machine cycle.

The counter/timer generates an interrupt at count '0' and then is automatically re-initialized. It has several modes of operation, all under software control:

- Event counter — counter decremented by EF1 or EF2.
- Timer — counter decremented by TPA divided by 32.
- Pulse duration measurements — TPA clocks to counter are gated by EF1 or EF2 lines.

The CDP1804 and CDP1804C are functionally identical. They differ in that the CDP1804 has an operating voltage range of 4 to 10.5 volts and the CDP1804C has an operating voltage range of 4 to 6.5 volts. Both are supplied in 40-lead hermetic dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix).

CDP1804, CDP1804C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1804 . . . . . −0.5 to +11 V
CDP1804C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = −40 to +85°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS		LIMITS[1]				UNITS
			CDP1804D CDP1804E		CDP1804CD CDP1804CE		
	f_{CL} (MHz)	V_{DD} (V)	Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	–	4	10.5	4	6.5	V
Input Voltage Range	–	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Input Rise or Fall Time, t_rCL, t_fCL	–	4 – 6.5	–	1	–	1	μs
	–	4 – 10.5	–	1	–	–	
Instruction Time[2]	4	5	4		4		μs
	8	10	2		–		
DMA Transfer Rate	–	5	–	2	–	2	M Bytes/sec
	–	10	–	4	–	–	
Clock Input Frequency, f_{CL}[3]	–	5	DC	4	DC	4	MHz
	–	10	DC	8	–	–	

NOTES:
1. Typical values for Instruction Time.
2. Equals 2 machine cycles – one Fetch and one Execute operation for all instructions except Long Branch, Long Skip, NOP, and "68" family instructions, which are more than two cycles.
3. Load Capacitance (C_L) = 50 pF.

DYNAMIC POWER DISSIPATION at T_A=25°C

ALL TYPES
8 mW Typ. at V_{DD} = 5 V, f_{CL} = 4 MHz

CDP1804D, CDP1804E
80 mW Typ. at V_{DD} = 10 V, f_{CL} = 8 MHz

DATA RETENTION VOLTAGE

ALL TYPES
2 V Min. at T_A = 25°C
2.5 V Min. at T_A = −40 to +85°C

CDP1804, CDP1804C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1804D CDP1804E			CDP1804CD CDP1804CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	0,5	5	–	10	–	–	10	–	μA
	–	0,10	10	–	100	–	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.68	4	–	1.68	4	–	mA
($\overline{\text{Except XTAL}}$)	0.5	0,10	10	4.4	10.4	–	–	–	–	
$\overline{\text{XTAL}}$ Output I_{OL}	0.4	5	5	76	170	–	76	170	–	μA
Output High Drive (Source) Current I_{OH}	4.6	0,5	5	−1.68	−4	–	−1.68	−4	–	mA
($\overline{\text{Except XTAL}}$)	9.5	0,10	10	−4.4	−10.4	–	–	–	–	
$\overline{\text{XTAL}}$ Output I_{OH}	4.6	0	5	−38	−85	–	−38	−85	–	μA
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05	–	0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	±0.1	±1	–	±0.1	±1	μA
		0,10	10	–	±0.1	±1	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	±0.2	±2	–	±0.2	±2	μA
	0,10	0,10	10	–	±0.2	±2	–	–	–	

* Typical values are for T_A = 25°C.

ARCHITECTURE

The CDP1804 block diagram is shown in Fig. 2. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With few exceptions, COSMAC instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and more if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one

CDP1804, CDP1804C Types

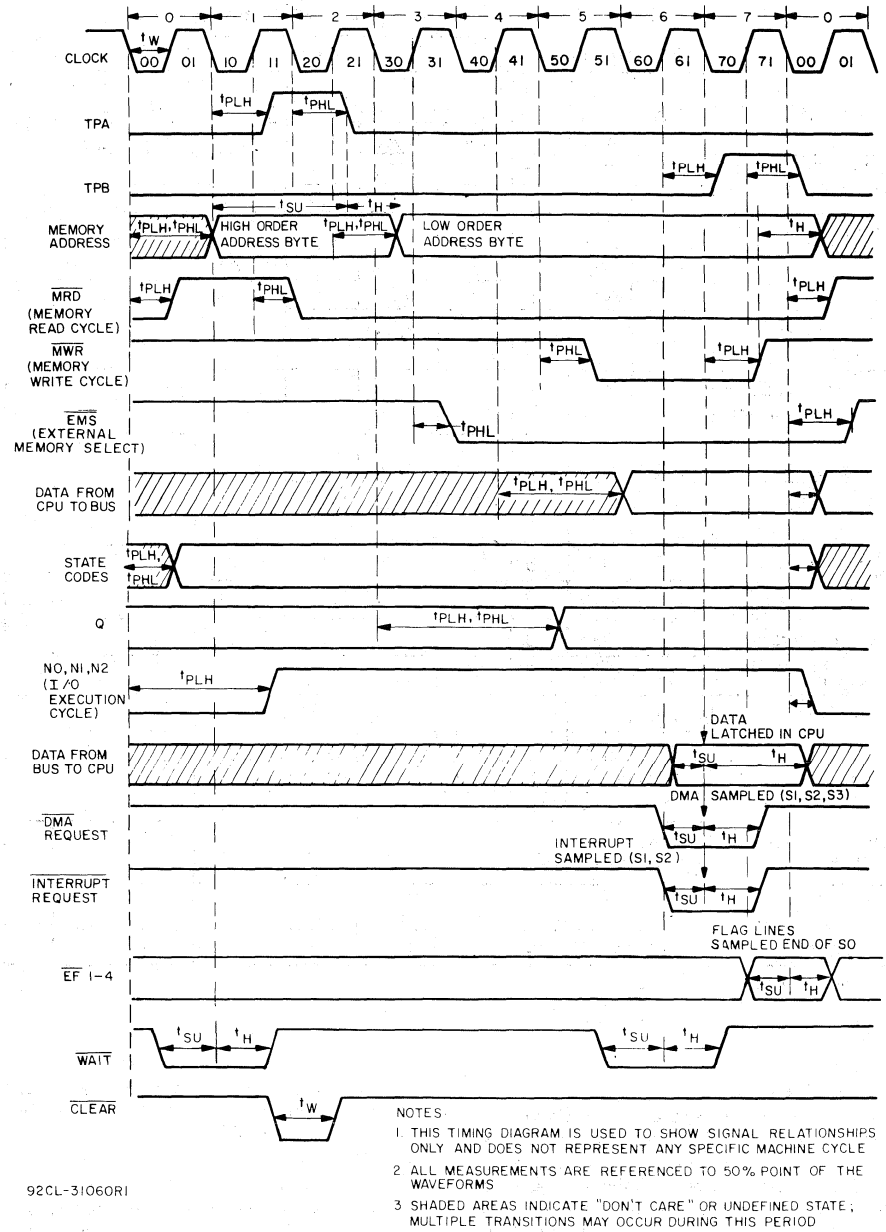


Fig. 1 – Timing waveforms.

so that R(P) is now "pointing" to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);

CDP1804, CDP1804C Types

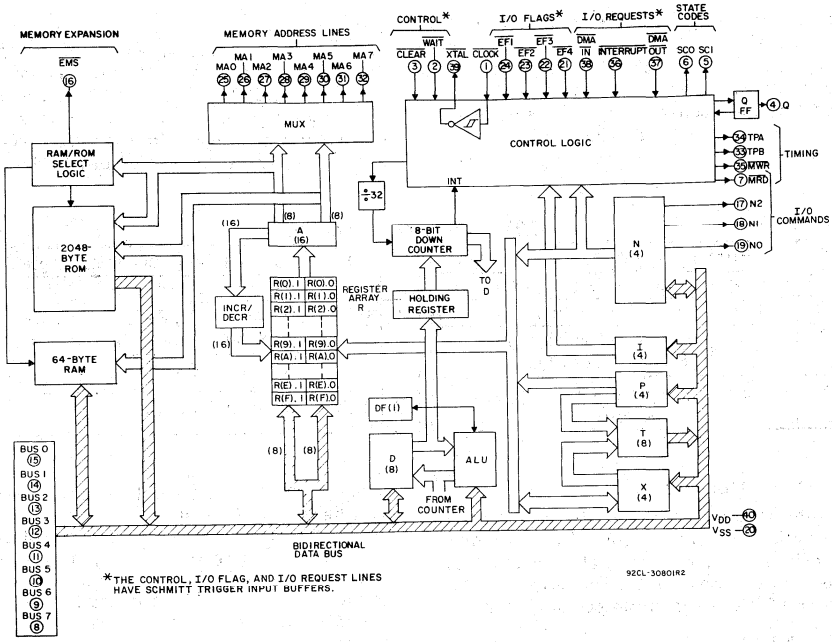


Fig. 2 – Block diagram for CDP1804.

5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the user's interrupt servicing routine. After reset, and during a DMA operation, R (0) is used as the program counter. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F1-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions—70-73, 78, 60, F0.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions, the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the COSMAC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this

CDP1804, CDP1804C Types

mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction), the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically de-

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)	N	4 Bits	Holds Low-Order Instr. Digit
DF	1 Bit	Data Flag (ALU Carry)	I	4 Bits	Holds High-Order Instr. Digit
R	16 Bits	1 of 16 Scratchpad Registers	T	8 Bits	Holds old X, P after Interrupt (X is high nybble)
P	4 Bits	Designates which register is Program Counter	IE	1 Bit	Interrupt Enable
X	4 Bits	Designates which register is Data Pointer	Q	1 Bit	Output Flip Flop

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. It can also be driven by the output of the counter. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request occurs activated to inhibit further interruptions. The user's interrupt routine is now in control; the contents of T may be saved by means of a single instruction (78) in the memory location pointed to by R (X). At the conclusion of the interrupt, the user's routine may restore the pre-interrupted value of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

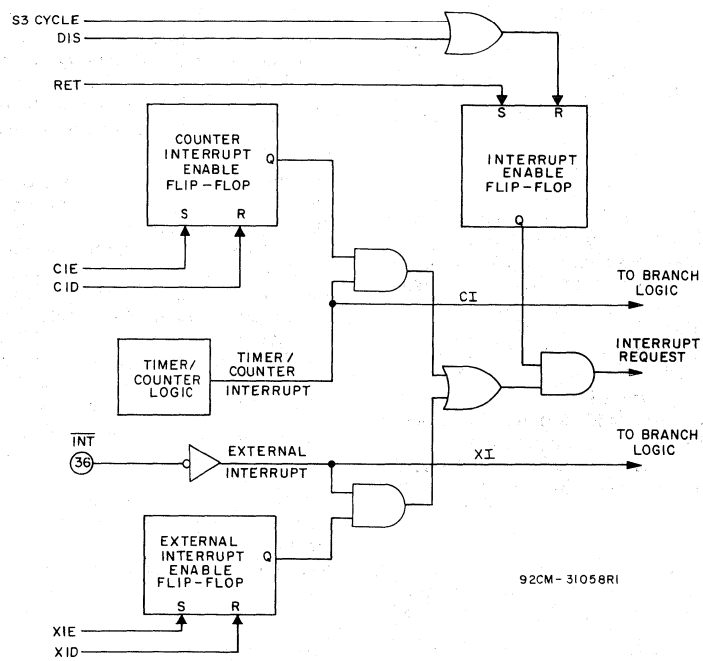


Fig. 3 – CDP1804 interrupt logic control diagram.

Interrupts can be generated either externally through the Interrupt input, or internally via the counter on the transition from count $(01)_{16}$ to its next value. Short branch instructions on Counter Interrupt and External Interrupt provide a means of identifying the source of the interrupt. The branch will be taken if an interrupt request is pending, regardless of the state of the interrupt enable flip-flop. The counter interrupt request flip-flop will be reset if its branch is taken. Interrupt logic control is shown in Fig. 3.

Counter and Controls

This logic consists of a presettable 8-bit down-counter (Module N type), and a conditional divide-by 32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the timer/counter interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a load instruction to the counter, the counter and its buffer register are loaded, the prescaler reset, the mode reset and any previous interrupts cleared. Read operations do not affect the counter.

The counter has the following five programmable modes:

1. Event counter 1: input to counter is connected to the $\overline{EF1}$ terminal. The high-to-low transition decrements the counter.
2. Event counter 2: Input to counter is connected to the $\overline{EF2}$ terminal. The high-to-low transition decrements the counter.
3. Timer: Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA.
4. Pulse duration measurement 1: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal is low. On the transition of this signal to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter decrements to "one" while the input is low, interrupt will also be set, but the counter will continue.
5. Pulse duration measurement 2: Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF2}$ terminal is low. On the transition of this signal to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter decrements to "one" while the input is low, interrupt will also be set, but the counter will continue.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The stop counter (STPC) command clears the counter mode and stops counting.

In addition to the five programmable modes, the decrement counter instruction (DTC) enables the user to count in software. In order to avoid conflict with counting done in the event counter mode, the instruction should be used only after the mode has been cleared by a stop counter instruction.

The toggle Q enable command connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q line changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops.

Memory

The locations of ROM and RAM in the CDP1804 are determined by AND-gate decoders which decode the upper memory addresses and are programmable at the time of ROM pattern masking. The logical values of the decoder inputs are selectable as 1 (positive), 0 (negative), or X (don't care). A 5-bit decoder is used for the ROM selection, so the ROM can be placed at one or more 2K blocks in memory. Similarly, the RAM has a 10-bit decoder and can be selected at one or more of the 1024, 64-byte spaces within the 65,536 locations of memory. If the RAM is located within the ROM space, the RAM will be enabled at the locations where both are mapped.

An External Memory Select output ($\overline{EMS}$) is provided for memory expansion. This output is low whenever the external memory is being addressed, i.e. during a memory reference machine cycle in which the address does not correspond to internal ROM or RAM. Both internal ROM and RAM are disabled when the Test Mode is activated ($\overline{CLEAR}$ = $\overline{WAIT}$ = low) forcing all instructions to be fetched and executed from external memory. In this case, $\overline{EMS}$ is low for any internal or external memory reference machine cycle. $\overline{EMS}$ is low only when an external memory reference operation is in progress, and the addresses are stable.

CDP1804, CDP1804C Types

INSTRUCTION SET

The CDP1804 instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation
M(R(N)) → D; R(N) + 1 → R(N)

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I – INSTRUCTION SUMMARY
(For Notes, see page 12)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N)) → D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N)) → D; R(N) +1 → R(N)
LOAD VIA X	LDX	F0	M(R(X)) → D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X)) → D; R(X) + 1 → R(X)
LOAD IMMEDIATE	LDI	F8	M(R(P)) → D; R(P) +1 → R(P)
STORE VIA N	STR	5N	D → M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D → M(R(X)); R(X) –1 → R(X)
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1 → R(N)
DECREMENT REG N	DEC	2N	R(N) –1 → R(N)
INCREMENT REG X	IRX	60	R(X) +1 → R(X)
GET LOW REG N	GLO	8N	R(N).0 → D
PUT LOW REG N	PLO	AN	D → R(N).0
GET HIGH REG N	GHI	9N	R(N).1 → D
PUT HIGH REG N	PHI	BN	D → R(N).1
LOGIC OPERATIONS◆◆			
OR	OR	F1	M(R(X)) OR D → D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D → D; R(P) +1 → R(P)
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D → D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D → D; R(P) +1 → R(P)
AND	AND	F2	M(R(X)) AND D → D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D → D; R(P) +1 → R(P)
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D) → DF, 0 → MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D) → DF, DF → MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D) → DF, 0 → LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D) → DF, DF → LSB(D)
RING SHIFT LEFT	RSHL		
REGISTER LOAD VIA X AND ADVANCE	RLXA	686N	M(R(X)) → R(N).1; M(R(X) +1) → R(N).0; R(X) +2 → R(X)
REGISTER LOAD IMMEDIATE	RLDI	68CN	M(R(P)) → R(N).1; M(R(P) +1) → R(N).0; R(P) +2 → R(P)
REGISTER STORE VIA X AND DECREMENT	RSXD	68AN	R(N).0 → M(R(X)); R(N).1 → M(R(X)-1); R(X) –2 → R(X)
REGISTER N TO REGISTER X COPY	RNX	68BN	R(N) → R(X)

CDP1804, CDP1804C Types

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS◆◆			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1→R(P)
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1→R(P)
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P) +1→R(P)
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P) +1→R(P)
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P) +1→R(P)
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P) +1→R(P)
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38◆	R(P) +1→R(P)
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF DF=1	BDF	33◆	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B◆	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF1=1 ($\overline{EF1}$ = V_{SS})	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF1=0 ($\overline{EF1}$ = V_{DD})	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF2=1 ($\overline{EF2}$ = V_{SS})	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF2=0 ($\overline{EF2}$ = V_{DD})	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF3=1 ($\overline{EF3}$ = V_{SS})	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF3=0 ($\overline{EF3}$ = V_{DD})	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF4=1 ($\overline{EF4}$ = V_{SS})	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH IF EF4=0 ($\overline{EF4}$ = V_{DD})	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1→R(P)
SHORT BRANCH ON COUNTER INTERRUPT	BCI	683E	IF CI=1, M(R(P))→R(P).0; 0→CI ELSE R(P) +1→R(P)
SHORT BRANCH ON EXTERNAL INTERRUPT	BXI	683F	IF XI=1, M(R(P))→R(P).0 ELSE R(P) +1→R(P)

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.

AFTER AN ADD INSTRUCTION:
- DF = 1 DENOTES A CARRY HAS OCCURRED
- DF = 0 DENOTES A CARRY HAS NOT OCCURRED

AFTER A SUBTRACT INSTRUCTION:
- DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
- DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT

THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

CDP1804, CDP1804C Types

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8◆	R(P) +2→R(P)
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2→R(P)
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38◆	R(P) +1→R(P)
LONG SKIP (SEE NLBR)	LSKP	C8◆	R(P) +2→R(P)
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2→R(P) ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2→R(P) ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)–1→R(2)
ENABLE TOGGLE Q	ETQ	6809■	COUNTER = 01 AND COUNTER CLOCK ↓ ⇒ $\overline{Q}$→Q

■ETQ cleared by LDC, reset of CPU, or BCI • (CI = 1).

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA-OUT}}$) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

CDP1804, CDP1804C Types

TABLE I – INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
COUNTER INSTRUCTIONS			
LOAD COUNTER	LDC	6806	D→COUNTER
GET COUNTER	GEC	6808	COUNTER→D
STOP COUNTER	STPC	6800	0→COUNTER CLOCK
DECREMENT COUNTER	DTC	6801	COUNTER – 1→COUNTER
SET TIMER MODE AND START	STM	6807	TPA÷32→COUNTER CLOCK
SET COUNTER MODE 1 AND START	SCM1	6805	EF1→COUNTER CLOCK
SET COUNTER MODE 2 AND START	SCM2	6803	EF2→COUNTER CLOCK
SET PULSE WIDTH MODE 1, START	SPM1	6804	TPA·EF1→COUNTER CLOCK; $\overline{EF1}$ ↓ STOPS COUNT
SET PULSE WIDTH MODE 2, START	SPM2	6802	TPA·EF2→COUNTER CLOCK; $\overline{EF2}$ ↓ STOPS COUNT
INTERRUPT CONTROL			
EXTERNAL INTERRUPT ENABLE	XIE	680A	1→XIE
EXTERNAL INTERRUPT DISABLE	XID	680B	0→XIE
COUNTER INTERRUPT ENABLE	CIE	680C	1→CIE
COUNTER INTERRUPT DISABLE	CID	680D	0→CIE
RETURN	RET	70	M(R(X))→X,P; R(X)+1→R(X);1→IE
DISABLE	DIS	71	M(R(X))→X,P; R(X)+1→R(X);0→IE
SAVE	SAV	78	T→M(R(X))
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS;R(X)+1→R(X);N LINES=1
OUTPUT 2	OUT 2	62	M(R(X))→BUS;R(X)+1→R(X);N LINES=2
OUTPUT 3	OUT 3	63	M(R(X))→BUS;R(X)+1→R(X);N LINES=3
OUTPUT 4	OUT 4	64	M(R(X))→BUS;R(X)+1→R(X);N LINES=4
OUTPUT 5	OUT 5	65	M(R(X))→BUS;R(X)+1→R(X);N LINES=5
OUTPUT 6	OUT 6	66	M(R(X))→BUS;R(X)+1→R(X);N LINES=6
OUTPUT 7	OUT 7	67	M(R(X))→BUS;R(X)+1→R(X);N LINES=7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7
CALL AND RETURN			
STANDARD CALL	SCAL	688N	R(N).0→M(R(X)); R(N).1→M(R(X)–1); R(X)–2→R(X); R(P)→ R(N); THEN M(R(N))→ R(P).1; M(R(N)+1)→R(P).0; R(N)+2→R(N)
STANDARD RETURN	SRET	689N	R(N)→R(P); M(R(X)+1) →R(N).1; M(R(X)+2)→ R(N).0; R(X)+2→R(X)

CDP1804, CDP1804C Types

1. Long-Branch, Long-Skip and No Op instructions require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:

   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch (NLBR).

2. The short-branch instructions are two or three bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address, except for the branches on interrupt. For those, the first two bytes specify the condition to be tested and the third byte specifies the branching address.

   The short-branch instruction can:

   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch
   g) Test for interrupts

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch within the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch (NBR).

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:

   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

4. Instructions 6800 through 680D, 683E, and 683F take 3 machine cycles; 68BN takes 4 machine cycles; 686N, 68AN, and 68CN take 5 machine cycles; 688N takes 10 machine cycles; and 689N takes 8 machine cycles. In all cases, the first two cycles are fetches and subsequent cycles are executes. The first byte (68) of these two byte op codes is used to generate the second fetch, the second byte is then interpreted differently than the same code without the 68 prefix. DMA and INT requests are **not** serviced until the end of the last execute cycle.

CDP1804, CDP1804C Types

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus)

8-bit bi-directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Lines)

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the $\overline{MRD}$ signal.

$\overline{MRD} = V_{DD}$: Data from I/O to CPU and Memory

$\overline{MRD} = V_{SS}$: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

$\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$ (3 I/O Requests)

These inputs are sampled by the CDP1804 during the interval in the middle of TPB.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines)

These outputs indicate that the CPU is: 1 fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. $H = V_{DD}$, $L = V_{SS}$.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address.

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines, 1/2 cycle after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

CDP1804, CDP1804C Types

$\overline{MWR}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{MRD}$ (Read Level)

A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does **not** have a three-state high-impedance output, $\overline{MRD}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. A typical clock frequency is 4 MHz at V_{DD} = 5 volts.

The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{XTAL}$

Connection to be used with clock input terminal, for an external crystal, or RC network if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{XTAL}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information on crystal oscillators, see ICAN-6565. A typical RC oscillator is shown in Fig. 4. The frequency is approximately $0.25/RC$.

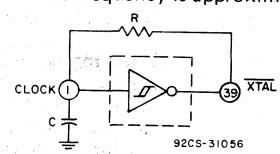


Fig. 4 – RC network for oscillator

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Test
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Test

Disables internal ROM and RAM, so that all memory references are to external memory. This mode is equivalent to the RUN mode in all other respects.

Reset

Registers I, N, Q, and prescaler are reset. IE, XIE, and CIE are set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset-run can be realized by connecting an RC network to $\overline{CLEAR}$.

CDP1804, CDP1804C Types

Pause

Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 5).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition, while if paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 5). When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

$\overline{EMS}$

This signal line is used for external memory expansion. It is low when external memory is being addressed and high at all other times. It is initiated 1.5 clock periods after TPA (at which time all addresses are stable) and terminates at the end of the cycle. Use of $\overline{EMS}$ for memory selection allows 3.5 clock cycles for data access.

V_{DD}, V_{SS}

V_{SS} is the most negative supply voltage terminal and is normally connected to ground. V_{DD} is the positive supply voltage terminal. All outputs swing from V_{SS} to V_{DD}. The recommended input voltage swing is from V_{SS} to V_{DD}.

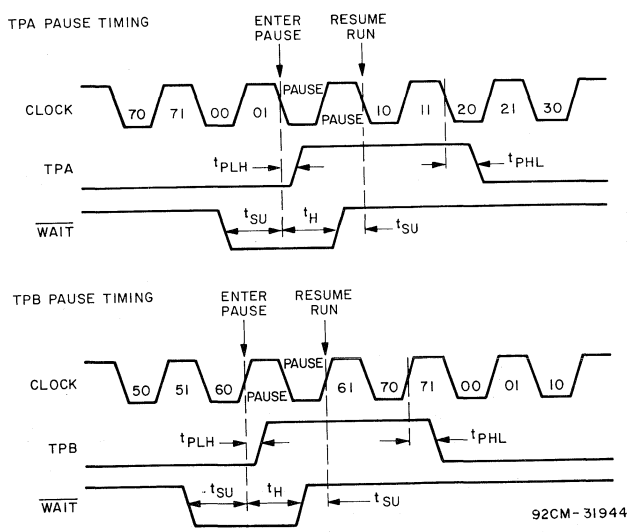


Fig. 5 — Pause mode timing diagrams.

CDP1804, CDP1804C Types

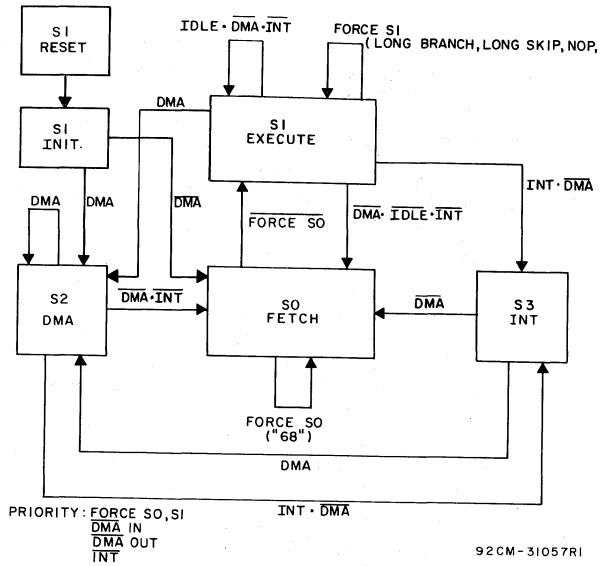


Fig. 6 – State transition diagram.

STATE TRANSITIONS

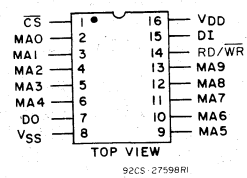
The CDP1804 state transitions are shown in Fig. 6. Each machine cycle requires the same period of time, 8 clock pulses, except the initialization cycle (INIT) which requires 9 clock pulses. The execution of an instruction requires either 2 or 3 machine cycles. S2 is the response to a DMA request and S3 is the interrupt response.

CDP1821, CDP1821C Types

1024-Word x 1-Bit Static Random-Access Memory

Features:

- **Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible**
- **Compatible with CDP1800—series microprocessors at maximum speed**
- **Fast access time:**
  125 ns typ. at V_{DD} = 5 V; typical;
  75 ns typ. at V_{DD} = 10 V typical
- **Single voltage supply**
- **No precharge or external clocks required**
- **Low quiescent and operating power**
- **Separate data inputs and outputs**



The RCA-CDP1821 and CDP1821C are 1024-word x 1-bit COS/MOS silicon-on-sapphire (SOS), fully static, random-access memories for use in CDP1800 microprocessor systems.

The output state of the CDP1821 and CDP1821C is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore, the chip-select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$=1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The CDP1821 and CDP1821C are functionally identical. They differ in that the CDP1821 has a recommended operating voltage range of 4-10.5 volts, and the CDP1821C, a recommended operating voltage range of 4-6.5 volts.

The CDP1821 and CDP1821C types are supplied in a 16-lead hermetic dual-in-line side-brazed ceramic package (D Suffix) and in a 16-lead dual-in-line plastic package (E Suffix).

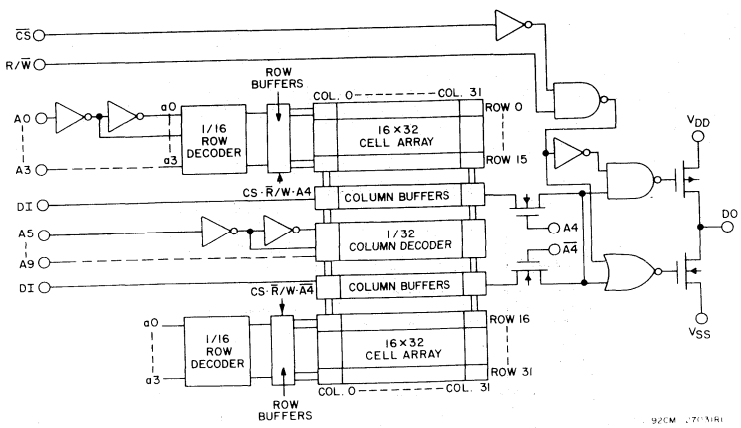


Fig. 1 — Functional block diagram.

CDP1821, CDP1821C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal)
CDP1821 . . . . . −0.5 to +11 V
CDP1821C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D). . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D. . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1821		CDP1821C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/ WRITE R/W	CHIP-SELECT CS	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	0	High Impedance
Read	1	0	Contents of Addressed Cell

X = DON'T CARE

LOGIC 1 ≅ HIGH
LOGIC 0 ≡ LOW

CDP1821, CDP1821C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, Except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1821			CDP1821C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	–	0,5	5	–	50	500	–	50	500	μA
	–	0,10	10	–	500	1000	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	2	4	–	2	4	–	mA
	0.5	0,10	10	4	8	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1	−2	–	−1	−2	–	mA
	9.5	0,10	10	−2	−4	–	–	–	–	
Output Voltage Low-Level V_{OL}▲	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage HighLevel, V_{OH}▲	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Current, I_{IN}	–	0,5	5	–	–	±5	–	–	±5	μA
	–	0,10	10	–	–	±10	–	–		
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	–	±5	–	–	±5	μA
	0,10	0,10	10	–	–	±10	–	–	–	
Operating Current, I_{DD1}#	–	0,5	5	–	2	4	–	2	4	mA
	–	0,10	10	–	4	8	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	–	–	

* Typical values are for T_A = 25°C.

▲ I_{OL} = I_{OH} = 1 μA.

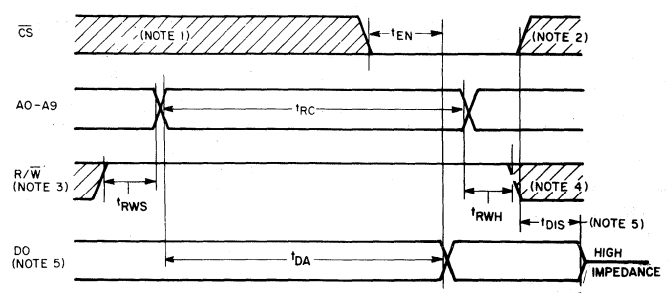
Operating current is measured at 2 MHz with open outputs.

CDP1821, CDP1821C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%
t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1821			CDP1821C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle								
Data Access t_{DA}	5	–	125	250	–	125	250	ns
	10	–	75	125	–	–	–	
Read Cycle t_{RC}	5	250	–	–	250	–	–	
	10	125	–	–	–	–	–	
Output Enable t_{EN}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Output Disable t_{DIS}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Read/$\overline{\text{Write}}$ Setup Time t_{RWS}	5	75	–	–	75	–	–	
	10	50	–	–	–	–	–	
Read/$\overline{\text{Write}}$ Hold Time t_{RWH}	5	75	–	–	75	–	–	
	10	50	–	–	–	–	–	

*Typical values are for T_A = 25°C and nominal voltages.
†Time required by a limit device to allow for the indicated function.



Note 1 Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.

Note 2 Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.

Note 3 Read/Write (R/$\overline{W}$) must be at a high level during all address transitions.

Note 4 Don't care.

Note 5 Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/W or the rising edge of $\overline{CS}$.

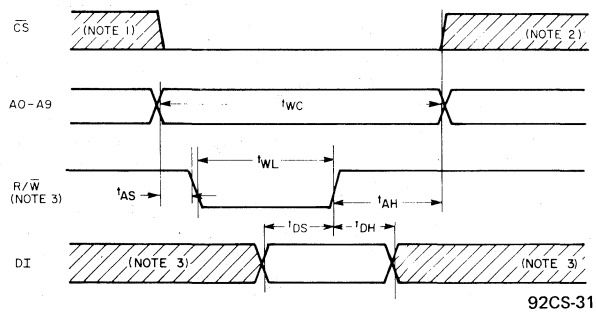
Fig. 2 – Read-cycle timing diagram.

CDP1821, CDP1821C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%
t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1821			CDP1821C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle								
Write Cycle t_{WC}	5	275	–	–	275	–	–	ns
	10	175	–	–	–	–	–	
Address Setup Time t_{AS}	5	75	–	–	75	–	–	
	10	50	–	–	–	–	–	
Address Hold Time t_{AH}	5	75	–	–	75	–	–	
	10	50	–	–	–	–	–	
Input Data Setup Time t_{DS}	5	100	–	–	100	–	–	
	10	75	–	–	–	–	–	
Input Data Hold Time t_{DH}	5	75	–	–	75	–	–	
	10	50	–	–	–	–	–	
Read/$\overline{\text{Write}}$ Pulse Width Low t_{WL}	5	125	–	–	125	–	–	
	10	75	–	–	–	–	–	

*Typical values are for T_A = 25°C and nominal voltages.
†Time required by a limit device to allow for the indicated function.



Note 1 Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.

Note 2 Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.

Note 3 Don't care.

Fig. 3 – Write cycle timing diagram.

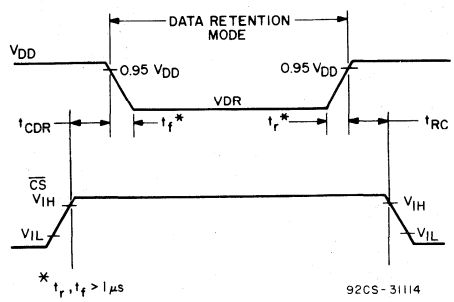


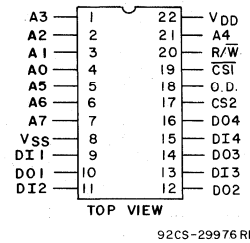
Fig. 4 – Low V_{DD} data retention waveforms and timing diagram.

CDP1822, CDP1822C Types

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Interfaces directly with CDP1802 microprocessor*
- *Very low operating current—4 mA typ. at V_{DD} = 5 V and cycle time = 1 μs*
- *Industry standard pinout*
- *Two Chip-Select inputs—simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min.*
- *Single-power-supply operation— 4 to 6.5 V for CDP1822C and 4 to 10.5 V for CDP1822*
- *High noise immunity—30% of V_{DD} over the range 5 to 10.5 V*
- *TTL compatible CDP1822C*
  - *— Drives one TTL load*
  - *— Accepts TTL level inputs using pull-up resistor*
- *Output-Disable for common I/O systems*
- *3-State data output for bus-oriented systems*
- *Separate data inputs and outputs*



CDP1822, CDP1822C TERMINAL ASSIGNMENTS

RCA Type No.	T_A = −40 to +85°C	Max. Access Time — ns
CDP1822D CDP1822E	V_{DD} = 10 V	250 250
CDP1822CD CDP1822CE	V_{DD} = 5V	450 450

The RCA-CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4 to 6.5 volts for the CDP1822C and 4 to 10.5 volts for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

The CDP1822 and CDP1822C types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(ALL VOLTAGES REFERENCED TO V_{SS} TERMINAL)
CDP1822 ..... −0.5 TO +11V
CDP1822C ..... −0.5 TO +7V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGE (D SUFFIX TYPES) ..... −55 TO +125 °C
PLASTIC PACKAGE (E SUFFIX TYPES) ..... −40 TO +85 °C
STORAGE-TEMPERATURE RANGE (T_{STG}) ..... −65 TO +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 S MAX. ..... +265 °C

CDP1822, CDP1822C Types

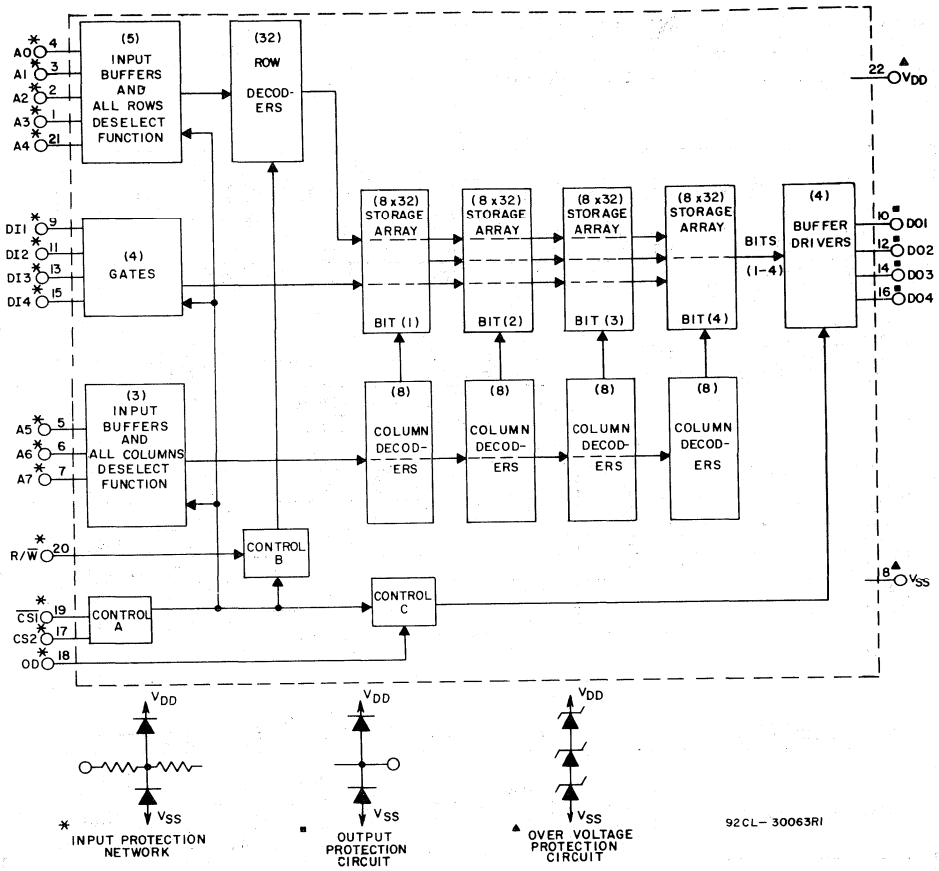


Fig. 1 — Functional block diagram for CDP1822 and CDP1822C.

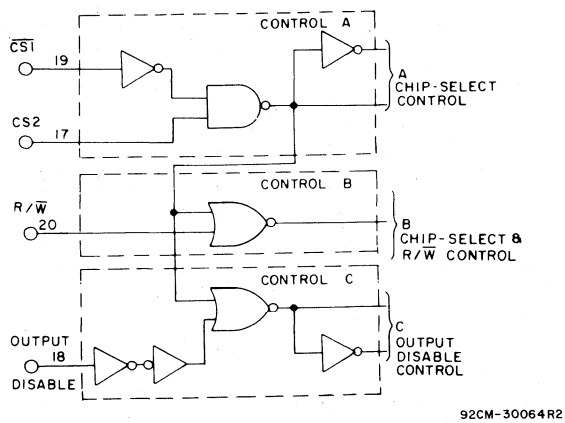


Fig. 2 — Logic diagram of controls for CDP1822 and CDP1822C.

CDP1822, CDP1822C Types

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1822		CDP1822C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	$\overline{\text{Read/Write}}$ $R/\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5%

CHARACTERISTICS	TEST CONDITIONS			LIMITS						Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1822			CDP1822C			
				Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	—	500	—	—	500	μA
	—	0,10	10	—	—	1000	—	—	—	
Output Voltage:	—	0,5	5	—	0	0.1	—	0	0.1	V
Low-Level, V_{OL}	—	0,10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink) Current, I_{OL}	0.4	0,5	5	2	4	—	2	4	—	mA
	0.5	0,10	10	4.5	9	—	—	—	—	
Output High (Source) Current, I_{OH}	4.6	0,5	5	−1	−2	—	−1	−2	—	
	9.5	0,10	10	−2.2	−4.4	—	—	—	—	
Input Current, I_{IN}	—	0,5	5	—	—	±5	—	—	±5	μA
	—	0,10	10	—	—	±10	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	—	±5	—	—	±5	
	0,10	0,10	10	—	—	±10	—	—	—	
Operating Current, I_{DD1}#	—	0,5	5	—	4	8	—	4	8	mA
	—	0,10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	5	7.5	—	5	7.5	

#Outputs open circuited; cycle time = 1 μs.

•Typical values are for T_A = 25°C and nominal voltage.

CDP1822, CDP1822C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF and 1 TTL Load; See Figs. 4 and 5.

CHARACTERISTIC		V_{DD}	CDP1822			CDP1822C			UNITS
		(V)	Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	
Read Cycle Times									
Read Cycle	t_{RC}	5	450	—	—	450	—	—	ns
		10	250	—	—	—	—	—	
Access from Address	t_{ADA}	5	—	250	450	—	250	450	ns
		10	—	150	250	—	—	—	
Output Valid from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	5	—	250	450	—	250	450	ns
		10	—	150	250	—	—	—	
Output Valid from Chip-Select 2	t_{DOA2}	5	—	250	450	—	250	450	ns
		10	—	150	250	—	—	—	
Output Active from Output Disable	t_{DOA3}	5	—	—	200	—	—	200	ns
		10	—	—	110	—	—	—	
Output Hold from $\overline{\text{Chip-Select 1}}$	t_{DOH1}	5	20	—	—	20	—	—	ns
		10	20	—	—	—	—	—	
Output Hold from Chip-Select 2	t_{DOH2}	5	20	—	—	20	—	—	ns
		10	20	—	—	—	—	—	
Output Hold from Output Disable	t_{DOH3}	5	20	—	—	20	—	—	ns
		10	20	—	—	—	—	—	
Write Cycle Times									
Write Cycle	t_{WC}	5	500	—	—	500	—	—	ns
		10	300	—	—	—	—	—	
Address Setup	t_{AS}	5	200	—	—	200	—	—	ns
		10	110	—	—	—	—	—	
Write Recovery	t_{WR}	5	50	—	—	50	—	—	ns
		10	40	—	—	—	—	—	
Write Width	t_{WRW}	5	250	—	—	250	—	—	ns
		10	150	—	—	—	—	—	
Data In Width Effective	t_{DIW}	5	250	—	—	250	—	—	ns
		10	150	—	—	—	—	—	
Data In Hold	t_{DIH}	5	50	—	—	50	—	—	ns
		10	40	—	—	—	—	—	
$\overline{\text{Chip-Select 1}}$ Setup	t_{CSS1}	5	450	—	—	450	—	—	ns
		10	260	—	—	—	—	—	
Chip-Select 2 Setup	$t_{\overline{CS}S2}$	5	450	—	—	450	—	—	ns
		10	260	—	—	—	—	—	
Output Disable Setup	t_{ODS}	5	200	—	—	200	—	—	ns
		10	110	—	—	—	—	—	

#Time required by a limit device to allow for the indicated function.

• Typical values are for T_A = 25°C and nominal V_{DD}.

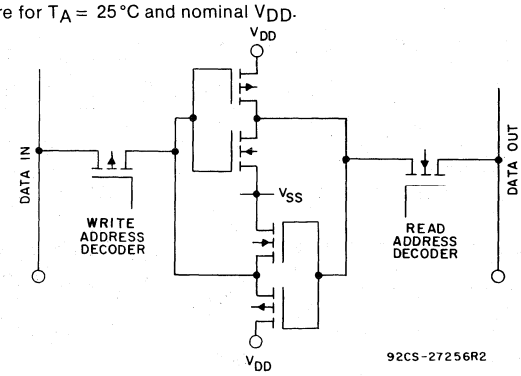


Fig. 3 — Memory cell configuration.

CDP1822, CDP1822C Types

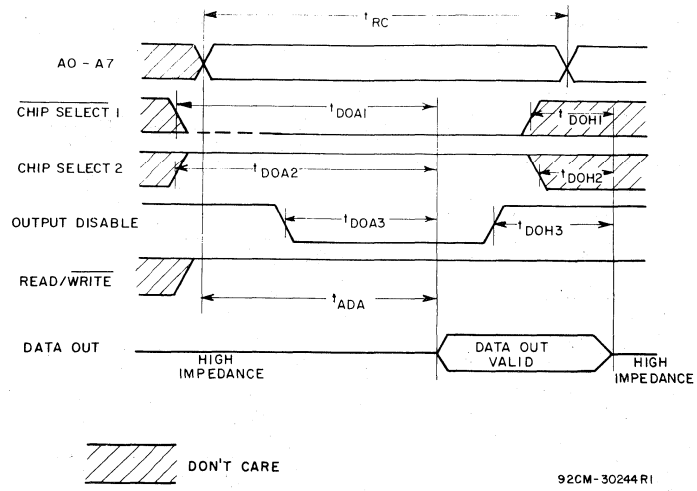
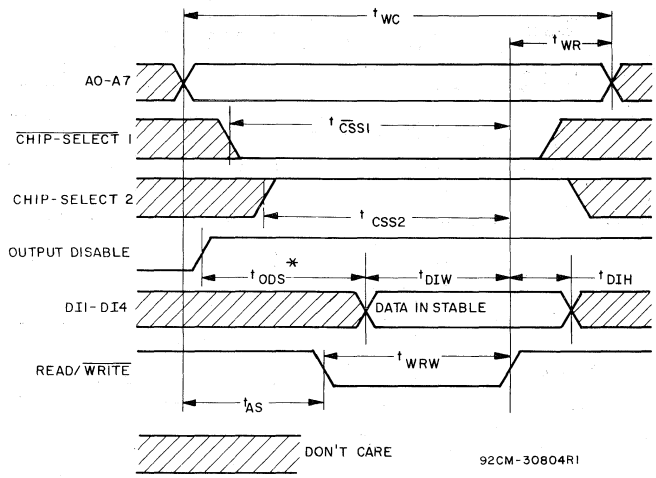


Fig. 4 — Read cycle waveforms and timing diagram.



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY; FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE.

Fig. 5 — Write cycle waveforms and timing diagram.

DATA RETENTION CHARACTERISTICS at $T_A = -40$ to $+85$ °C; see Fig. 6.

CHARACTERISTIC	TEST CONDITIONS		CDP1822			CDP1822C			UNITS
	V_{DR} (V)	V_{DD} (V)	Min.	Typ. ●	Max.	Min.	Typ. ●	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	

● Typical values are for $T_A = 25$ °C and nominal V_{DD}.

CDP1822, CDP1822C Types

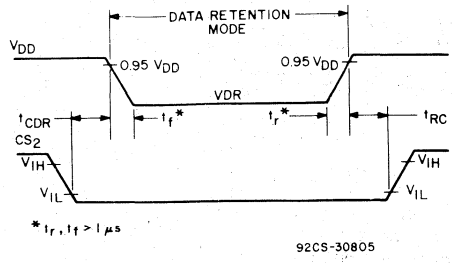
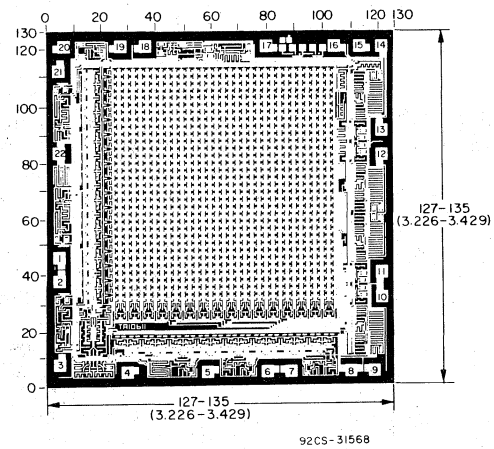


Fig. 6 — Low V_{DD} data retention waveforms and timing diagram.



The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10 − 3 inch).

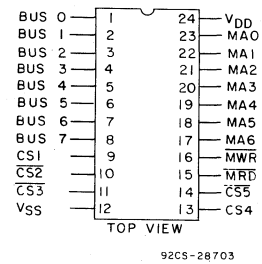
Dimensions and pad layout for CDP1822H.

CDP1823, CDP1823C Types

128-Word x 8-Bit Static Random-Access Memory

Features:

- *Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible*
- *Compatible with CDP1800-series microprocessors at maximum speed*
- *Interfaces with CDP1802 and CDP1804 microprocessors without additional components*
- *Fast access time:*
  275 ns typ. at $V_{DD} = 5$ V;
  140 ns typ. at $V_{DD} = 10$ V
- *Single voltage supply*
- *Common data inputs and outputs*
- *Multiple-chip select inputs to simplify memory system expansion*



TERMINAL ASSIGNMENT

The RCA-CDP1823 and CDP1823C are 128-word x 8-bit COS/MOS SOS static random-access memories. These memories are compatible with the CDP1802 and CDP1804 microprocessors, and will interface directly without additional components. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1823C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

The CDP1823 and CDP1823C are supplied in hermetic 24-lead dual-in-line ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

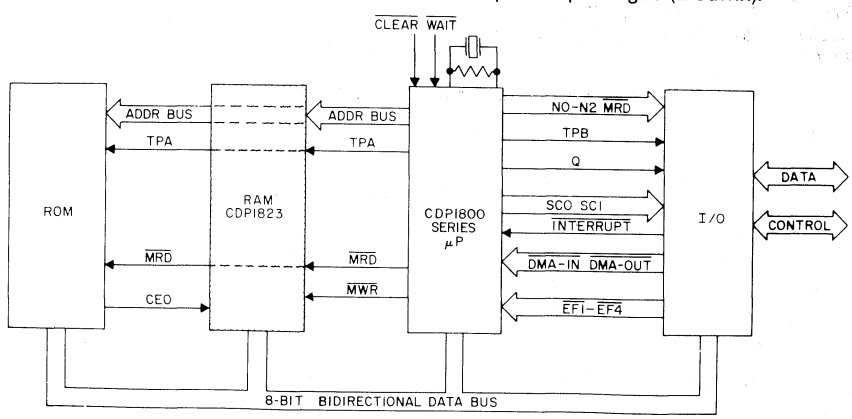


Fig. 1 — Typical CDP1802 microprocessor system.

92CM-28954R1

CDP1823, CDP1823C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1823 ..... −0.5 to +11 V
CDP1823C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) ..... −55 to +125 °C
PLASTIC PACKAGES (E SUFFIX TYPES) ..... −40 to +85 °C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265 °C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

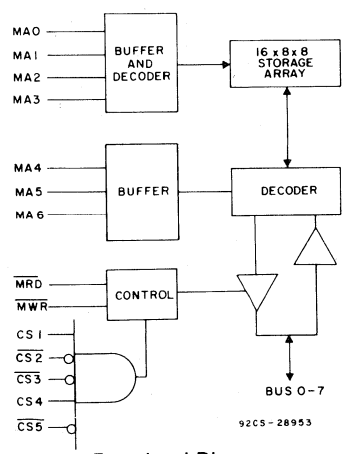
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

OPERATIONAL MODES

Function	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	Bus Terminal State
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care



Functional Diagram

CDP1823, CDP1823C Types

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, Except as Noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1823D CDP1823E			CDP1823CD CDP1823CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	—	0,5	5	—	—	500	—	—	500	µA
	—	0,10	10	—	—	1000	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	2	4	—	2	4	—	mA
	0.5	0,10	10	4.5	9	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4.6	0,5	5	−1	−2	—	−1	−2	—	mA
	9.5	0,10	10	−2.2	−4.4	—	—	—	—	
Output Voltage• Low-Level V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage• High-Level V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	—	±5	—	—	±5	µA
		0,10	10	—	—	±10	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	—	±5	—	—	±5	µA
	0,10	0,10	10	—	—	±10	—	—	—	
Operating Current, I_{DD}▲	—	0,5	5	—	4	8	—	4	8	µA
	—	0,10	10	—	8	16	—	—	—	
Data Retention Current, I_{DR}	—	—	2	—	—	50	—	—	50	µA
Min. Data Retention Voltage, V_{DR}	—	—	V_{DR}	—	—	2	—	—	2	V
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	—	—	pF

*Typical values are for $T_A = 25$ °C. •$I_{OL} = I_{OH} = 1$ µA.

▲Measured with 1 µs read cycle time and outputs floating.

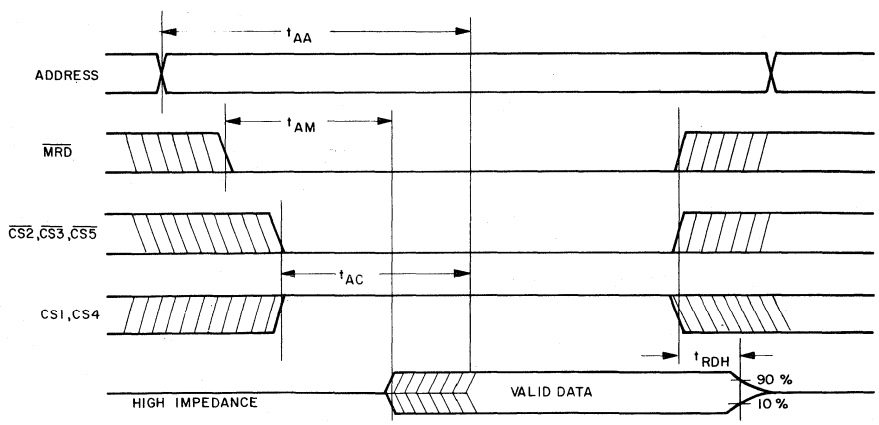
CDP1823, CDP1823C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $C_L = 100$ pF.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle (See Fig. 2)								
Access Time From Address Change, t_{AA}	5	—	275	450	—	275	450	ns
	10	—	150	250	—	—	—	
Access Time From Chip Select, t_{AC}	5	—	150	250	—	150	250	ns
	10	—	100	150	—	—	—	
$\overline{MRD}$ to Output Active, t_{AM}	5	—	150	250	—	150	250	ns
	10	—	100	150	—	—	—	
Data Hold Time After Read, t_{RDH}	5	25	50	75	25	50	75	ns
	10	15	25	40	—	—	—	
Write Cycle (See Fig. 3)								
Write Release, t_{WR}	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	
Write Cycle, t_{WC}	5	400	—	—	400	—	—	ns
	10	225	—	—	—	—	—	
Write Pulse Width, t_{WW}	5	200	—	—	200	—	—	ns
	10	100	—	—	—	—	—	
Address to CS Setup Time, $t_{\overline{ACS}}$	5	125	—	—	125	—	—	ns
	10	75	—	—	—	—	—	
Address to $\overline{MWR}$ Setup Time, $t_{\overline{AWS}}$	5	125	—	—	125	—	—	ns
	10	75	—	—	—	—	—	
Data to $\overline{MWR}$ Setup Time, t_{DSU}	5	100	—	—	100	—	—	ns
	10	75	—	—	—	—	—	
Data Hold Time From $\overline{MWR}$, t_{DH}	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	

*Typical values are at $T_A = 25$ °C and nominal voltage.

†Time required by a limit device to allow for the indicated function.



NOTE: $\overline{MWR}$ IS HIGH DURING READ OPERATION.
TIMING MEASUREMENT REFERENCE IS $0.5\,V_{DD}$.

92CM-31942

Fig. 2 — Read cycle timing diagram.

CDP1823, CDP1823C Types

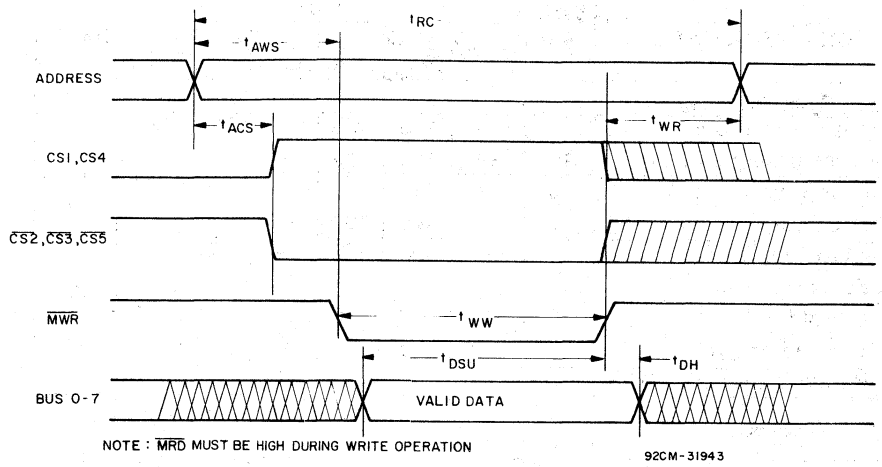
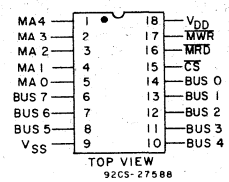


Fig. 3 — Write cycle timing diagram.

32-Word x 8-Bit Static Random-Access Memory

Features:

- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors
- Interfaces with CDP1802 microprocessor without additional components
- Fast access time:
  300 ns typ. at V_{DD} = 5 V;
  150 ns typ. at V_{DD} = 10 V (CDP1824)
- Single voltage supply
- No precharge or clock required
- Operating temperature range
  −55°C to +125°C (CDP1824D, CDP1824CD); −40°C to +85°C (CDP1824E, CDP1824CE)
- Low quiescent and operating power



Terminal Assignment

The RCA-CDP1824 and CDP1824C types are 32-word x 8-bit fully static COS/MOS random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4 to 10.5 volts, and the CDP1824C has an operating voltage range of 4 to 6.5 volts. The CDP1824 and CDP1824C types are supplied in 18-lead hermetic dual-in-line ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

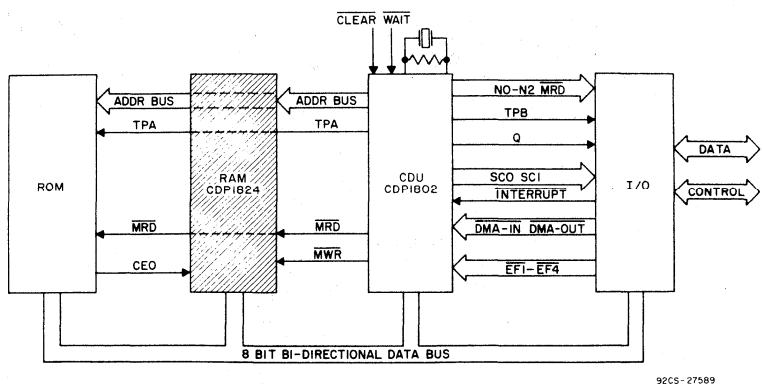


Fig. 1—Typical CDP1802 microprocessor system.

CDP1824, CDP1824C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1824 . . . . . −0.5 to +11 V
CDP1824C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) . . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS
		CDP1824D CDP1824E		CDP1824CD CDP1824CE		
	V_{DD} (V)	Min.	Max.	Min.	Max.	
Supply-Voltage Range	–	4	10.5	4	6.5	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time,▲	5	–	5	–	5	μs
t_r,t_f	10	–	2	–	–	

▲ Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

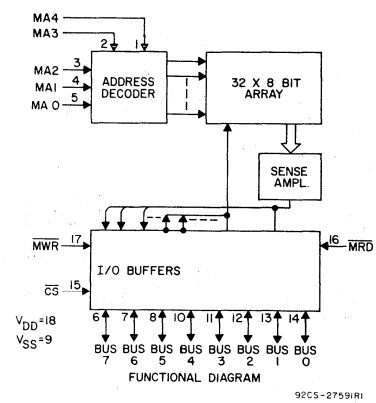


Fig. 2 – Functional diagram.

CDP1824, CDP1824C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1824D CDP1824E			CDP1824CD CDP1824CD			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	–	5	–	50	100	–	250	500	μA
	–	–	10	–	250	500	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.8	2.2	–	1.8	2.2	–	mA
	0.5	0,10	10	3.6	4.5	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−0.9	−1.1	–	−0.9	−1.1	–	mA
	9.5	0,10	10	−1.8	−2.2	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05	–	0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	±0.1	±1	–	±0.1	±1	μA
		0,10	10	–	±0.1	±1	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	±0.2	±2	–	±0.2	±2	μA
	0,10	0,10	10	–	±0.2	±2	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}.

OPERATIONAL MODES

Function	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	Data Pins Status
READ	0	0	X	Output: High/ Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

CDP1824, CDP1824C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Read Operation								
Access Time From Address Change, t_{AA}	5	–	400	710	–	400	710	ns
	10	–	200	320	–	–	–	
Access Time From Chip Select, t_{AC}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	
Output Active From $\overline{MRD}$, t_{AM}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	
Write Operation								
Write Pulse Width, t_{WW}	5	390	200	–	390	200	–	ns
	10	180	150	–	–	–	–	
Data Setup Time, t_{DS}	5	390	100	–	390	100	–	ns
	10	180	50	–	–	–	–	
Data Hold Time, t_{DH}	5	70	40	–	70	40	–	ns
	10	35	20	–	–	–	–	
Chip Select Setup Time, t_{CS}	5	425	210	–	425	210	–	ns
	10	215	110	–	–	–	–	
Address Setup Time, t_{AS}	5	640	500	–	640	500	–	ns
	10	390	300	–	–	–	–	

Time required by a limit device to allow for the indicated function.

● Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}.

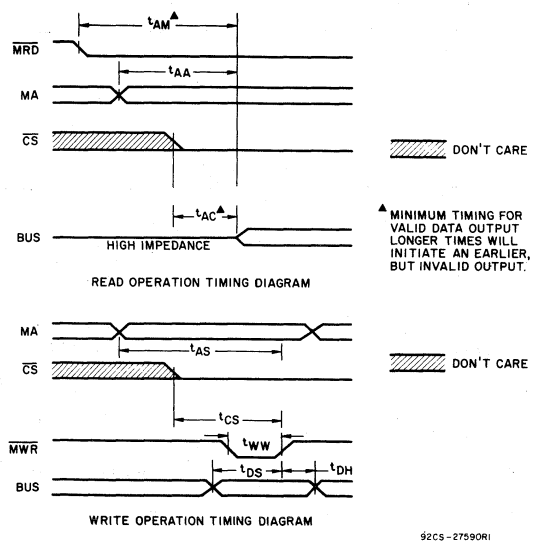


Fig. 3 – Timing diagrams.

CDP1824, CDP1824C Types

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$ } Data transfers from

$t_{\overline{DS}} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

DATA RETENTION CHARACTERISTICS at T_A = –40 to +85°C; see Fig. 4.

CHARACTERISTIC	TEST CONDITIONS		CDP1824		CDP1824C		UNITS
		V_{DD} (V)	Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}		–	2.5	–	2.5	–	V
Data Retention Quiescent Current, I_{DD}	V_{DR} = 2.5 V	–	–	50	–	250	μA
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR} = 2.5 V	5	600	–	600	–	ns
		10	300	–	–	–	
Recovery to Normal Operation Time, t_{RC}	V_{DR} = 2.5 V	5	600	–	600	–	ns
		10	300	–	–	–	

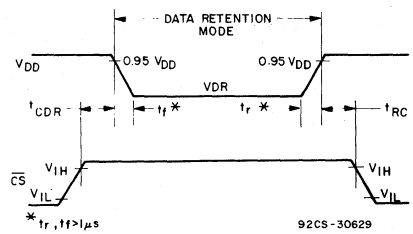


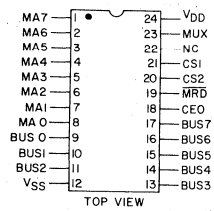
Fig. 4 – Low V_{DD} data retention waveforms and timing diagram.

CDP1831, CDP1831C Types

512-Word x 8-Bit Static Read-Only Memory

Features:

- Static Silicon-Gate CMOS circuitry – CD4000-series compatible
- Compatible with CDP1800-series microprocessors
- Interfaces with CDP1802 microprocessor without additional components
- Fast access time: 300 ns max. at V_{DD} = 10 V (CDP1831)
- Single voltage supply
- On-chip address latch
- Operating temperature range; –55°C to +125°C (CDP1831D, CDP1831CD) –40°C to +85°C (CD1831E, CDP1831CE)
- Optional programmable location within 64K memory space
- Low quiescent and operating power



Terminal Assignment

The RCA-CDP1831 and CDP1831C types are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with the CDP1802 microprocessor without additional components.

The CDP1831 and CDP1831C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store and 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word byte of 64K memory space. (See PD30, "ROM Purchase Policy and Data Programming Instructions".) Three Chip-Select signals—CS1, CS2, MRD—are also provided.

The polarity of the clock (TPA), and CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) goes "high" when the device is selected. This signal is intended for use as an output disable control for small memory systems.

The CDP1831C is functionally identical to the CDP1831. The CDP1831 has an operating voltage range of 4 to 10.5 volts, and the CDP1831C has an operating voltage range of 4 to 6.5 volts.

The CDP1831 and CDP1831C types are supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix).

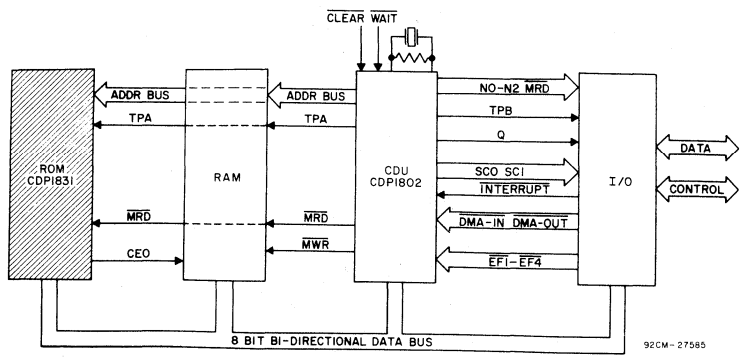


Fig. 1 – Typical CDP1802 microprocessor system.

CDP1831, CDP1831C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal
CDP1831 . . . . . −0.5 to +11 V
CDP1831C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) . . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 unch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1831D CDP1831E		CDP1831CD CDP1831CE		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

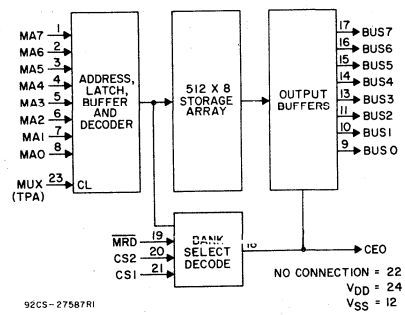


Fig. 2 – Functional diagram

CDP1831, CDP1831C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1831D CDP1831E			CDP1831CD CDP1831CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	100	–	50	500	μA
	–	–	10	–	10	500	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.8	–	–	0.8	–	–	mA
	0.5	0,10	10	1.8	–	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	–0.8	–	–	–0.8	–	–	mA
	9.5	0,10	10	–1.8	–	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05		0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	–	±1	–	–	±1	μA
		0,10	10	–	–	±1	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	–	±1	–	–	±1	μA
	0,10	0,10	10	–	–	±1	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1831 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

CDP1831, CDP1831C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1831D CDP1831E			CDP1831CD CDP1831CE			
		Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	
Access Time from Address Change, t_{AA}	5	–	850	1000	–	850	1000	ns
	10	–	350	400	–	–	–	
Access Time from Chip Select, t_{ACS}	5	–	700	800	–	700	800	ns
	10	–	250	300	–	–	–	
Chip Select Delay, t_{CS}	5	–	600	–	–	600	–	ns
	10	–	200	300	–	–	–	
Address Setup Time, t_{AS}	5	50	–	–	50	–	–	ns
	10	25	–	–	–	–	–	
Address Hold Time, t_{AH}	5	150	–	–	150	–	–	ns
	10	75	–	–	–	–	–	
Read Delay, $t_{\overline{MRD}}$	5	–	300	500	–	300	500	ns
	10	–	100	150	–	–	–	
Chip Enable Output Delay from Address, t_{CA}	5	–	500	600	–	500	600	ns
	10	–	200	250	–	–	–	
Bus Contention Delay, t_D	5	–	200	350	–	200	350	ns
	10	–	100	150	–	–	–	
MUX Pulse Width (TPA), t_{PAW}	5	200	–	–	200	–	–	ns
	10	70	–	–	–	–	–	

Time required by a limit device to allow for the indicated function.

• Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}.

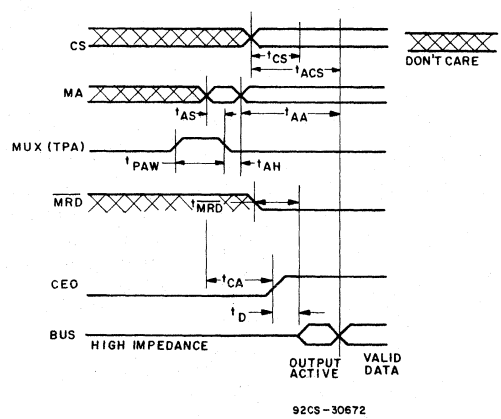
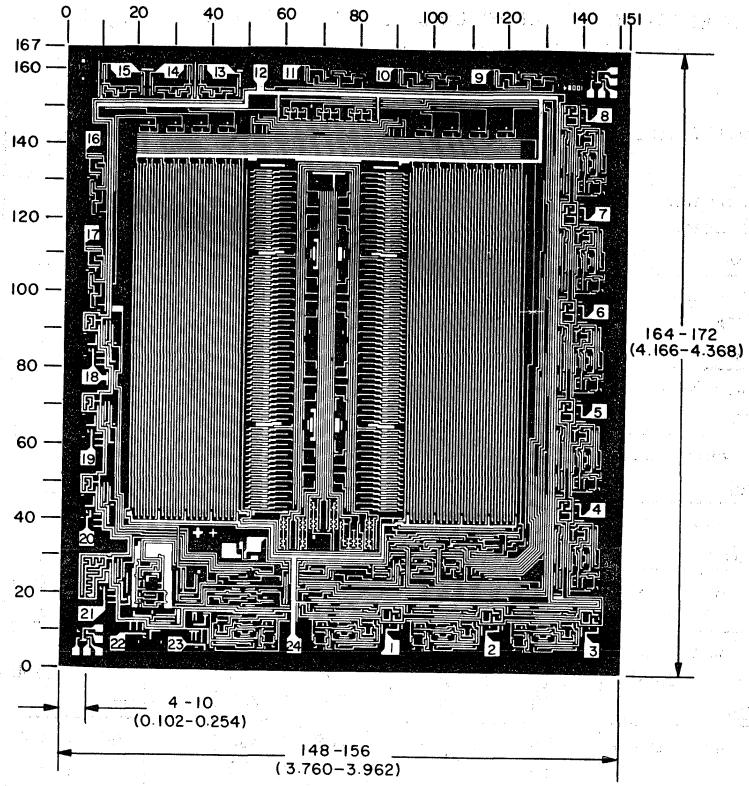


Fig. 3 – Timing diagrams.

CDP1831, CDP1831C Types



Dimensions and pad layout for CDP1831, CDP1831C chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

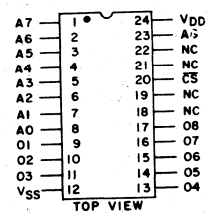
The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1832, CDP1832C Types

512-Word x 8-Bit Static Read-Only Memory

Features:

- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors
- Fast access time:
  400 ns typ. at V_{DD} = 10 V (CDP1832)
- Single voltage supply
- Operating temperature range
  −55°C to + 125°C (CDP1832D, CDP1832CD)
  −40°C to + 85°C (CDP1832E, CDP1832CE)
- Functional replacement for industry type
  8704 512 x 8 PROM
- Three-state outputs
- Low quiescent and operating power



Terminal Assignment

92CS-27579

The RCA-CDP1832 and CDP1832C types are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. (See PD30, "ROM Purchase Policy and Data Programming Instructions").

The CDP1832 ROM's are completely static—no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$ = 0.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704/8704 Reprogrammable Read-Only Memories.

The CDP1832C is functionally identical to the CDP1832. The CDP1832 has a operating voltage range of 4 to 10.5 volts, and the CDP1832C has a operating voltage range of 4 to 6.5 volts.

The CDP1832 and CDP1832C are supplied in 24-lead, hermetic, dual-in-line ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix).

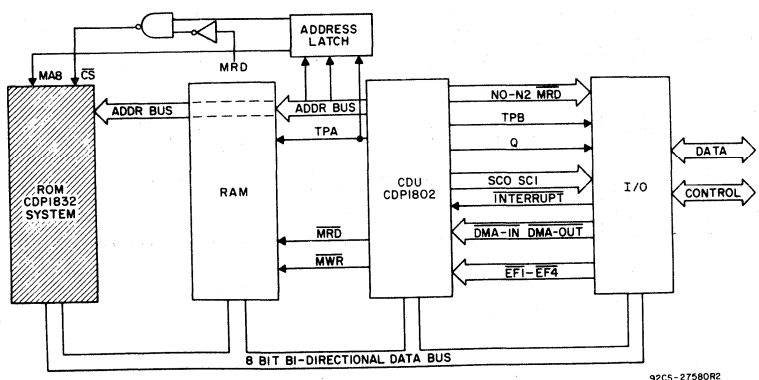


Fig. 1 — Typical CDP1802 microprocessor system.

CDP1832, CDP1832C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal
CDP1832 . . . . . −0.5 to +11 V
CDP1832C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES). . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1832D CDP1832E		CDP1832CD CDP1832CE		
	Min.	Max.	Min.	Max.	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1832D CDP1832E			CDP1832CD CDP1832CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	–	–	5	–	1	100	–	1	500	μA
	–	–	10	–	10	500	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	–	5	0.8	–	–	0.8	–	–	mA
	0.5	–	10	1.8	–	–	–	–	–	
Output High Drive (Source) Current I_{OH}	4.5	–	5	0.8	–	–	0.8	–	–	
	9.5	–	10	1.8	–	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	–	5	–	0	0.05	–	0	0.05	V
	–	–	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	–	5	4.95	5	–	4.95	5	–	
	–	–	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	–	–	5	–	–	1.5	–	–	1.5	
	–	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	–	–	5	3.5	–	–	3.5	–	–	
	–	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	–	–	10	–	–	±1	–	–	±1	μA
3-State Output Leakage Current I_{OUT}	–	–	10	–	–	±1	–	–	±1	

* Typical values are for T_A = 25°C and nominal V_{DD}.

CDP1832, CDP1832C Types

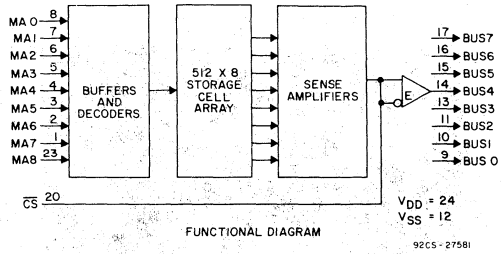


Fig. 2 – Functional diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1832D CDP1832E			CDP1832CD CDP1832CE			
		Min.	Typ.●	Max.	Min.	Typ.●	Max.	
Access Time From Address Address Change, t_{AA}	5	–	850	1000	–	850	1000	ns
	10	–	400	500	–	–	–	
Access Time From Chip Select, t_{ACS}	5	–	400	550	–	400	550	
	10	–	200	250	–	–	–	
Chip Select Delay, t_{CS}	5	–	200	250	–	200	250	
	10	–	100	130	–	–	–	

● Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}.

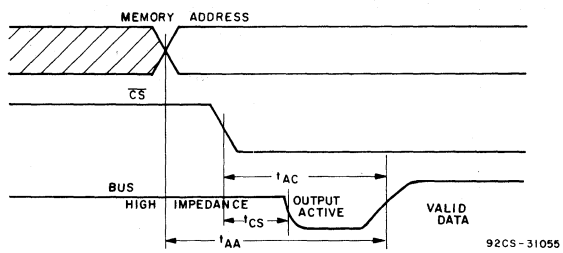
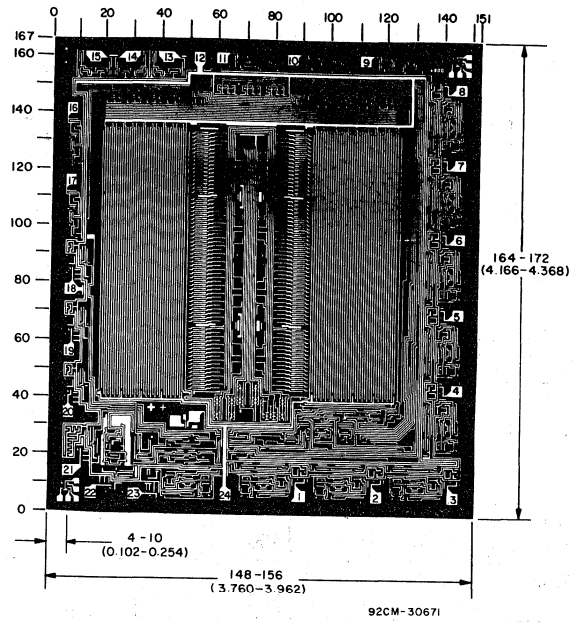


Fig. 3 – Timing diagrams.

CDP1832, CDP1832C Types



Dimensions and pad layout for CDP1832 and CDP1832C chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

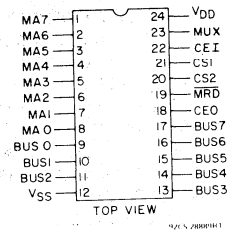
The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1833, CDP1833C Types

1024-Word x 8-Bit Static Read-Only Memory

Features:

- Compatible with CDP1800-series microprocessors
- Static CMOS circuitry—CD4000-series compatible
- Interfaces with CDP1802 and CDP1804 microprocessors without additional components
- Fast access time: 350 ns typ. at V_{DD}=10 V
- Single voltage supply
- On-chip address latch
- 3-state outputs
- Operating temperature range—−55 to +125°C (CDP1833D, CDP1833CD) −40 to +85°C (CDP1833E, CDP1833CE)
- Low quiescent and operating power



Terminal Assignment

The RCA-CDP1833 and CDP1833C are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024-words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with the CDP1802 and CDP1804 microprocessors without additional components.

The CDP1833 and CDP1833C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits on the 16-bit address. By mask option, this ROM can be programmed to operate in any 1024-word byte of 64K memory space. (See PD30, "ROM Purchase Policy and Data Programming Instructions".) Two Chip-Select inputs are also provided.

The polarity of MUX(TPA), CEI, CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) is "high" with coincidence of Address CS1, CS2 and CEI. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM chips in a microprocessor system without additional components.

The CDP1833C is functionally identical to the CDP1833. The CDP1833 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1833C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1833 and CDP1833C are supplied in 24-lead hermetic dual-in-line side-brazed ceramic package (D suffix) and 24-lead dual-in-line plastic package (E suffix).

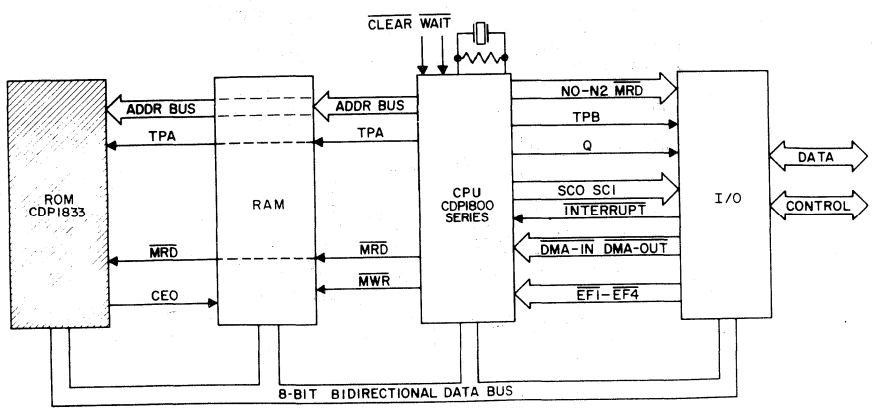


Fig. 1 — Typical CDP1800 Series microprocessor system.

CDP1833, CDP1833C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal)

CDP1833	−0.5 to +11 V
CDP1833C	−0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPE D	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1833		CDP1833C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

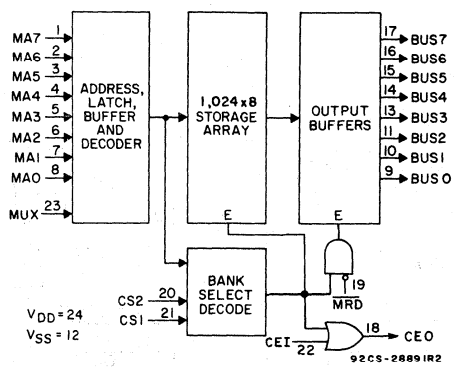


Fig. 2 – Functional diagram.

CDP1833, CDP1833C Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1833D CDP1833E			CDP1833CD CDP1833CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	5	5	–	0.01	50	–	0.02	200	μA
	–	10	10	–	1	200	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.8	–	–	0.8	–	–	mA
	0.5	0,10	10	1.8	–	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	–0.8	–	–	–0.8	–	–	mA
	9.5	0,10	10	–1.8	–	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05		0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	$\pm10^{-4}$	±1	–	$\pm10^{-4}$	±1	μA
		0,10	10	–	$\pm10^{-4}$	±2	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	$\pm10^{-4}$	±1	–	$\pm10^{-4}$	±1	μA
	0,10	0,10	10	–	$\pm10^{-4}$	±2	–	–	–	

*Typical values are for T_A = 25°C and nominal V_{DD}.

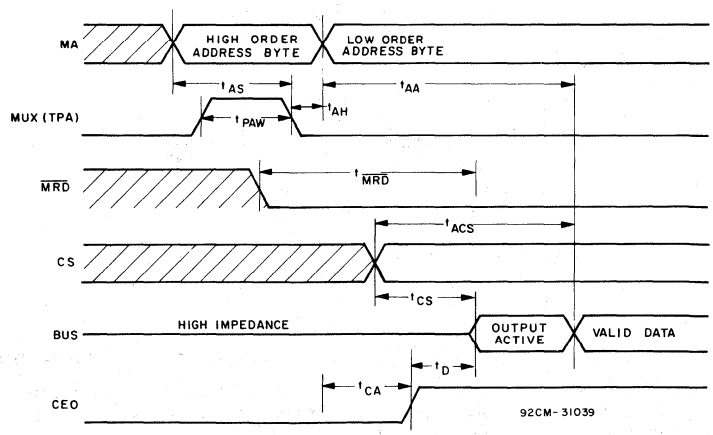


Fig. 3 – Timing diagram.

CDP1833, CDP1833C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1833			CDP1833C			
		Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	
Access Time from Address Change, t_{AA}	5	–	650	775	–	650	775	ns
	10	–	350	425	–	–	–	
Access Time from Chip Select, t_{ACS}	5	–	500	625	–	500	625	ns
	10	–	275	310	–	–	–	
Chip Select Delay, t_{CS}	5	–	250	320	–	250	320	ns
	10	–	125	180	–	–	–	
Address Setup Time, t_{AS}	5	75	50	–	75	50	–	ns
	10	40	25	–	–	–	–	
Address Hold Time, t_{AH}	5	100	75	–	100	75	–	ns
	10	50	30	–	–	–	–	
Read Delay, $t_{\overline{MRD}}$	5	–	400	500	–	400	500	ns
	10	–	200	275	–	–	–	
Chip Enable Output Delay from Address, t_{CA}	5	–	120	170	–	120	170	ns
	10	–	70	100	–	–	–	
Bus Contention Delay, t_D	5	–	220	270	–	220	270	ns
	10	–	130	150	–	–	–	
MUX Pulse Width (TPA), t_{PAW}	5	200	–	–	200	–	–	ns
	10	70	–	–	–	–	–	
Dynamic Power Dissipation P_D (cycle time = 2.5 μs)	5	–	30	–	–	30	–	ns
	10	–	120	–	–	–	–	

#Time required by a limit device to allow for the indicated function.

•Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal voltages.

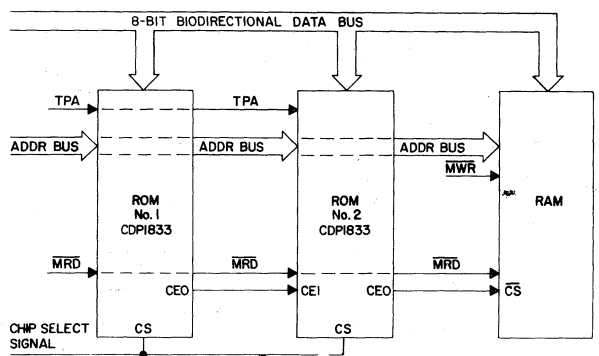
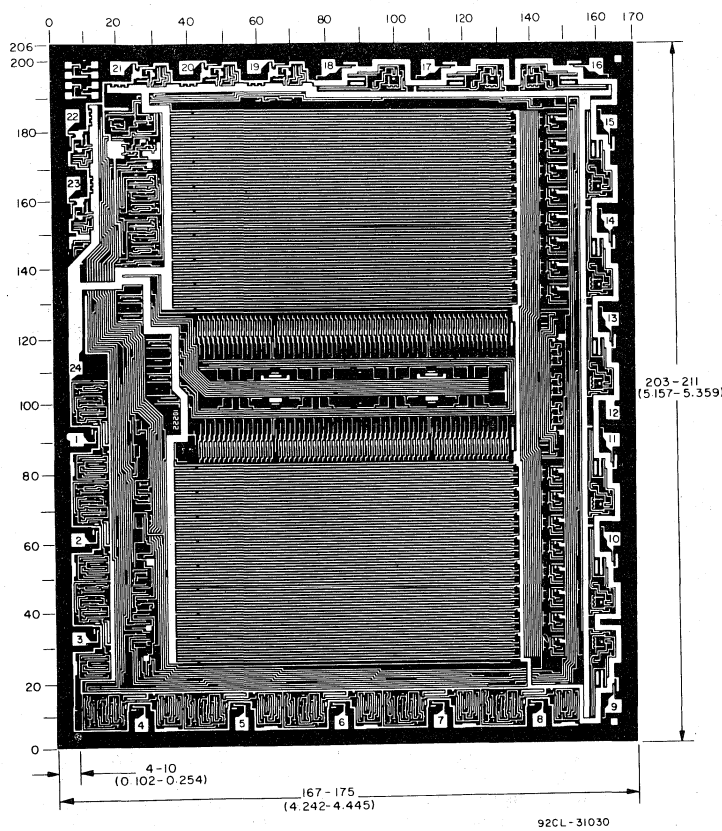


Fig. 4 – Daisy chaining CDP1833's.

92CS-31973

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM #1 was masked-programmed for memory locations 000-03FF$_{16}$ and ROM #2 masked-programmed for memory locations 0400$_{16}$-07FF$_{16}$, for addresses from 0000-07FF$_{16}$ the RAM would be disabled and the ROM enabled. For locations above 07FF$_{16}$ the ROM's would be disabled and the RAM enabled.

CDP1833, CDP1833C Types



Dimensions and pad layout for CDP1833 chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1833. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1833 is used with the CDP1802 or CDP1804 microprocessor.

$t_{AH} = 0.5\ t_C$
$t_{PAW} = 1.0\ t_C$
MRD occurs one clock period (t_C) earlier then the adress bits MA0-MA7.

where $t_C = \frac{1}{\text{CPU clock frequency}}$

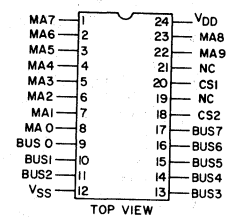
The CDP1833 is capable of operating at the maximum clock frequency of the CDP1802 or CDP1804 microprocessor.

CDP1834, CDP1834C Types

1024-Word x 8-Bit Static Read-Only Memory

Features:

- Compatible with CDP1800-series microprocessors
- Static CMOS circuitry – CD4000-series compatible
- Interfaces with CDP1802 microprocessor without additional components
- Fast access time: 350 ns typ. at V_{DD} = 10V
- Single voltage supply
- On-chip address latch
- Operating temperature range —— –55 to +125°C (CDP1834D, CDP1834CD) –40 to +85°C (CDP1834E, CDP1834CE)
- Low quiescent and operating power
- 3-state outputs



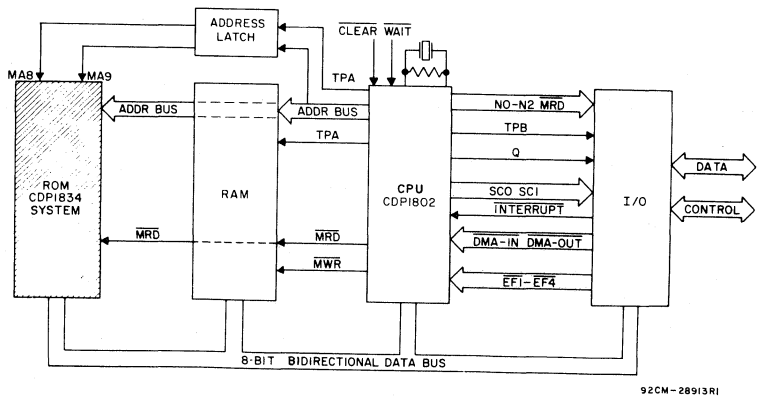
NC = NO CONNECTION

92CS-28727

Terminal Assignment

The RCA-CDP1834 and CDP1834C are static 8192-bit mask-programmable COS/MOS read-only memories organized as 1024-words x 8-bits and designed for use in CDP1800-series microprocessor systems. The CDP1834-series ROM's are completely static; no clocks are required.

Two Chip-Select inputs (CS1, CS2) are provided for memory expansion. The polarity of each Chip-Select is user mask-programmable. (See PD30, "ROM Purchase Policy and Data Programming Instructions".) The CDP1834-series is pin-compatible with industry types 2308 ROM and 2708 EPROM. The CDP1834C is functionally identical to the CDP1834. The CDP1834 has a recommended operating voltage range of 4 to 10.5 volts and the CDP1834C has a recommended operating voltage range of 4 to 6.5 volts. The CDP1834 and CDP1834C are supplied in 24-lead dual-in-line ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix).



92CM-28913R1

Fig. 1 – Typical CDP1802 microprocessor system.

CDP1834, CDP1834C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal
CDP1834 . . . . . −0.5 to +11 V
CDP1834C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) . . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1834D CDP1834E		CDP1834CD CDP1834CE		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1834D CDP1834E			CDP1834CD CDP1834CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	100	–	1	500	μA
	–	–	10	–	10	500	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.8	–	–	0.8	–	–	mA
	0.5	0,10	10	1.8	–	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	−0.8	–	–	−0.8	–	–	mA
	9.5	0,10	10	−1.8	–	–	–	–	–	
Output Voltage Low-Level V_{OL}	–	0,5	5	–	0	0.05		0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	–	±1	–	–	±1	μA
		0,10	10	–	–	±1	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	–	±1	–	–	±1	μA
	0,10	0,10	10	–	–	±1	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}.

CDP1834, CDP1834C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1834D CDP1834E			CDP1834CD CDP1834CE			
		Min.	Typ.●	Max.	Min.	Typ.●	Max.	
Access Time from Address Change, t_{AA}	5	–	575	750	–	575	750	ns
	10	–	350	425	–	–	–	
Access Time from Chip-Select t_{ACS}	5	–	600	700	–	600	700	ns
	10	–	325	410	–	–	–	
Chip-Select Delay, t_{CS}	5	–	480	580	–	480	580	ns
	10	–	250	340	–	–	–	

● Typical values are for T_A = 25°C and nominal V_{DD}.

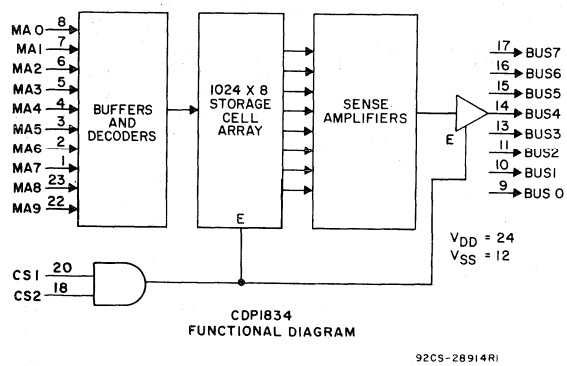


Fig. 2 – Functional diagram.

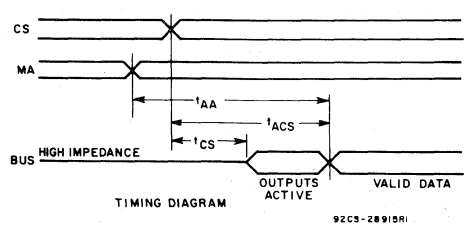
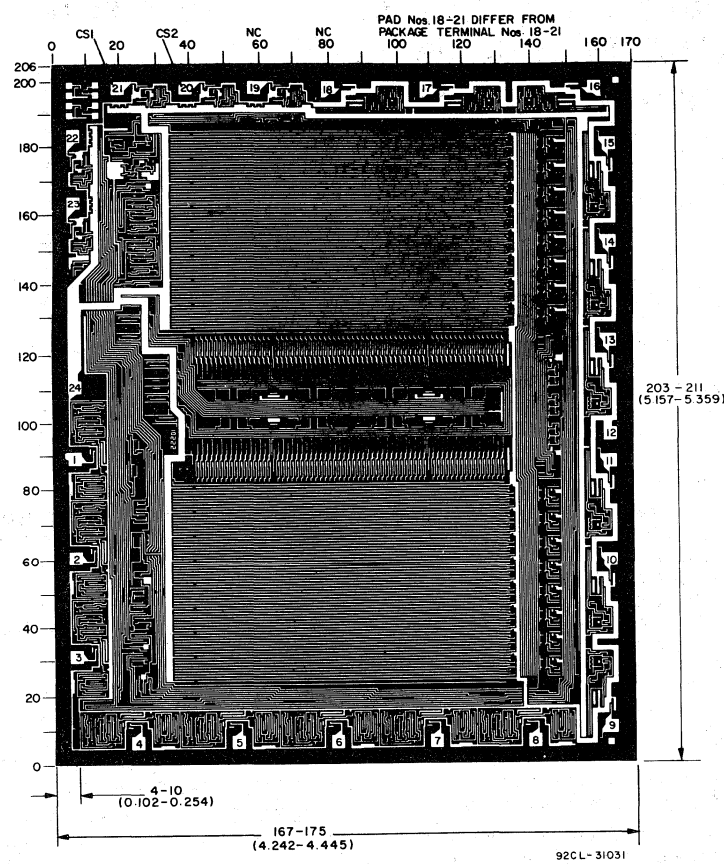


Fig. 3 – Timing diagram.

CDP1834, CDP1834C Types



Dimensions and pad layout for CDP1834 chip.

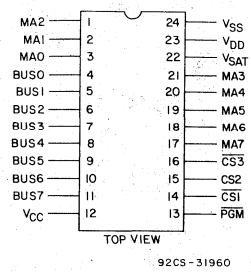
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1842C Types

256-Word x 8-Bit Static EEPROM (Electrically Erasable/Programmable Read-Only Memory)

Objective Data



TERMINAL ASSIGNMENT

Features:

- *Static silicon-gate CMOS circuitry—CD4000-series compatible*
- *Compatible with CDP1800-series microprocessors*
- *Single voltage supply (during READ): 4-6.5 V*
- *Low power dissipation (READ): 20 mW typ.*
- *Fast access time: 1 μs max.*
- *Fast programming time: 5 sec. typ.*
- *Data retention (125°C): 17.3 years typ.*
- *Write/erase endurance ($V_{SAT} \leq 200$ V): >100 cycles*
- *3-state outputs, TTL compatible*
- *Functional replacement for 1700-series UV erasable PROMs*

The RCA-CDP1842C is a static CMOS, 2048-bit programmable read-only memory, organized as 256 words by 8 bits. It is compatible with the CDP1802 microprocessor and will interface directly with the CDP1802 as shown in the system diagram (Fig. 1). The CDP1842C has common data inputs and data outputs and utilizes a single power supply during read operations. RCA ion-implanted, silicon-gate, CMOS technology is employed in the CDP1842C. Three CHIP-SELECT signals ($\overline{CS1}$, CS2, $\overline{CS3}$) are provided. The device is designed for systems where simplicity and low power are desirable.

The CDP1842C is electrically erasable and electrically programmable, making it ideally suited for experimentation and other uses where rapid design changes are necessary. Complete programming and functional testing are performed on each device prior to shipment.

The CDP1842C is supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix).

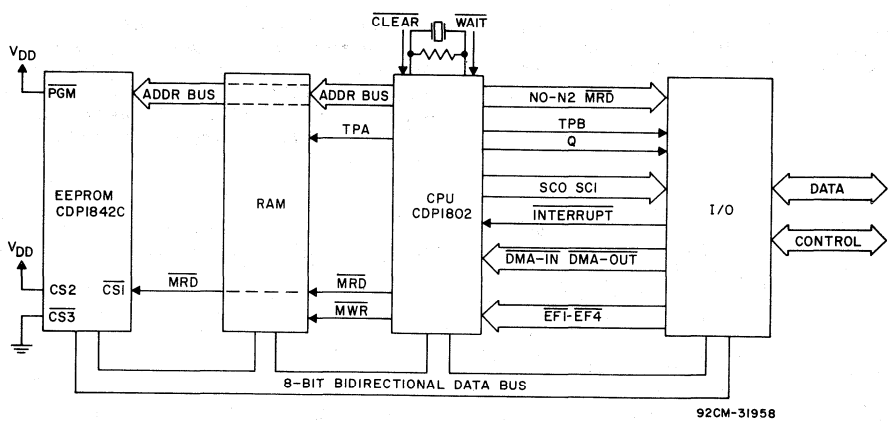


Fig. 1 — Typical CDP1802 microprocessor system using the CDP1842CD.

CDP1842C Types

Erasing Procedure

The erase procedure is a bulk erase in which all 2048 bits (256 x 8) assume a 0 state (OUTPUTS = LOW), allowing the user to program a new bit pattern. The erase procedure consists of raising the V_{SAT} input to the proper erase voltage for 10 ms, with all inputs and outputs low and V_{DD},V_{CC} = 5 volts. Erasing will occur between 90 V and 200 V, with each successive erase procedure requiring a higher erase voltage. In order to maintain the write/erase endurance rating, an interactive erase circuit should be used in which the erase voltage starts at the minimum erase voltage and is increased in 1 volt increments with a verify procedure before each increment.

Programming Procedure

After being erased, the CDP1842C exhibits a zero state (OUTPUT = LOW) in all locations. Programming is accomplished by introducing a 1 state (OUTPUT = HIGH) in the desired bit locations. Programming is done on a byte basis, in which any previously erased bits may be selectively programmed to a 1 state. This feature allows the user to change any 0 bits to 1's in a particular byte in an already programmed CDP1842C without having to do a bulk program or a bulk erase. The program procedure consists of addressing a cell, selecting the CDP1842C, with the $\overline{PGM}$ ($\overline{PROGRAM}$) input at a logic 0 (V_{SS}), and raising the V_{DD} and V_{SAT} inputs to the proper program voltage. The data to be programmed is applied to the BUS0-BUS7 inputs. See Fig. 4. Programming is a function of the program voltage (18-28 V) and the program voltage pulse width (0.1 ms min.). Each successive write/erase cycle requires a higher program voltage and/or a longer pulse width. In order to maintain the write/erase endurance rating, an interactive program circuit should be used in which the program voltage and program voltage pulse width start at the minimum and are increased in 1 volt and/or 0.1 ms increments, with a verify procedure before each increment.

Read Procedure

During a read operation, the CDP1842C functions as a normal CMOS ROM. The read procedure consists of addressing a cell and selecting the CDP1842C, with the $\overline{PGM}$ input at a logic 1 (V_{DD},V_{SAT} = V_{CC}). Data is read at the BUS0-BUS7 outputs. See Fig. 3.

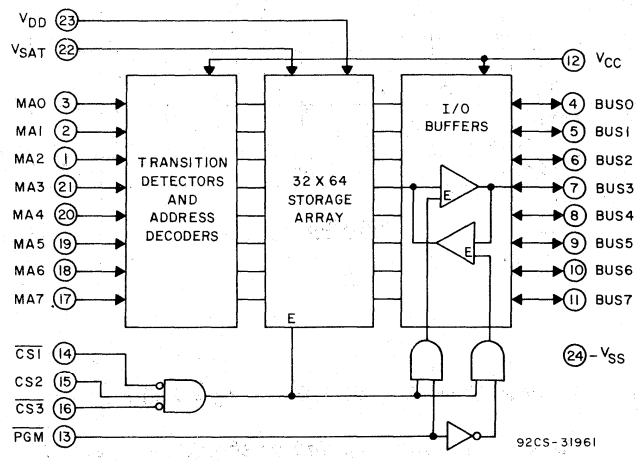


Fig. 2 — Block diagram for CDP1842CD.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)

V_{CC} (READ, PROGRAM, ERASE)	−0.5 to 7 V
V_{DD} (READ, ERASE)	−0.5 to 7 V
V_{DD} (PROGRAM)	−0.5 to 30 V
V_{SAT} (READ)	−0.5 to 7 V
V_{SAT} (PROGRAM)	−0.5 to 30 V
V_{SAT} (ERASE)	−0.5 to 200 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{CC} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
OPERATING-TEMPERATURE RANGE (T_A)	−40 to +85 °C
STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

CDP1842C Types

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, unless otherwise noted.

CHARACTERISTIC	CONDITIONS					LIMITS			UNITS
	V_O (V)	V_{IN} (V)	V_{CC} (V)	V_{DD} (V)	V_{SAT} (V)	CDP1842CD Min.	Typ.*	Max.	
Quiescent Device Current:									
Read Operation									
I_{CC}	—	0,5	5	5	5	—	10	100	
I_{DD}	—	0,5	5	5	5	—	10	100	
I_{SAT}	—	0,5	5	5	5	—	1	10	
Program Operation									μA
I_{CC}	—	0,5	5	28	28	—	10	100	
I_{DD}	—	0,5	5	28	28	—	10	100	
I_{SAT}	—	0,5	5	28	28	—	1	10	
Output Low Drive (Sink Current) I_{OL}	0.4	0,5	5	—	—	1.4	1.6	—	mA
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	—	—	−1.6	−2.0	—	
Output Voltage (Low Level) V_{OL}	—	0,5	5	—	—	—	0	0.05	V
Output Voltage (High Level) V_{OH}	—	0,5	5	—	—	4.95	5	—	
Input Voltage (Low Level) V_{IH}	0.5,4.5	—	5	—	—	—	—	1.5	V
Input Voltage (High Level) V_{IL}	0.5,4.5	—	5	—	—	3.5	—	—	
Input Leakage Current I_{IN}	0.5,4.5	Any Input	5	—	—	—	—	±1	μA
3-State Output Leakage Current I_{OUT}	—	0,5	5	—	—	—	±1	±5	
Input Capacitance C_{IN}	Any Input						5	7.5	pF
Output Capacitance C_{OUT}	Any Output					—	5	7.5	

*Typical values are for $T_A = 25$ °C.

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS	UNITS
Read Operation:		
Supply Voltage Range V_{CC}, V_{DD}, V_{SAT}	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{CC}	
Program Operation:		
Supply Voltage Range V_{CC}	4 to 6.5	
Supply Voltage Range V_{DD}, V_{SAT}	18 to 28	V
Input Voltage Range	V_{SS} to V_{CC}	
Erase Operation:		
Supply Voltage Range V_{CC}, V_{DD}	4 to 6.5	
Supply Voltage Range V_{SAT}	90 to 200	V
Input Voltage Range	V_{SS} to V_{CC}	
Input Signal Rise Or Fall Times t_r,t_f	≤5	μs

CDP1842C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C; V_{CC}, V_{DD}, V_{SAT} ± 5%; Input $t_r, t_f = 10$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC		CONDITIONS V_{CC} (V)	CONDITIONS V_{DD} (V)	CONDITIONS V_{SAT} (V)	TYPICAL VALUES*	UNITS
Read Operation						
Read Cycle Time	t_{RC}				1000	ns
Access Time From Address Change	t_M	5	5	5	1000	ns
Access Time From Chip Select	t_{ACS}	5	5	5	1000	ns
Address Setup Time	t_{AS}	5	5	5	0	ns
Address Hold Time	t_{AH}	5	5	5	0	ns
Bus Contention Delay	t_D	5	5	5	50	ns
Output Hold Time From Address Change	t_{OHA}	5	5	5	50	ns
Output 3-State From Deselection	t_{OTD}	5	5	5	50	ns
Access Time From $\overline{PGM}$	t_{AP}	5	5	5	1000	ns
Program Operation						
Program Cycle Time	t_{PC}	5	18	18	10	ms
		5	28	28	0.1	
Address Setup Time	t_{AS}	5	18,28	18,28	0	ns
Address Hold Time	t_{AH}	5	18,28	18,28	0	ns
PGM To Outputs Inactive	t_{PX}	5	18,28	18,28	200	ns
Chip Select To Program Setup Time	t_{CS}	5	18,28	18,28	500	ns
Chip Select To Program Hold Time	t_{CH}	5	18,28	18,28	200	ns
$\overline{PGM}$ To Program Voltage Setup Time	t_{PS}	5	18,28	18,28	500	ns
$\overline{PGM}$ To Program Voltage Hold Time	t_{PH}	5	18,28	18,28	200	ns
Data Setup Time	t_{DS}	5	18,28	18,28	200	ns
Data Hold Time	t_{DH}	5	18,28	18,28	200	ns
Program Voltage Pulse Width	t_{PVW}	5	18	18	10	ms
		5	28	28	0.1	
Program Voltage Rise Or Fall Time	t_{PR}, t_{PF}	5	18,28	18,28	2	μs

*Typical values are for $T_A = 25$ °C.

TABLE I - OPERATING MODES FOR CDP1842CD

OPERATING MODE	V_{SS} (V)	V_{CC} (V)	V_{DD} (V	V_{SAT} (V)	$\overline{CS1}$ (V)	$\overline{CS2}$ (V)	$\overline{CS3}$ (V)	$\overline{PGM}$ (V)	BUS 0-BUS 7
READ	0	5	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{CC}	OUTPUT
PROGRAM	0	5	18-28	18-28	V_{SS}	V_{CC}	V_{SS}	V_{SS}	INPUT
ERASE	0	5	V_{CC}	90-200	X,V_{CC}	X,V_{SS}	X,V_{CC}	V_{CC}	3-STATE
DESELECT	0	5	V_{CC}	V_{CC}	X	X	V_{CC}	V_{CC}	3-STATE
DESELECT	0	5	V_{CC}	V_{CC}	X	V_{SS}	X	V_{CC}	3-STATE
DESELECT	0	5	V_{CC}	V_{CC}	V_{CC}	X	X	V_{CC}	3-STATE

X = DON'T CARE

CDP1842C Types

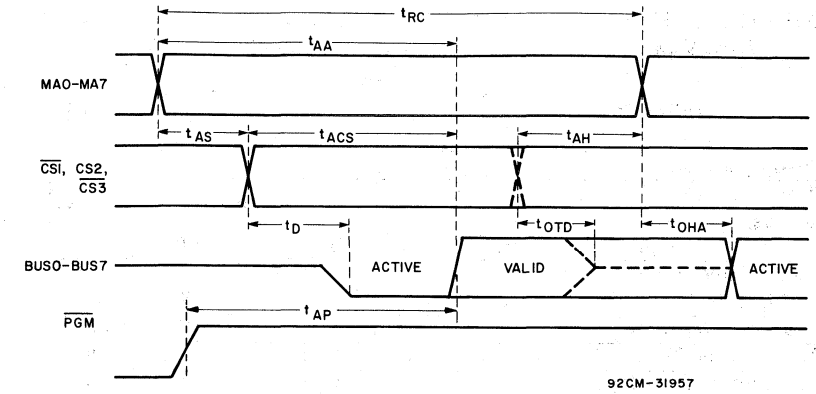


Fig. 3 — READ timing diagram.

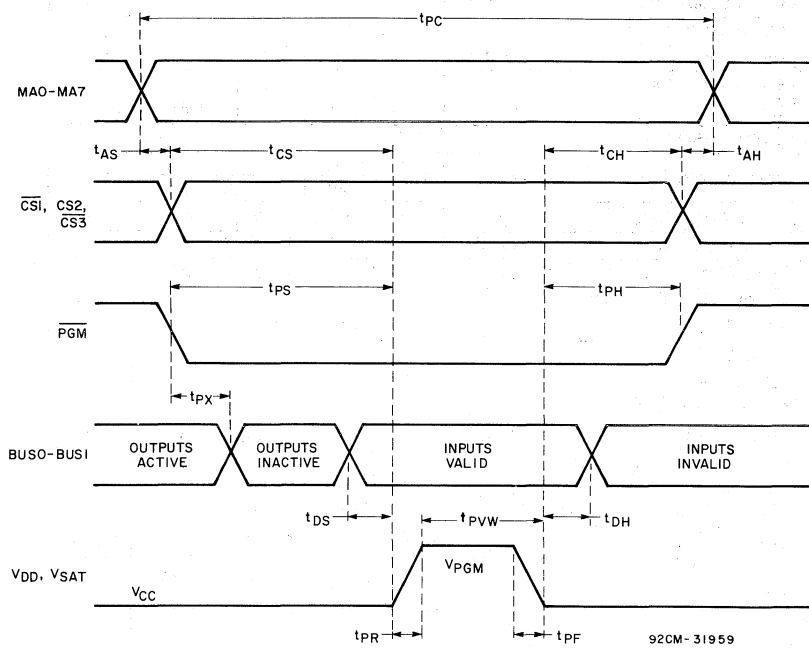


Fig. 4 — Program timing diagram.

TABLE II · POWER DISSIPATION FOR CDP1842CD

OPERATION	CONDITIONS			TYPICAL VALUES*	UNITS
	V_{CC} (V)	V_{DD} (V)	V_{SAT} (V)		
READ QUIESCENT	5	5	5	0.05	mW
READ UNSELECTED (1 MHz)	5	5	5	10	mW
READ SELECTED (1 MHz)	5	5	5	20	mW
WRITE ALL 0'S	5	18	18	0.1	mW
	5	28	28	0.2	
WRITE ALL 1'S	5	18	18	120	mW
	5	28	28	300	
ERASE	5	5	90	0.01	mW
	5	5	200	0.1	

*Typical values are for $T_A = 25\,°C$.

CDP1851, CDP1851C Types

COS/MOS Programmable I/O Interface

Preliminary Data

Features:

- *Silicon-gate CMOS Circuitry*
- *Single Voltage Supply*
- *Operates in Either I/O or Memory Spaces*
- *20 Programmable I/O Lines*
- *Programmable for Operation in Four Modes:*
  - *Input*
  - *Output*
  - *Bidirectional*
  - *Bit-programmable*

The RCA-CDP1851 is a CMOS programmable two-port I/O designed for use as a general-purpose I/O device. It is directly compatible with CDP1800 series microprocessors at maximum speed. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

The CDP1851 has a supply-voltage range of 4 to 10.5 V, and the CDP1851C has a range of 4 to 6.5 V. Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages.

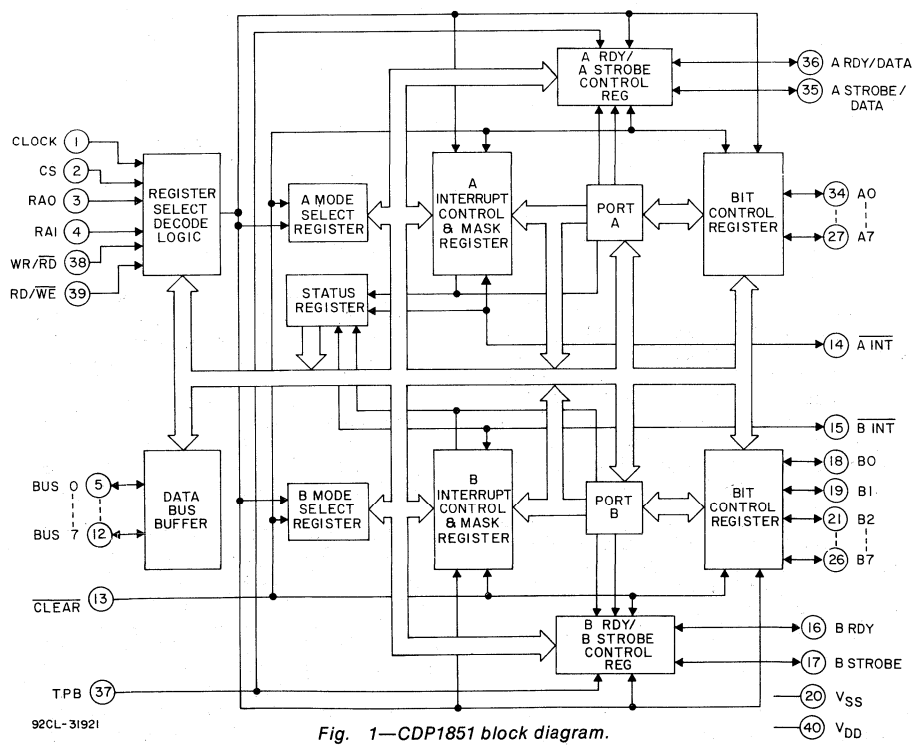


Fig. 1—CDP1851 block diagram.

CDP1851, CDP1851C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1851 ..... −0.5 to +11 V
CDP1851C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) ..... −55 to +125 °C
PLASTIC PACKAGES (E SUFFIX TYPES) ..... −40 to +85 °C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265 °C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1851D CDP1851E		CDP1851CD CDP1851CE		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

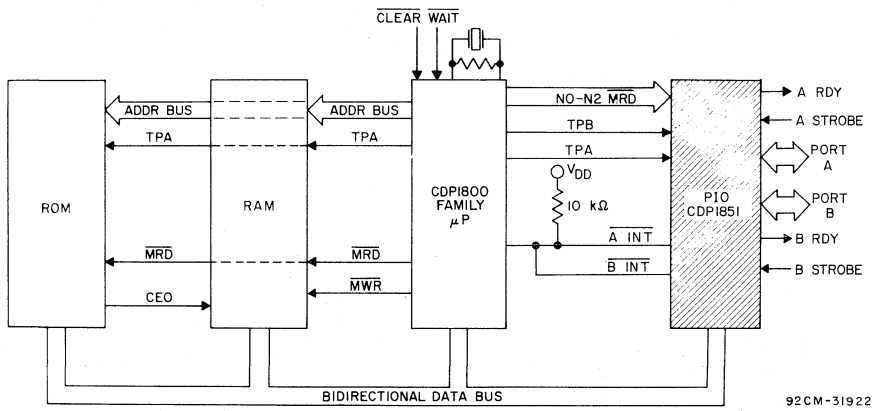


Fig. 2—Typical CDP1800 series microprocessor system.

Functional Description

The CDP1851 is a two-port I/O interface with four programmable modes; input, output, bidirectional, and bit-programmable. Port A is programmable for all modes, and port B is programmable for the input, output, and bit-programmable modes. When port A is in the bidirectional mode, port B must be in the bit-programmable mode.

In the input mode, each port has two handshaking lines, RDY and STROBE. A high-to-low transition on the STROBE line will generate an interrupt to indicate that data have been loaded into the port. When the CPU reads the data, the interrupt is reset, and the RDY line goes high to indicate that the port is empty.

The STROBE and RDY lines are also the handshaking lines for the output mode. A high-to-low transition on the STROBE line generates an interrupt to indicate that data have been received by a peripheral device. When the CPU loads data into the port, the interrupt is reset and the RDY line goes high to indicate that the port is full.

In the bidirectional mode, port A has four handshaking lines. A RDY and A STROBE are used for input control. A high-to-low transition on the A STROBE line generates an interrupt ($\overline{\text{A INT}}$) to indicate that data have been loaded into port A. When the CPU reads the data, the interrupt ($\overline{\text{A INT}}$) is reset and the A RDY line goes high to indicate that port A is empty. The port B handshaking lines, B RDY and B STROBE, are used for the output control. B STROBE functions as an output enable signal. When high, the 3-state drivers are turned on. A high-to-low transition on the B STROBE line generates an interrupt ($\overline{\text{A INT}}$) to indicate that data have

CDP1851, CDP1851C Types

been received by a peripheral device. When the CPU loads data into port A, the interrupt is reset, and the B RDY line goes high to indicate that port A is full. The status register must be read to determine whether $\overline{A\ INT}$ was set by A STROBE or by B STROBE. When port A is in the bidirectional mode, port B has no use for its handshaking lines, and must be programmed in the bit-programmable mode.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, Except as Noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1851D CDP1851E			CDP1851CD CDP1851CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	—	0,5	5	—	0.01	50	—	0.02	200	μA
	—	0,10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4.6	0,5	5	−1.15	−2.3	—	−1.15	−2.3	—	mA
	9.5	0,10	10	−2.6	−5.2	—	—	—	—	
Output Voltage• Low-Level V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage• High-Level V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	—	±1	—	—	±1	μA
		0,10	10	—	—	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	μA
	0,10	0,10	10	—	$\pm 10^{-4}$	±10	—	—	—	
Operating Current, I_{DD}▲	—	0,5	5	—	1.5	—	—	1.5	—	mA
	—	0,10	10	—	10	—	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	pF

*Tyical values are for $T_A = 25$ °C.

•$I_{OL} = I_{OH} = 1$ μA.

▲Operating current is measured at 200 kHz for 5 V and 400 kHz for 10 V with open outputs. (These are max. frequencies in a CDP1802 system.)

CDP1851, CDP1851C Types

In the bit-programmable mode, the RDY, STROBE, and I/O lines of each port can be set as individual data bit I/O lines. The RDY/STROBE control register is programmed to set the RDY and STROBE lines as inputs or outputs. To read these lines, if set as inputs, the status register is read. The exception to this is when port A is bidirectional. In this mode, port A has use of B RDY and B STROBE. The bit-control register is programmed to set the individual data bit I/O lines of the ports as either inputs or outputs. In the bit-programmable mode, the interrupt control and mask register determine the logical combination of data bit lines which, when true, will generate an interrupt. The RDY and STROBE lines are not monitored for interrupts.

In all modes, interrupts can be detected on the $\overline{INT}$ output terminals or by reading the status register. The $\overline{INT}$ outputs are open-drain NMOS devices that allow wired ORing, and they must be tied to pullup resistors (normally 10kΩ). When reading or writing to the ports or to the control/status register, the register address lines, RA0 and RA1, are used for port or register selection. The CDP1851 can be used in either memory or I/O space.

INPUT MODE

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, see Figs. 3 and 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1851			CDP1851C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Times:								
Chip Select to CLOCK, t_{CSCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
RD/$\overline{WE}$ to CLOCK, t_{RWCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
WR/$\overline{RE}$ to CLOCK, t_{WRCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Data In to STROBE, t_{DIST}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Minimum Hold Times:								
Chip Select After CLOCK, t_{HCSCL}	5	—	75	120	—	75	120	ns
	10	—	40	60	—	—	—	
Address After TPB, T_{HATPB}	5	—	−50	0	—	−50	0	
	10	—	−25	0	—	—	—	
Data In After STROBE, t_{HSTDI}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus Out After Address, t_{HADOH}	5	50	325	500	50	325	500	
	10	25	165	250	—	—	—	
Propagation Delay Times:								
TPB to $\overline{INT}$, t_{PINT}	5	—	200	300	—	200	300	ns
	10	—	100	150	—	—	—	
STROBE to $\overline{INT}$, t_{STINT}	5	—	200	300	—	200	300	
	10	—	100	150	—	—	—	
TPB to RDY, t_{TPRDY}	5	—	250	375	—	250	375	
	10	—	125	200	—	—	—	
STROBE to RDY, t_{STRDY}	5	—	260	400	—	260	400	
	10	—	130	200	—	—	—	
Minimum Pulse Widths:								
CLOCK, t_{WCL}	5	—	75	120	—	75	120	ns
	10	—	40	60	—	—	—	
TPB, t_{WTPB}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
STROBE, t_{WST}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
Access Time, Address to Data Bus Out, t_{ADA}	5	—	325	500	—	325	500	ns
	10	—	165	250	—	—	—	

Note 1 - Typical values are for $T_A = 25$ °C and nominal voltages.

Note 2 - Maximum limits of minimum characteristics are the values above which all devices function.

CDP1851, CDP1851C Types

OUTPUT MODE

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, see Figs. 4 and 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1851			CDP1851C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Times:								
Chip Select to CLOCK, t_{CSCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
RD/$\overline{WE}$ to CLOCK, t_{RWCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
WR/$\overline{RE}$ to CLOCK, t_{WRCL}	5	—	75	120	—	75	120	
	10	—	40	60	—	—	—	
Address to WRITE*, t_{AW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus to WRITE*, t_{DW}	5	—	80	120	—	80	120	
	10	—	40	60	—	—	—	
Minimum Hold Times:								
Chip Select After CLOCK, t_{HCSCL}	5	—	75	120	—	75	120	ns
	10	—	40	60	—	—	—	
Address After WRITE*, t_{HAW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Data Bus After WRITE*, t_{HDW}	5	—	50	75	—	50	75	
	10	—	25	40	—	—	—	
Propagation Delay Times:								
WRITE* to Data Out, t_{WDO}	5	—	225	350	—	225	350	ns
	10	—	125	200	—	—	—	
WRITE* to $\overline{INT}$, t_{WINT}	5	—	300	450	—	300	450	
	10	—	150	225	—	—	—	
WRITE* to RDY, t_{WRDY}	5	—	350	525	—	350	525	
	10	—	175	275	—	—	—	
STROBE to $\overline{INT}$, t_{STINT}	5	—	200	300	—	200	300	
	10	—	100	150	—	—	—	
STROBE to RDY, t_{STRDY}	5	—	260	400	—	260	400	
	10	—	130	200	—	—	—	
Minimum Pulse Widths:								
CLOCK, t_{WCL}	5	—	75	120	—	75	120	ns
	10	—	40	60	—	—	—	
STROBE, t_{WST}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
WRITE*, t_{WW}	5	—	175	275	—	175	275	
	10	—	90	150	—	—	—	

*WRITE is the overlap of RD/$\overline{WE} = 0$ and WR/$\overline{RE} = 1$.

Note 1 - Typical values are for $T_A = 25$ °C and nominal voltages.

Note 2 - Maximum limits of minimum characteristics are the values above which all devices function.

CDP1851, CDP1851C Types

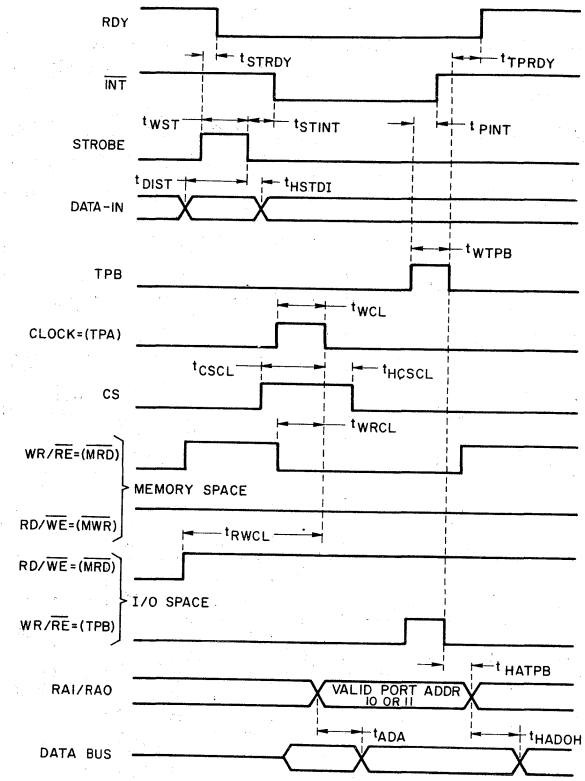
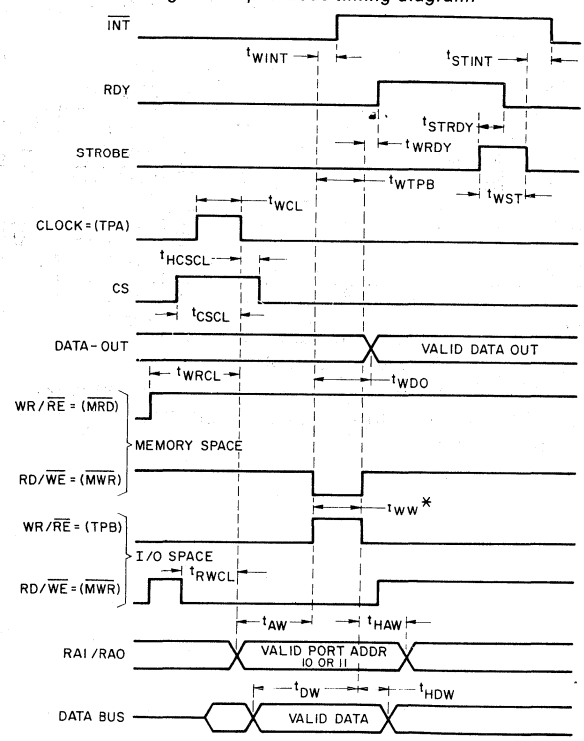


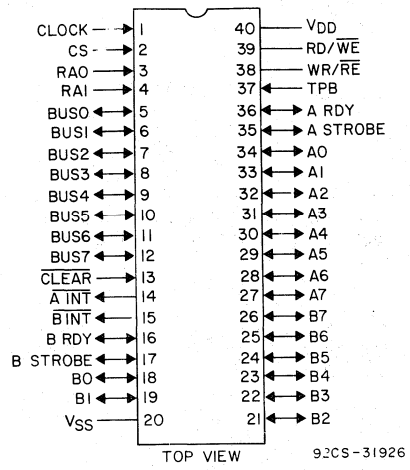
Fig. 3—Input mode timing diagram.



* WRITE IS THE OVERLAP OF WR/RE=1 AND RD/WE=0

Fig. 4—Output mode timing diagram.

CDP1851, CDP1851C Types



CDP1851 Terminal Assignment

FUNCTIONAL DESCRIPTION OF CDP1851 TERMINALS

CLOCK (Input);
Positive input pulse that latches READ and CS on its trailing edge.

CS—CHIP SELECT (Input):
A high-level voltage at this input selects the CDP1851 PIO.

RA0—REGISTER ADDRESS 0 (Input):
This input and RA1 are used to select either the ports or the control/status registers.

RA1—REGISTER ADDRESS 1 (Input):
See RA0

BUS 0—BUS 7:
Bidirectional CPU data bus.

$\overline{\text{CLEAR}}$ (Input):
A low-level voltage at this input resets both ports to the input mode, and also resets the status register, A RDY, B RDY, and interrupt enable (disabling interrupts).

$\overline{\text{A INT}}$—$\overline{\text{A INTERRUPT}}$ (Output):
A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table V. This output is an open-drain NMOS device (to allow wired ORing) and must be tied to a pullup resistor, normally 10 kΩ.

$\overline{\text{B INT}}$—$\overline{\text{B INTERRUPT}}$ (Output):
A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table VI. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY—B READY (Output):
This output is a handshaking or data bit I/O line in the bit-programmable mode. See Table VII.

B STROBE (Input):
An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B 0—B 7:
Data input or output lines for port B.

V_{SS}:
Ground.

A 0—A 7:
Data input or output lines for port A.

A STROBE (Input):
An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

A RDY—A READY (Output):
An output handshaking line or data bit I/O line. See Table VIII.

TPB (Input):
A positive input pulse used as a data load, set, or reset strobe.

WR/$\overline{\text{RE}}$—WRITE/$\overline{\text{READ}}$ ENABLE (Input):
A positive input used to write data from the CPU bus into the CDP1851.

RD/$\overline{\text{WE}}$—READ/$\overline{\text{WRITE}}$ ENABLE (Input):
A positive input used to read data from the CDP1851 to the CPU bus.

V_{DD}:
Positive supply voltage.

Operation

1. Initialization and Controls

The CDP1851 must be cleared by a low on the $\overline{\text{CLEAR}}$ input during power-on to set the PIO for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. When in this mode the CDP1851 must be cleared to change modes. A low on the $\overline{\text{CLEAR}}$ input resets the status register, A RDY, B RDY, INTERRUPT MASK, and INTERRUPT ENABLE (disabling the INTERRUPTS), and also sets both ports to the input mode.

2. Input Mode

Either port can be set for the input mode. To set a port in the input mode, the PIO is reset by a low on $\overline{\text{CLEAR}}$ or the following control byte is sent with RA1 = 0 and RA0 = 1:

CONTROL BYTE #1

Bit	7	6	5	4	3	2	1	0
	0	0	x	Set B	Set A	x	1	1

CDP1851, CDP1851C Types

To set port A, Set A = 1, and to set port B, Set B = 1. Input data from a peripheral device are latched into the port on a high-to-low transition of the STROBE line. The $\overline{INT}$ line is also set on this transition indicating, that input data have been strobed into the port by a peripheral device. The RDY line is reset on the leading edge of STROBE. To read the port the CPU selects the chip with a high voltage level on CS and addresses the correct port with RA0 and RA1. CS and READ* are latched on the trailing edge of the clock. A low-to-high transition on TPB resets $\overline{INT}$. A high-to-low transition on TPB during READ sets the RDY line indicating to the peripheral device that the port is empty and is ready to be loaded. If RDY is low when the input mode is entered (i.e. after reset), a "dummy" READ must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

3. Output Mode

Either port can be set for the output mode by sending the following control byte with RA1 = 0 and RA0 = 1:

CONTROL BYTE #2

Bit	7	6	5	4	3	2	1	0
	0	1	x	Set B	Set A	x	1	1

To set port A, Set A = 1, and to set port B, Set B = 1. A high-to-low transition on the STROBE line sets $\overline{INT}$, indicating that data have been read by the peripheral device. A low-to-high transition on the STROBE line resets the RDY line. To write to the port, the CPU selects the chip with a high voltage level on CS and addresses the correct port with RA0 and RA1. CS and READ are latched on the trailing edge of CLOCK. Data are latched into the port from the CPU on the trailing edge of WRITE*. The leading edge of WRITE resets $\overline{INT}$, and on the trailing edge the RDY line is set, indicating to the peripheral device that data have been loaded into the port and is ready to be read.

4. Bidirectional Mode

Only port A can be set in the bidirectional mode. Before setting port A for bidirectional operation, port B must be set (if it hasn't already been) for the bit programmable mode. To set port A, the following control byte is sent with RA1 = 0 and RA0 = 1:

CONTROL BYTE #3

Bit	7	6	5	4	3	2	1	0
	1	0	x	0	1	x	1	1

When port A is in the bidirectional mode, it uses port B's handshaking lines for output control.

a) Input—Input data from a peripheral device are latched into port A on a high-to-low transition of the STROBE line. The $\overline{A\ INT}$ line is also set on this transition, indicating that input data have been strobed into port A by the peripheral device. The A RDY line reset on the low-to-high transition of A STROBE. To read port A, the CPU selects the chip with a high voltage level on CS and addresses port A with RA0 = 0 and RA1 = 1. CS and READ are latched on the trailing edge of CLOCK. A low-to-high transition of TPB during READ resets $\overline{A\ INT}$. A high-to-low transition on TPB sets the A RDY line to indicate to the peripheral device that port A is empty and is ready to be loaded. If READY is low when the bidirectional mode is entered (i.e. after reset), a "dummy" READ must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

b) Output—For outputting data, B STROBE functions as an output enable. When high, the 3-state drivers are turned on. A high-to-low transition on the B STROBE line sets $\overline{A\ INT}$, indicating that data have been read by the peripheral device. A low-to-high transition on B STROBE line resets the B RDY line. To write to port A, the CPU selects the chip with a high voltage level on CS and addresses port A with RA0 = 0 and RA1 = 1. CS and READ are latched on the trailing edge of CLOCK. Data are latched into port A from the CPU on the trailing edge of WRITE. The leading edge of WRITE resets $\overline{A\ INT}$. The trailing edge of WRITE sets the B RDY line high indicating that data have been loaded into port A and are ready to be read.

Since $\overline{A\ INT}$ is used for both input and output, the status register (bits 2 and 3) must be read to determine what condition caused $\overline{A\ INT}$ to be set (see Control Byte #4).

*READ is the overlap of RD/$\overline{WE}$ = 1 and WR/$\overline{RE}$ = 0.

*WRITE is the overlap of WR/RE = 1 and RD/WE = 0.

CDP1851, CDP1851C Types

CONTROL BYTE #4

Bit	7	6	5	4	3	2	1	0	
	x	x	x	x	Output Data	Input Data	x	x	If Bit 3 = 1, $\overline{\text{A INT}}$ was set by B STROBE If Bit 2 = 1, $\overline{\text{A INT}}$ was set by A STROBE

5. Bit-Programmable Mode

Either port can be set in the bit-programmable mode. Each port has its own I/O lines (8) that are used as data bit I/O lines. These can be programmed as individual input or output lines. The handshaking lines of each port (2) can also be used as data bit I/O lines. An exception to this is when port A is in the bidirectional mode and is using port B's handshaking lines. In this case, port B has no control over B RDY or B STROBE. To set a port in the bit-programmable mode, the following control byte is sent with RA1 = 0 and RA0 = 1:

CONTROL BYTE #5

Bit	7	6	5	4	3	2	1	0
	1	1	x	Set B	Set A	x	1	1

To set port B, Set B = 1, and to set port A, Set A = 1. After setting a port in this mode the next control byte sent sets the I/O register, determining which I/O lines (8) are inputs and which are outputs (see Control Byte #6).

Lines programmed as outputs are set high or low by writing to the appropriate port. Data are latched from the CPU as if the port were in the output mode. Writing data to lines programmed as inputs has no effect.

The input lines are read by reading the appropriate port. Input lines are non-latching and therefore data must be stable during a READ to guarantee valid results. By reading a port, the CPU reads both the input and output lines.

The handshaking lines can also be used as data bit I/O lines. To set them as either input lines or output lines, control byte 7 is sent to the RDY/STROBE I/O control register with RA1 = 0 and RA0 = 1.

The STROBE/RDY select line is used to program the RDY and STROBE separately. To read the RDY or STROBE lines when used as inputs the status register is read (see Control Byte #8).

The eight I/O lines of each port can generate interrupts. These interrupts can be programmed to occur on certain logic conditions. To program the conditions

CONTROL BYTE #6

Bit	7	6	5	4	3	2	1	0
	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

$I/O_N = 1$ sets the I/O_N line to be an output
$I/O_N = 0$ sets the I/O_N line to be an input

CONTROL BYTE #7

Bit	7	6	5	4	3	2	1	0
	STROBE Line I/O	RDY Line I/O	STROBE Output Data	RDY Output Data	STROBE Select	RDY Select	A/B	O

A/B = 0, set A RDY/A STROBE control register
A/B = 1, set B RDY/B STROBE control register
STROBE/RDY line I/O = 0, input line
STROBE/RDY line I/O = 1, output line
STROBE/RDY output data = 0, output data = 0
STROBE/RDY output data = 1, output data = 1
STROBE/RDY Select = 0, no change for that data bit I/O line
STROBE/RDY Select = 1, Data bit line programmed according to control word

CONTROL BYTE #8

Bit	7	6	5	4	3	2	1	0
	B STROBE Data	B RDY Data	A STROBE Data	A RDY Data	x	x	x	x

CDP1851, CDP1851C Types

that will generate an interrupt, control byte 9 is sent to the interrupt control and mask register with RA1 = 0 and RA1 = 1. Interrupts should be disabled while programming the interrupt control and mask registers (see section 6).

If "mask follows" = 0, then no changes occur in the mask registers. If "mask follows" = 1, then the next control byte sent sets the interrupt mask as shown in Control Byte #10.

The interrupt mask determines what bits are monitored for logical interrupt conditions that have been programmed. If mask bit = 1, then that bit is masked out. If mask bit = 0 then that bit is monitored. Any combination of masked or monitored I/O data bit lines, except all lines masked out (control byte = FF), are permissible. If inputs only are to be monitored for interrupt conditions, then all outputs must be masked out, and also if only outputs are desired to be monitored then all inputs must be masked. But any combination of inputs or outputs can be monitored for interrupts. The logical-condition bits (6 and 5) of the interrupt control word determine the logical condition of the monitored I/O lines that will generate an interrupt.

Bit 6	Bit 5	Logic condition
0	0	NAND
0	1	OR
1	0	NOR
1	1	AND

INT will be reset when the logical combination of monitored I/O lines is no longer true. The handshaking lines cannot be monitored for interrupt conditions.

6. ENABLE/DISABLE, $\overline{INT}$

To enable or disable the $\overline{INT}$ line in all modes, control byte 11 is sent to the interrupt control register with RA1 = 0 and RA0 = 1. Interrupts can be detected on the $\overline{A\ INT}$ and $\overline{B\ INT}$ terminals or by reading the status register (see Control Byte #12).

When programming, all interrupts should be disabled or false interrupts may occur.

CONTROL BYTE #9

Bit	7	6	5	4	3	2	1	0
	0	Logical Condition	Logical Condition	Mask Follows	A/B	1	0	1

A/B = 0 sets the interrupt control register of port A
A/B = 1 sets the interrupt control register of port B

CONTROL BYTE #10

Bit	7	6	5	4	3	2	1	0
	Mask bit 7	Mask bit 6	Mask bit 5	Mask bit 4	Mask bit 3	Mask bit 2	Mask bit 1	Mask bit 0

CONTROL BYTE #11

Bit	7	6	5	4	3	2	1	0
	$\overline{INT}$ Enable	x	x	x	A/B	0	0	1

$\overline{INT}$ enable = 1 $\overline{INT}$ enabled (as addressed by bit 3)
$\overline{INT}$ enable = 0 $\overline{INT}$ disabled (as addressed by bit 3)
A/B = 0 sets port A's interrupt control register
A/B = 1 sets port B's interrupt control register

CONTROL BYTE #12

Bit	7	6	5	4	3	2	1	0
	x	x	x	x	x	x	$\overline{A\ INT}$	$\overline{B\ INT}$

$\overline{A\ INT}$ = 1 $\overline{A\ INT}$ has been set
$\overline{B\ INT}$ = 1 $\overline{B\ INT}$ has been set

CDP1851, CDP1851C Types

TABLE I—CONTROL REGISTER SELECTION SUMMARY

Bit 7	6	5	4	3	2	1	0	Action
0	0	x	Set B	Set A	x	1	1	See A
0	1	x	Set B	Set A	x	1	1	See B
1	0	x	0	1	x	1	1	See C
1	1	x	Set B	Set A	x	1	1	See D
STROBE Line I/O	RDY Line I/O	STROBE Output Data	RDY Output Data	STROBE Sel.	RDY Sel.	A/B	0	See E
0	Logic Con.	Logic Con.	Mask Follows	A/B	1	0	1	See F
$\overline{\text{INT}}$ Enable	x	x	x	A/B	0	0	1	See G

A. Set port input mode

B. Set port output mode

C. Set port A bidirectional mode

D. Set port bit-programmable mode

E. Set RDY/STROBE I/O control register

F. Set interrupt control and mask register—Bit programmable mode

G. Set interrupt enable/disable

TABLE II—STATUS REGISTER

Bit 7	6	5	4	3	2	1	0
B STROBE Data	B RDY Data	A STROBE Data	A RDY Data	Output Data	Input Data	A $\overline{\text{INT}}$	B $\overline{\text{INT}}$
Bit-Programmable Mode				Bidirectional Mode		All Modes	

TABLE III—CPU CONTROLS

CS*	RA1	RA0	RD/$\overline{\text{WE}}$	WR/$\overline{\text{RE}}$	Action
0	x	x	x	x	No-op bus 3-stated
x	0	0	x	x	No-op bus 3-stated
x	x	x	0	0	No-op bus 3-stated
x	x	x	1	1	No-op bus 3-stated
1	0	1	1	0	Read* status register
1	0	1	0	1	Load control register
1	1	0	1	0	Read* port A
1	1	0	0	1	Load port A
1	1	1	1	0	Read* port B
1	1	1	0	1	Load port B

*READ = RD/$\overline{\text{WE}}$ = 1 and WR/$\overline{\text{RE}}$ = 0 is latched on trailing edge of CLOCK.

TABLE IV—MEMORY I/O USE

	RD/$\overline{\text{WE}}$ Input	WR/$\overline{\text{RE}}$ Input	TPB Input	
I/O Space	$\overline{\text{MRD}}$	TPB	TPB	PIO Terminals
Memory Space	$\overline{\text{MWR}}$	$\overline{\text{MRD}}$	TPB	CPU Terminals

CDP1851, CDP1851C Types

TABLE V—$\overline{\text{A INT}}$

Set			Reset	
Mode Port A	**Mode Port B**	**Cause**	**Condition**	**Time**
Input	X	A STROBE ↓ (data loaded into port A by peripheral)	Data read by CPU from port A	TPB ↓
Output	X	A STROBE ↓ (output data re-received by peripheral)	Data loaded by CPU into port A	Leading edge of WRITE
Bit-Prog.	X	See data control word use	See data control word use	
*Bidirectional	Bit-prog.	A STROBE ↓ (data loaded into port A by peripheral or B STROBE ↓ (output data received by peripheral)	Data read from Port A by CPU or data loaded into port A by CPU	TPB ↓

*The status register indicates whether $\overline{\text{A INT}}$ occurred because port A is empty or full.

TABLE VI—$\overline{\text{B INT}}$

Set			Reset	
Mode Port A	**Mode Port B**	**Cause**	**Condition**	**Time**
Bidir.	Input	B STROBE ↓ (data loaded into port B by peripheral)	Data read by CPU from port B	TPB ↓
Bidir.	Output	B STROBE ↓ (output data received by peripheral)	Data loaded by CPU into port B	Leading edge of WRITE#
Bidir.	Bit-Prog.	See data control word use	See data control word use	
Bidir.	Bit-Prog.	Not used	Not used	

#WRITE is the overlap of WR/$\overline{\text{RE}}$ = 1 and RD/$\overline{\text{WE}}$ = 0.

TABLE VII—B RDY

Set			Reset	
Mode Port A	**Mode Port B**	**Cause**	**Condition**	**Time**
Bidir.	Input	TPB ↓ (data read by CPU from port B	Data loaded into port B by peripheral	B STROBE ↓
Bidir.	Output	Trailing edge of WRITE# (data loaded into port B from CPU)	Output data received by peripheral	B STROBE ↓
Bidir.	Bit-Prog.	See data control word use	See data control word use	
Bidir.*	Bit-Prog.	Trailing edge of WRITE (data loaded into port A from CPU	Output data received by peripheral	B STROBE ↓

#WRITE is the overlap of WR/$\overline{\text{RE}}$ = 1 and RD/$\overline{\text{WE}}$ = 0
*Port B must be programmed to be in the bit-programmable mode

CDP1851, CDP1851C Types

TABLE VIII— A RDY

Set			Reset	
Mode Port A	**Mode Port B**	**Cause**	**Condition**	**Time**
Input	X	TPB ↘ (data read by CPU)	Data loaded into port A by peripheral	A STROBE ↘
Output	X	Trailing edge of WRITE* (data loaded into port A from CPU)	Output data received by peripheral	A STROBE ↘
Bit-Prog.	X	See data control word use	See data control word use	
Bidir.▲	Bit-Prog.	TPB ↘ (data read by CPU)	Data loaded into port A by peripheral	A STROBE ↘

*WRITE is the overlap of WR/$\overline{RE}$ = 1 and RD/$\overline{WE}$ = 0
▲Port B must be in the bit-programmable mode.

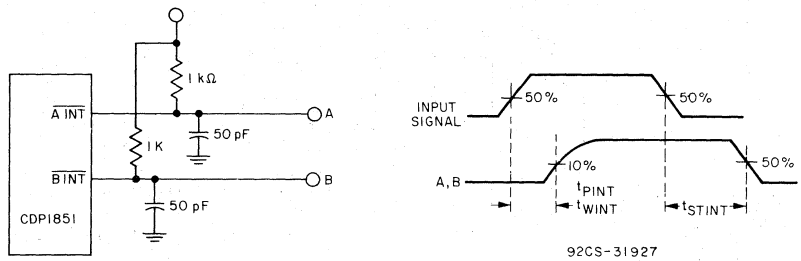


Fig. 5—Interrupt signal propagation delay time test circuit and waveforms.

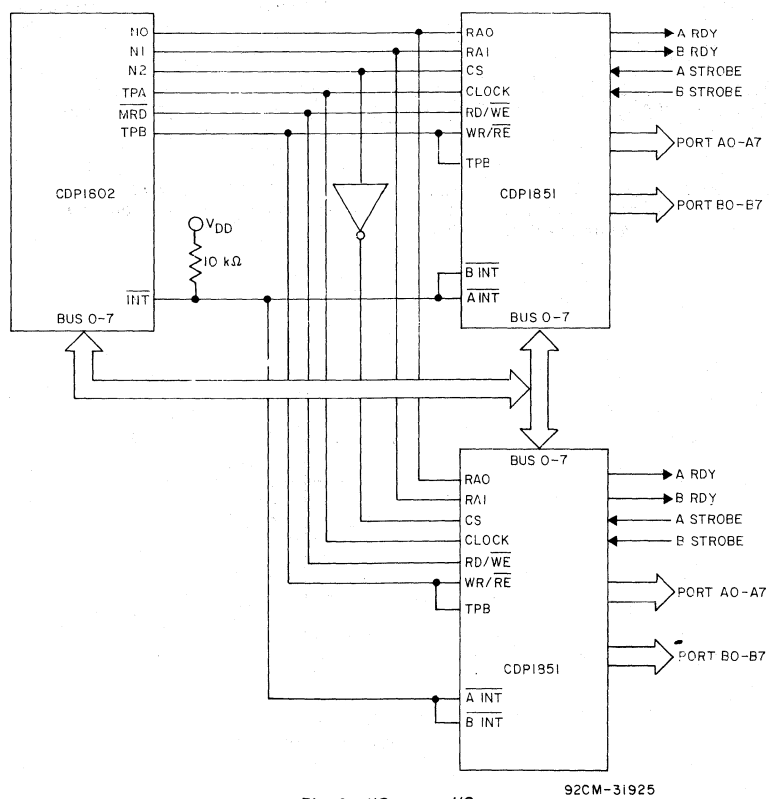
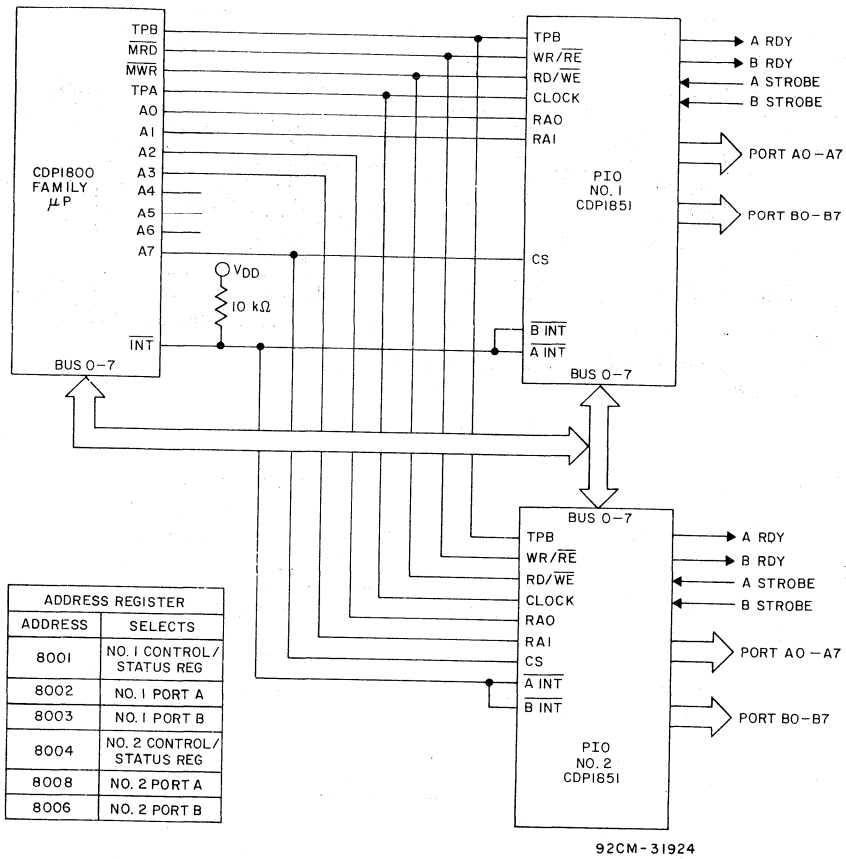


Fig. 6—I/O space I/O.

CDP1851, CDP1851C Types



ADDRESS REGISTER	
ADDRESS	SELECTS
8001	NO. 1 CONTROL/ STATUS REG
8002	NO. 1 PORT A
8003	NO. 1 PORT B
8004	NO. 2 CONTROL/ STATUS REG
8008	NO. 2 PORT A
8006	NO. 2 PORT B

Fig. 7—Memory space I/O. This configuration allows up to four CDP1851's to occupy memory space 8XXX with no additional hardware (A4·A5 and A6·A7 are used as RA0 and RA1 on the third and fourth PIO's).

CDP1851, CDP1851C Types

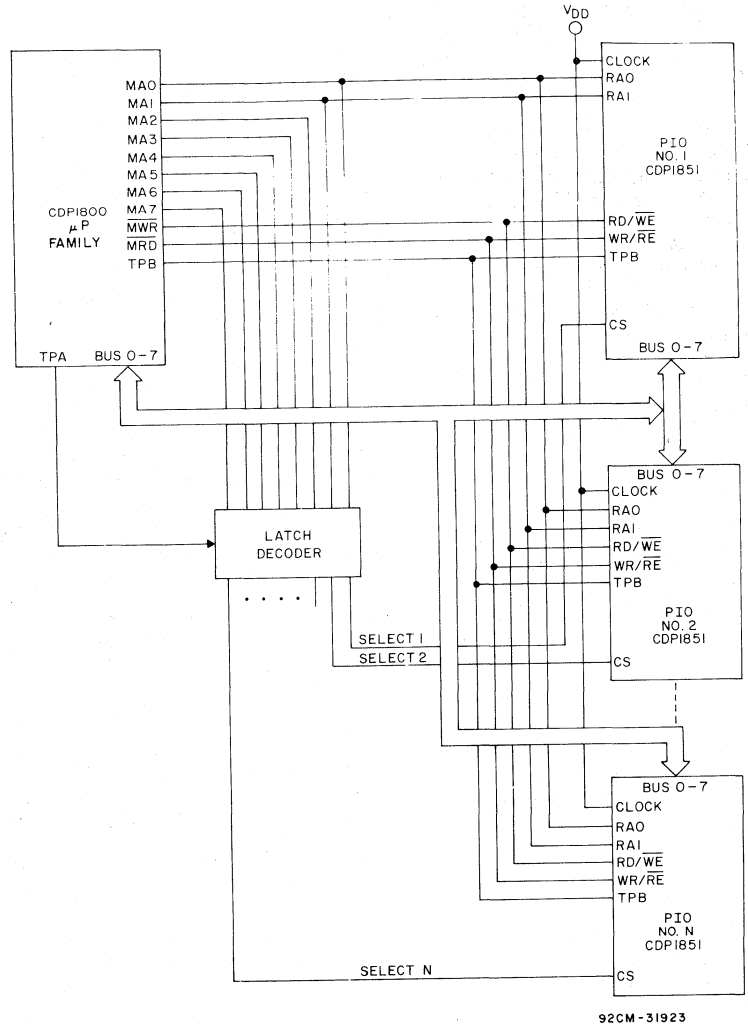


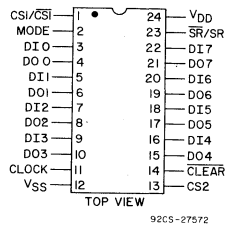
Fig. 8—Extended memory-mapped system with N PIO's using high-order address latch decoder.

CDP1852, CDP1852C Types

8-Bit Input/Output Port

Features:

- **Static Silicon-Gate CMOS circuitry**
- **Compatible with CDP1800-series**
- **Interfaces with CDP1802 and CDP1804 microprocessors without additional components**
- **Single voltage supply**
- **Full military temperature range (−55°C to +125°C)**
- **Parallel 8-bit data register and buffer**
- **Flip-flop for service request**
- **Asynchronous register clear**
- **Low quiescent and operating power**



Terminal Assignment

The RCA-CDP1852 and CDP1852C are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 or CDP1804 without additional components. They are also useful as 8-bit address latches in 1800-series microprocessor systems and as I/O ports in general purpose applications.

The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request output ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor via a flag or interrupt line. When CS1·CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1·CS2 resets the Service Request output, $\overline{SR}$=1.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1}$·CS2·CLOCK=1. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1}$·CS2=1 and will be present, 1 level, until the following negative, high-to-low transition of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852 and CDP1852C are supplied on 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix).

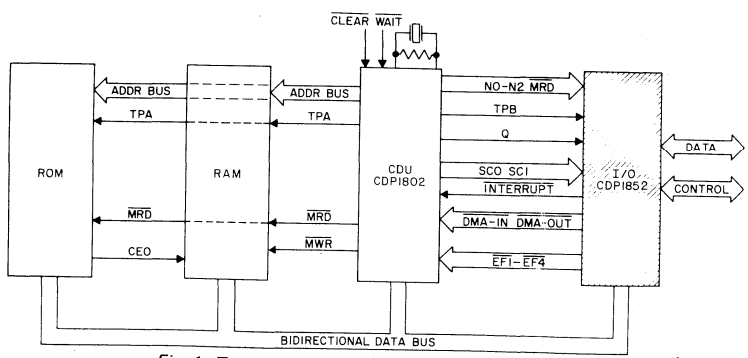


Fig. 1—Typical CDP1802 microprocessor system.

CDP1852, CDP1852C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
- CDP1852 . . . . . −0.5 to +11 V
- CDP1852C . . . . . −0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
- For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
- For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
- For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPES D, H . . . . . −55 to +125°C
- PACKAGE TYPE E . . . . . −40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

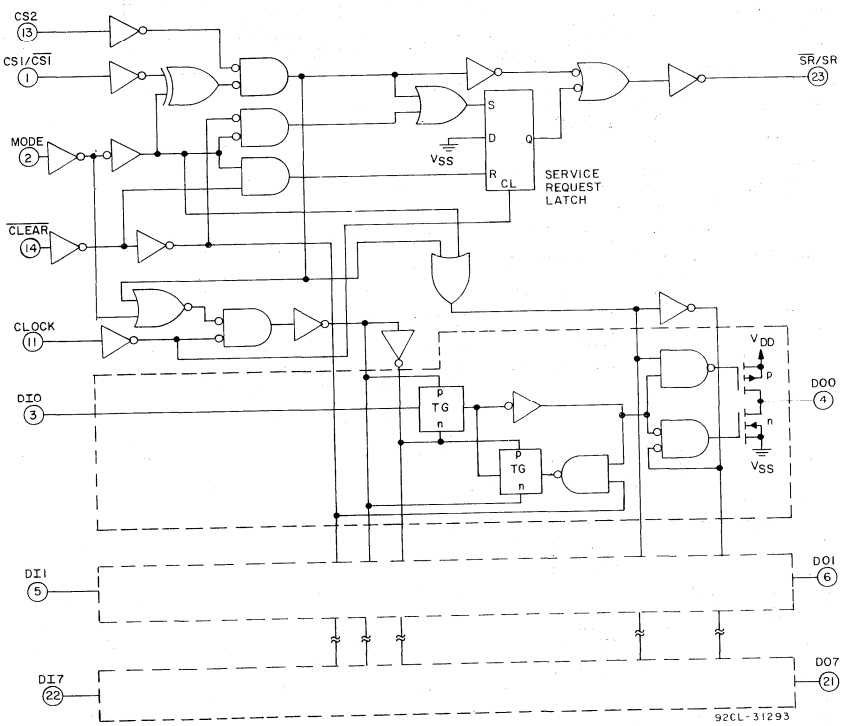


Fig. 2 – CDP1852 logic diagram.

CDP1852, CDP1852C Types

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1852		CDP1852C		
	Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852			CDP1852C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	–	0,5	5	–	–	100	–	–	500	µA
	–	0,10	10	–	–	500	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	3	6	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0,10	10	−3	−6	–	–	–	–	
Output Voltage Low-Level V_{OL}▲	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage HighLevel, V_{OH}	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Current, I_{IN}	–	0,5	5	–	–	±1	–	–	±1	µA
	–	0,10	10	–	–	±2	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	–	±1	–	–	±1	µA
	0,10	0,10	10	–	–	±2	–	–	–	
Operating Current, I_{DD1}#	–	0,5	5	–	130	200	–	150	200	µA
	–	0,10	10	–	400	600	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	5	7.5	–	–	–	

* Typical values are for T_A = 25°C and nominal V_{DD}.

▲ I_{OL} = I_{OH} = 1 µA

\# Operating current is measured at 2 MHz in an 1800 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA, ---- .

CDP1852, CDP1852C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} = ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, and 1 TTL Load
LIMITS AT V_{DD} = 10 V APPLY TO THE CDP1852 ONLY

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
MODE 0 – Input Port					
Required Select Pulse Width, t_{SW}	5	–	180	360	ns
	10	–	90	180	
Required Write Pulse Width, t_{WW}	5	–	90	180	
	10	–	45	90	
Required Clear Pulse Width, t_{CLR}	5	–	80	160	
	10	–	40	80	
Required Data Setup Time, t_{SD}	5	–	−10	0	
	10	–	−5	0	
Required Data Hold Time, t_{DH}	5	–	75	150	
	10	–	35	75	
Data Out Hold Time, t_{DOH}▲	5	30	185	370	
	10	15	100	200	
SR Output Transition Time	5	–	30	60	
	10	–	15	30	
Data Output Transition Time	5	–	30	60	
	10	–	15	30	
Propagation Delay Times, t_{PLH}, t_{PHL}: Select to Data Out▲	5	30	185	370	
	10	15	100	200	
Clear to SR	5	–	170	340	
	10	–	85	170	
Clock to SR	5	–	110	220	
	10	–	55	110	
Select to SR	5	–	120	240	
	10	–	60	120	
MODE 1 – Input Port					
Required Clock Pulse Width, t_{CL}	5	–	130	260	ns
	10	–	65	130	
Required Write Pulse Width, t_{WW}	5	–	130	260	
	10	–	65	130	
Required Clear Pulse Width, t_{CLR}	5	–	60	120	
	10	–	30	60	
Required Data Setup Time, t_{DS}	5	–	−10	0	
	10	–	−5	0	
Required Data Hold Time, t_{DH}	5	–	75	150	
	10	–	35	75	
Required Clock-after-Select Hold Time	5	–	−10	0	
	10	–	−5	0	
SR Output Transition Time	5	–	30	60	
	10	–	15	30	
Data Output Transition Time	5	–	30	60	
	10	–	15	30	

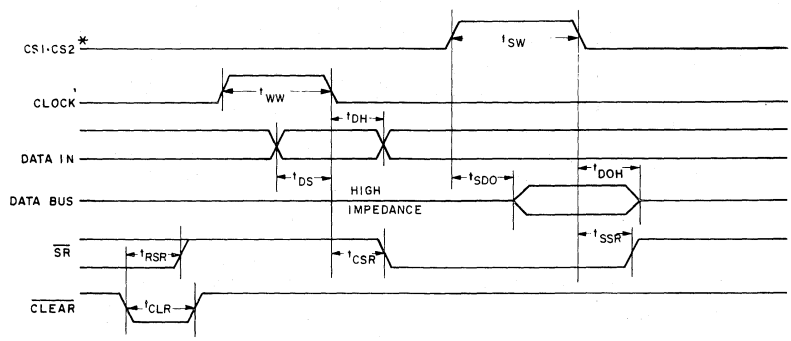
▲ Minimum value is measured from CS2; maximum value is measured from CS1.
* Typical values are for T_A = 25°C and nominal V_{DD}.

CDP1852, CDP1852C Types

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
Propagation Delay Times, t_{PLH}, t_{PHL}:					
Clear to Data Out	5	–	140	280	ns
	10	–	70	140	
Write to Data Out	5	–	220	440	
	10	–	110	220	
Data In to Data Out	5	–	100	200	
	10	–	50	100	
Clear to SR	5	–	120	240	
	10	–	60	120	
Clock to SR	5	–	120	240	
	10	–	60	120	
Select to SR	5	–	120	240	
	10	–	60	120	

* Typical values are for $T_A = 25^\circ C$ and nominal V_{DD}.



* CS1·CS2 IS THE OVERLAP OF CS1=1 AND CS2=1

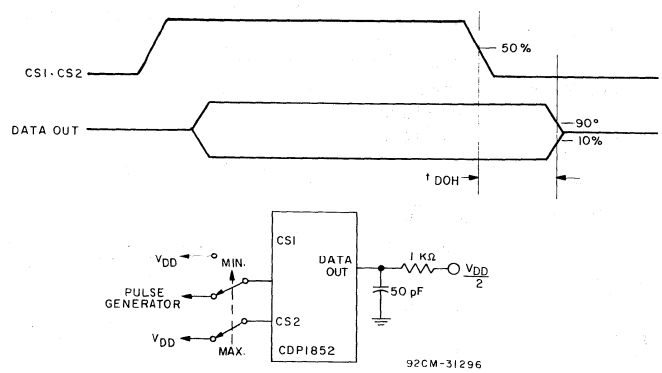
INPUTS			OUTPUTS	
CLOCK	CS1·CS2†	CLEAR	DATA OUT	SR OUT
X	0	0	HIGH Z	1
X	0	1	HIGH Z	SR LATCH•
0	1	0	0	0
0	1	1	DATA LATCH	0
1	1	X	DATA IN	0

INPUTS			OUTPUTS
CLOCK	CS1·CS2†	CLEAR	SR LATCH•
X	X	0	1
X	1	X	1
↓	0	1	0
↑	0	1	NO CHANGE

† CS1·CS2 = 1 ⇒ CS1 = 1 and CS2 = 1.
• SR Latch is internal to the device (See Fig. 2).

92CM-31292

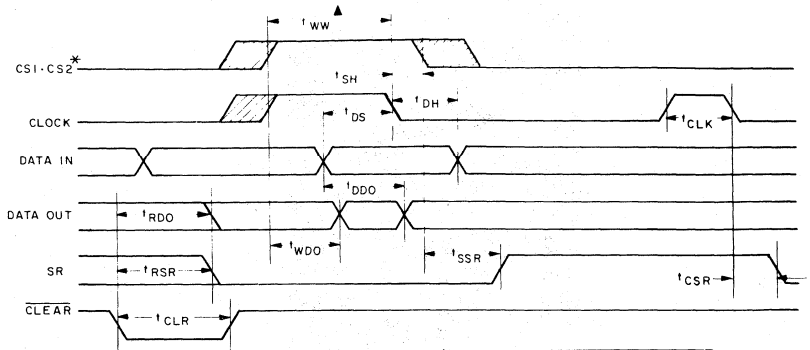
Fig. 3 – MODE 0 input port timing diagram and truth tables.



92CM-31296

Fig. 4 – Data out hold time waveforms and test circuit.

CDP1852, CDP1852C Types



* CS1·CS2 IS THE OVERLAP OF $\overline{CS1}$ = 0 AND CS2 = 1
▲ WRITE IS THE OVERLAP OF CS1·CS2 AND CLOCK

INPUTS			OUTPUTS	
CLOCK	CS1·CS2†	$\overline{CLEAR}$	DATA OUT	SR OUT
0	X	0	0	0
1	0	0	0	0
X	0	1	DATA LATCH	SR LATCH•
0	1	1	DATA LATCH	0
1	1	X	DATA IN	0

INPUTS			OUTPUT
CLOCK	CS1·CS2†	$\overline{CLEAR}$	SR LATCH•
X	X	0	0
X	1	1	1
↓	0	1	0
↑	0	1	NO CHANGE

† CS1·CS2 = 1 when CS1 = 0 and CS2 = 1.
• SR Latch is internal to the device (see Fig. 2).

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Fig. 5 – MODE 1 input port timing diagram and truth tables.

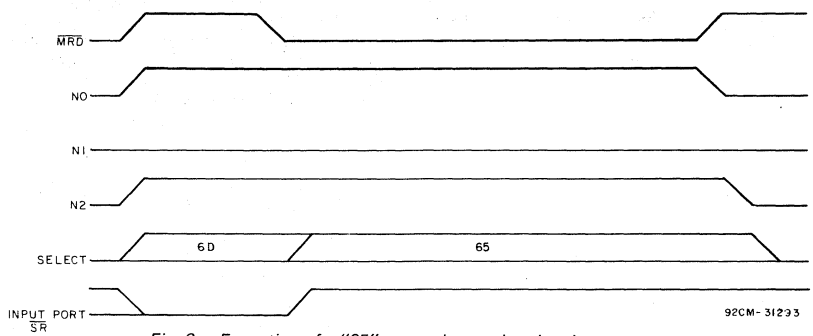
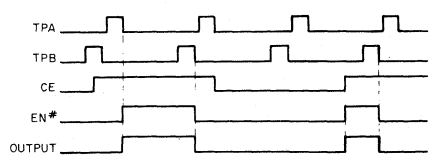


Fig. 6 – Execution of a "65" output instruction showing momentary selection of input port "D".

Application Information

In a CDP1802- or CDP1804-based system where MRD is used to distinguish between INP and OUT instructions, and INP instruction is assumed to occur at the beginning of every I/O cycle because MRD starts high. Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device will be selected for a short time (see Fig. 6). This condition forces SR low and resets the SR latch (see Fig. 2).



* OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY (SEE FIG. 1)

92CS-29024

Fig. 7 CDP1853 timing diagram.

In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems.

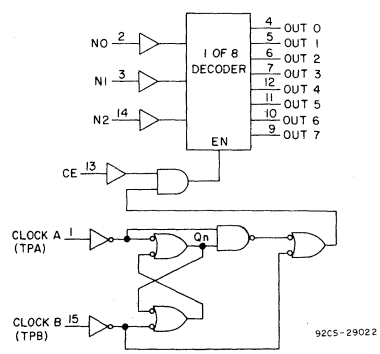
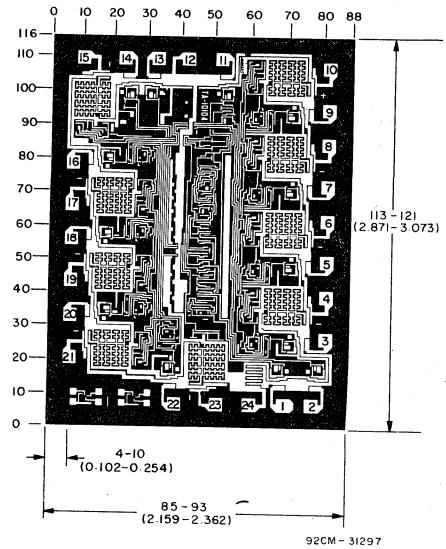


Fig. 8 – CDP1853 functional diagram.

CDP1852, CDP1852C Types



Dimensions and pad layout for CDP1852H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

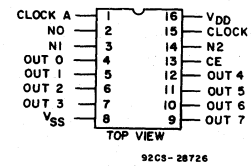
The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1853, CDP1853C Types

N-Bit 1of 8 Decoder

Features:

- Static Silicon-Gate CMOS circuitry — CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Low quiescent and operating power
- Provides direct control of up to 7 input and 7 output devices
- CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems
- Single voltage supply
- Full military temperature range (−55 to +125°C)



TERMINAL ASSIGNMENT

The RCA-CDP1853 and CDP1853C are 1 of 8 decoders designed for use in CDP1800-series microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1853C has a recommended operating voltage range of 4 to 6.5 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not selected (CE = 0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to CDP1802 or CDP1804 microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

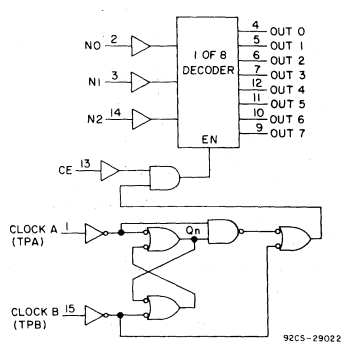


Fig. 1 — CDP1853 functional diagram.

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level 0 = Low level X = Don't care

*Qn-1 = Enable remains in previous state.

CDP1853, CDP1853C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal
CDP1853 ..... −0.5 to + 11 V
CDP1853C ..... −0.5 to + 7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) ..... −55 to + 125°C
PLASTIC PACKAGES (E SUFFIX TYPES) ..... −40 to + 85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to + 150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59±0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C. Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1853			CDP1853C			
	VO (V)	VIN (V)	VDD (V)	Min.	Typ.†	Max.	Min.	Typ.†	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	10	–	5	50	μA
	–	–	10	–	10	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source Current) I_{OH}	4.6	0,5	5	-1.15	-2.3	–	-1.15	-2.3	–	mA
	9.5	0,10	10	-2.6	-5.2	–	–	–	–	
Output Voltage Low-Level ▲ V_{OL}	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current I_{IN}	Any Input	0,5	5	–	–	±1	–	–	±1	μA
		0,10	10	–	–	±1	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	–	±1	–	–	±1	μA
	0,10	0,10	10	–	–	±1	–	–	–	
Operating Current I_{DD1}*	0,5	0,5	5	–	50	100	–	50	100	μA
	0,10	0,10	10	–	150	300	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance C_{OUT}	–	–	–	–	10	15	–	10	15	pF

† Typical values are for T_A = 25°C and nominal voltage.
* Operating current measured in a CDP1802 system at 2MHz with outputs floating.
▲ $I_{OL} = I_{OH} = 1\mu A$

CDP1853, CDP1853C Types

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1853		CDP1853C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD}=± 5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, t_r, t_f = 20 ns, C_L = 100pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1853		CDP1853C		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time:						
CE to Output, t_{EOH}, t_{EOL}	5	175	275	175	275	ns
	10	90	150	–	–	
N to Outputs, t_{NOH}, t_{NOL}	5	225	350	225	350	ns
	10	120	200	–	–	
Clock A to Output, t_{AO}	5	200	300	200	300	ns
	10	100	150	–	–	
Clock B to Output, t_{BO}	5	175	275	175	275	ns
	10	90	150	–	–	
Minimum Pulse Widths:						
Clock A, t_{CACA}	5	50	75	50	75	ns
	10	25	50	–	–	
Clock B, t_{CBCB}	5	50	75	50	75	
	10	25	50	–	–	

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: Typical values are for T_A = 25°C and nominal voltages.

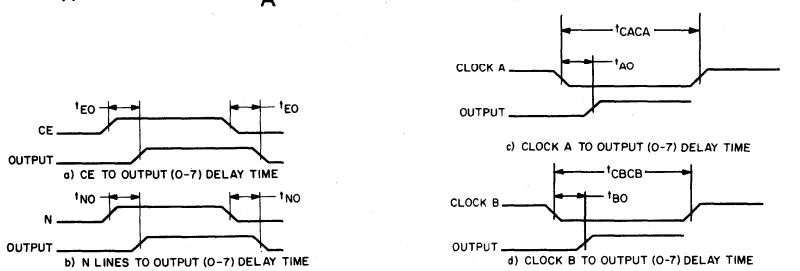


Fig. 2 – Propagation delay time diagrams.

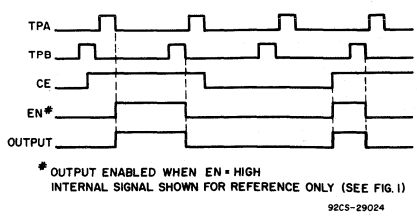


Fig. 3 – Timing diagram.

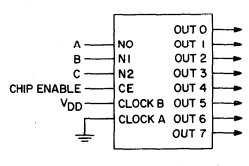


Fig. 4 – N-bit decoder used as a 1 of 8 decoder.

CDP1853, CDP1853C Types

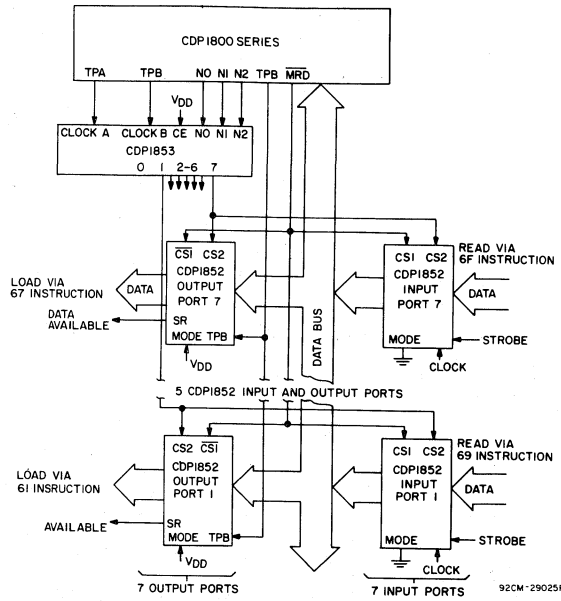


Fig. 5 – N-bit decoder in a one-level I/O system.

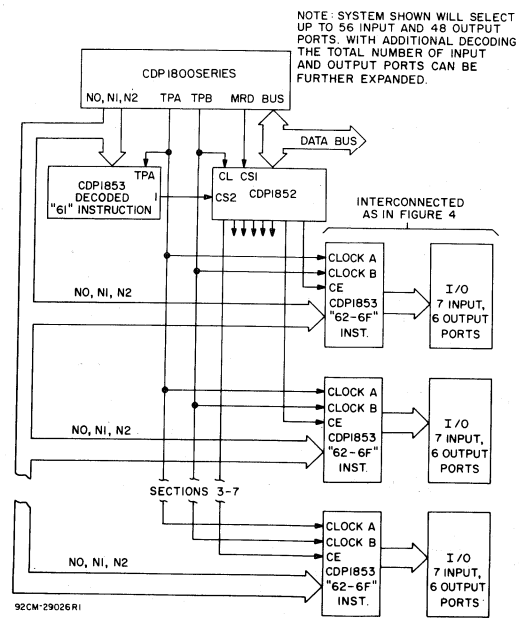


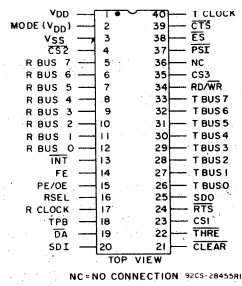
Fig. 6 – Two-level I/O using CDP1853 and CDP1852.

CDP1854A, CDP1854AC Types

COS/MOS Programmable Universal Asynchronous Receiver/Transmitter (UART)

Features:

- Static silicon-gate CMOS circuitry—CD4000 Series compatible
- Two operating modes:
  Mode 0—functionally compatible with industry standard types such as the TR1602A
  Mode 1—interfaces directly with the CDP1802 and CDP1804 microprocessors without additional components
- Full- or half-duplex operation
- Baud rate — DC to 250K bits/sec. (typ.) @ V_{DD} = 5 V
  DC to 500K bits/sec. (typ.) @ V_{DD} = 10 V
- Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits
- False start bit detection
- Parity, framing, and overrun error detection
- Low quiescent and operating power
- Single-voltage supply
- Wide operating-voltage range
- Operating-temperature range: −55 to +125°C (CDP1854AD, CDP1854ACD) −40 to +85°C (CDP1854AE, CDP1854ACE)



MODE 1
Terminal Assignment

The CDP1854A and CDP1854AC are silicon-gate COS/MOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, it can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1802 or CDP1804 parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE = 1), the CDP1854A is directly compatible with the CDP1802 and CDP1804 microprocessor system without additional interface circuitry.

When the mode input is low (MODE = 0), the device is functionally compatible with in-

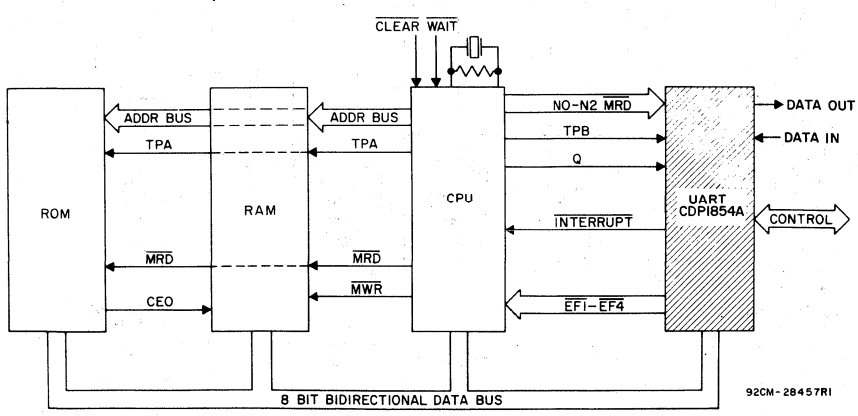


Fig. 1 — Typical CDP1800-series microprocessor system using the CDP1854A.

CDP1854A, CDP1854AC Types

dustry standard UART's such as the TR-1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG} = −12 V supply connection.

The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating-voltage range of 4–10.5 volts, and the CDP1854AC has a recommended operating-voltage range of 4–6.5 volts.

The CDP1854A and CDP1854AC are supplied in hermetic 40-lead dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1854A . . . . . −0.5 to +11 V
CDP1854AC . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to 100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

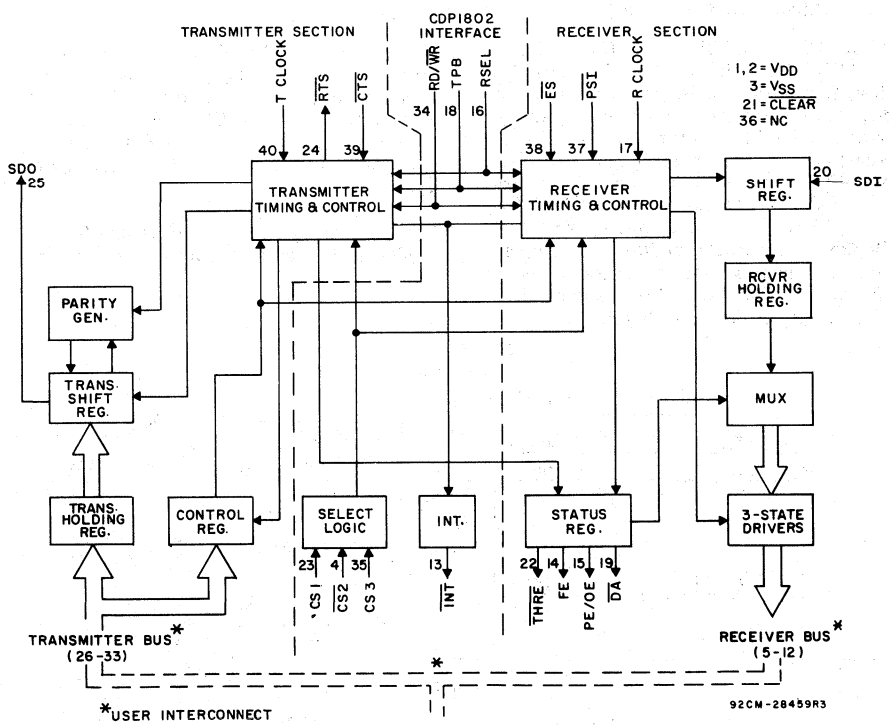


Fig. 2 – MODE 1 block diagram (CDP1802 and CDP1804 compatible).

CDP1854A, CDP1854AC Types

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1854A		CDP1854AC		
	Min.	Max.	Min.	Max.	
DC Operating-Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, unless otherwise noted.

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1854A			CDP1854AC			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	–	0,5	5	–	0.01	50	–	0.02	200	μA
	–	0,10	10	–	1	200	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	0.55	1.1	–	0.55	1.1	–	mA
	0.5	0,10	10	1.3	2.6	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−0.55	−1.1	–	−0.55	−1.1	–	mA
	9.5	0,10	10	−1.3	−2.6	–	–	–	–	
Output Voltage Low-Level V_{OL}▲	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage HighLevel, V_{OH}	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Current, I_{IN}	–	0,5	5	–	$\pm10^{-4}$	±1	–	$\pm10^{-4}$	±1	μA
	–	0,10	10	–	$\pm10^{-4}$	±2	–	–	–	
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	$\pm10^{-4}$	±1	–	$\pm10^{-4}$	±1	μA
	0,10	0,10	10	–	$\pm10^{-4}$	±10	–	–	–	
Operating Current, I_{DD1}#	–	0,5	5	–	1.5	–	–	1.5	–	mA
	–	0,10	10	–	10	–	–	–	–	
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	10	15	

*Typical values are for T_A = 25°C. ▲ $I_{OL} = I_{OH}$ = 1 μA.

Operating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V in a CDP1802 system, with open outputs.

CDP1854A, CDP1854AC Types

CDP1802 COMPATIBLE MODE 1 OPERATION (MODE INPUT = V_{DD})

1. Initialization and Controls

In the CDP1802 and CDP1804 compatible mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/$\overline{WR}$ and RSEL inputs as follows:

TABLE I-Register Selection Summary

RSEL	RD/$\overline{WR}$	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	High	Read Status Register from Receiver Bus

In this mode the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. CDP1802 and CDP1804 I/O control output signals can be connected directly to the CDP1854A inputs as shown in Fig. 3. The $\overline{CLEAR}$ input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus in order to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · CS2 · CS3=1) and the Control Register is designated (RSEL = H, RD/$\overline{WR}$ = L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0-R BUS 7) in order to determine the status of the UART. Some of these status bits are also available at separate terminals as indicated in Fig. 7.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Fig. 6) is set. Loading the Control Register with TR = 1 (bit 7 = high) inhibits changing the other control bits. Therefore two loads are required: one to format the UART, the second to set TR. When TR has been set, a $\overline{TRANSMITTER\ HOLDING\ REGISTER\ EMPTY}$ ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low-level on the $\overline{REQUEST\ TO\ SENT}$ ($\overline{RTS}$) output to the peripheral. It is not necessary to set TR for proper operation for the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 · CS2 · CS3 = 1, and the Holding Register is selected by RSEL = L and RD/$\overline{WR}$ = L. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input, which can be connected to a peripheral device output, goes low, the Transmitter Shift Register will

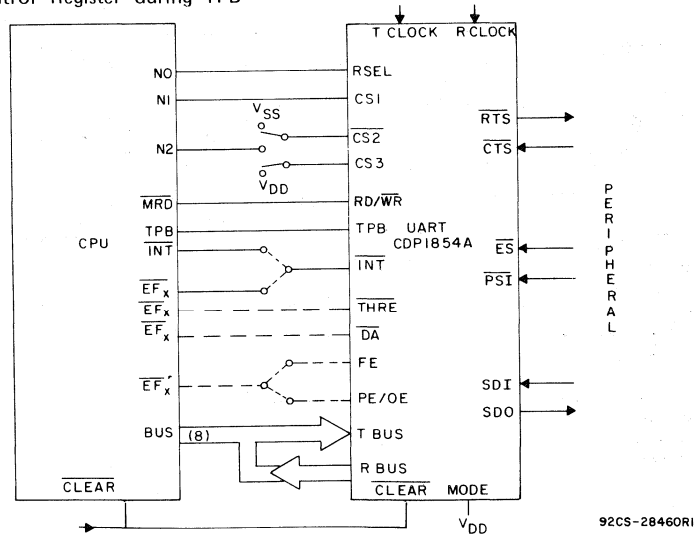


Fig. 3 – CDP1800-series cpu/CDP1854A connection diagram.

be loaded from the Transmitter Holding Register and data transmission will begin. If $\overline{CTS}$ is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB and transmission of a start bit will occur 1/2 clock period later (see Fig. 4). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the transmitter shift register will not be transmitted.

One transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE • TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Fig. 6). SDO is held low until the BREAK bit is reset.

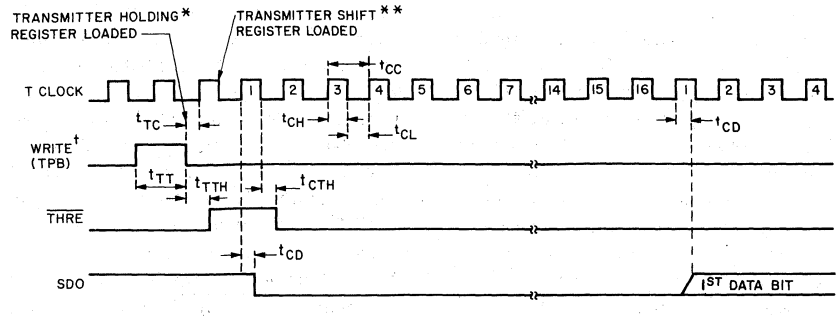
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Figs. 4 and 5.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.●	Max.▲	Typ.●	Max.▲	
Transmitter Timing – MODE 1							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	–	–	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	–	–	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	–	–	
TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	–	–	
Minimum Setup Time: TPB to Clock	t_{TC}	5	175	225	175	225	ns
		10	90	150	–	–	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	–	–	
TPB to $\overline{THRE}$	t_{TTH}	5	200	300	200	300	ns
		10	100	150	–	–	
Clock to $\overline{THRE}$	t_{CTH}	5	200	300	200	300	ns
		10	100	150	–	–	
CPU Interface – WRITE Timing – MODE 1							
Minimum Pulse Width: TPB	t_{TT}	5	100	150	100	150	ns
		10	50	75	–	–	
Minimum Setup Time: RSEL to Write	t_{RSW}	5	50	75	50	75	ns
		10	25	40	–	–	
Data to Write	t_{DW}	5	−100	−75	−100	−75	ns
		10	−50	−35	–	–	
Minimum Hold Time: RSEL after Write	t_{WRS}	5	50	75	50	75	ns
		10	25	40	–	–	
Data after Write	t_{WD}	5	75	125	75	125	ns
		10	40	60	–	–	

●Typical values are for T_A = 25°C and nominal voltages.

▲Maximum limits of minimum characteristics are the values above which all devices function.

CDP1854A, CDP1854AC Types



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB.

** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{TC} AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

† WRITE IS THE OVERLAP OF TPB, CSI, AND CS3 = 1 AND $\overline{CS3}$, RD / $\overline{WR}$ = 0.

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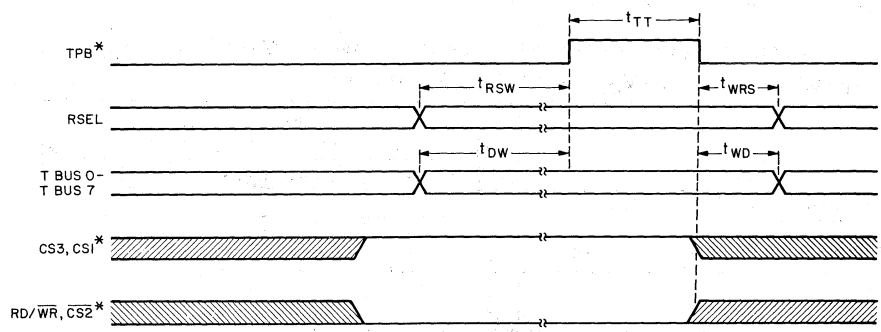
Fig. 4 – Transmitter timing diagram – MODE 1.



* WRITE IS THE OVERLAP OF TPB, CSI, CS3=1 AND $\overline{CS2}$, RD/$\overline{WR}$=0.

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Fig. 5 – MODE 1 cpu interface (WRITE) timing diagram.

CONTROL REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0 PARITY INHIBIT (PI):

When set high parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited the stop bits(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1 EVEN PARITY ENABLE (EPE):

When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2 STOP BIT SELECT (SBS):
See table below.

3 WORD LENGTH SELECT 1 (WLS1):
See table below.

4 WORD LENGTH SELECT 2 (WLS2):
See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SBS	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

Fig. 6 – Control Register bit assignment. *(continued on next page)*

Bit Signal: Function

5 INTERRUPT ENABLE (IE):

When set high $\overline{THRE}$, DA, THRE · TSRE, $\overline{CTS}$, and PSI interrupts are enabled (see Interrupt Conditions, Table II).

6 TRANSMIT BREAK (BREAK):

Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{CLEAR}$ goes low; $\overline{CTS}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros).

7 TRANSMIT REQUEST (TR):

When set high, $\overline{RTS}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{THRE}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops.)

Fig. 6 – Control Register bit assignment. *(continued from page 6)*

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2 in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the Data Available status bit is also set and the $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) and $\overline{INTERRUPT}$ ($\overline{INT}$) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1 · CS2 · CS3 = 1) and RD/$\overline{WR}$ = high. Status can be read when RSEL = high. Data is read when RSEL = low. When reading data, TPB latches data in the microprocessor and resets $\overline{DATA\ AVAILABLE}$ ($\overline{DA}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

STATUS REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	–	–	–	14	15	15	19*

* Polarity reversed at output terminal.

BIT SIGNAL: FUNCTION

0 DATA AVAILABLE (DA):

When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19 but with its polarity reversed.

1 OVERRUN ERROR (OE):

When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal OR'ed with PE is output at Term. 15.

2 PARITY ERROR (PE):

When set high, this bit indicates that the received parity bit does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal OR'ed with OE is output at Term. 15.

Fig. 7 – Status Register bit assignment. *(continued on next page)*

CDP1854A, CDP1854AC Types

BIT SIGNAL: FUNCTION

3 FRAMING ERROR (FE):

When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4 EXTERNAL STATUS (ES):

This bit is set high by a low-level input at Term. 38 ($\overline{ES}$).

5 PERIPHERAL STATUS INTERRUPT (PSI):

This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{PSI}$). The $\overline{INTERRUPT}$ output (Term. 13) is also asserted (INT = low) when this bit is set.

6 TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains set until the start of transmission of the next character.

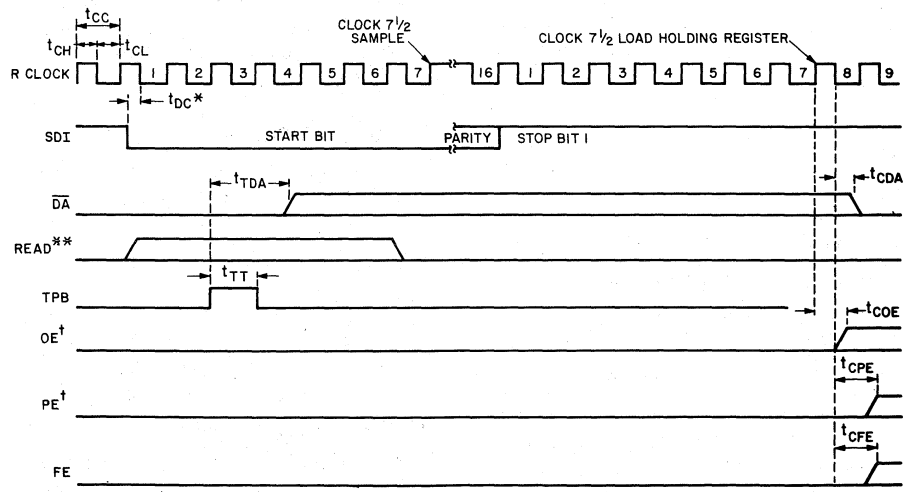
7 TRANSMITTER HOLDING REGISTER EMPTY (THRE):

When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term.22) low and causes an INTERRUPT (INT = low), if TR is high.

Fig. 7 – Status Register bit assignment. *(continued from page 7)*

4. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{REQUEST\ TO\ SENT}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{EXTERNAL\ STATUS}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{PERIPHERAL\ STATUS\ INTERRUPT}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modem $\overline{DATA\ CARRIER\ DETECT}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (See Fig. 7).



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{WR}$ = 1 AND $\overline{CS2}$ = 0. IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

† OE AND PE SHARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER.

Fig. 8 – MODE 1 receiver timing diagram.

CDP1854A, CDP1854AC Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Figs. 8 and 9.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1854A			CDP1854AC			
			Min.	Typ.●	Max.▲	Min.	Typ.●	Max.▲	
Receiver Timing — MODE 1									
Minimum Clock Period	t_{CC}	5	—	250	310	—	250	310	ns
		10	—	125	155	—	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	—	100	125	—	100	125	ns
		10	—	75	100	—	—	—	
Clock High Level	t_{CH}	5	—	100	125	—	100	125	ns
		10	—	75	100	—	—	—	
TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Propagation Delay Time: TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	—	220	325	—	220	325	ns
		10	—	110	175	—	—	—	
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	—	220	325	—	220	325	ns
		10	—	110	175	—	—	—	
Clock to Overrun Error	t_{COE}	5	—	210	300	—	210	300	ns
		10	—	105	150	—	—	—	
Clock to Parity Error	t_{CPE}	5	—	240	375	—	240	375	ns
		10	—	120	175	—	—	—	
Clock to Framing Error	t_{CFE}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
CPU Interface — READ Timing — MODE 1									
Minimum Pulse Width: TPB	t_{TT}	5	—	100	150	—	100	150	ns
		10	—	50	75	—	—	—	
Minimum Setup Time: RSEL to TPB	t_{RST}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Hold Time: RSEL after TPB	t_{TRS}	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Read to Data Access Time	t_{RDDA}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
Read to Data Valid Time	t_{RDV}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
RSEL to Data Valid Time	t_{RSDV}	5	—	150	225	—	150	225	ns
		10	—	75	125	—	—	—	
Hold Time: Data after Read	t_{RDM}	5	50	150	—	50	150	—	ns
		10	25	75	—	—	—	—	

● Typical values are for T_A = 25°C and nominal voltages.

▲ Maximum limits of minimum characteristics are the values above which all devices function.

CDP1854A, CDP1854AC Types

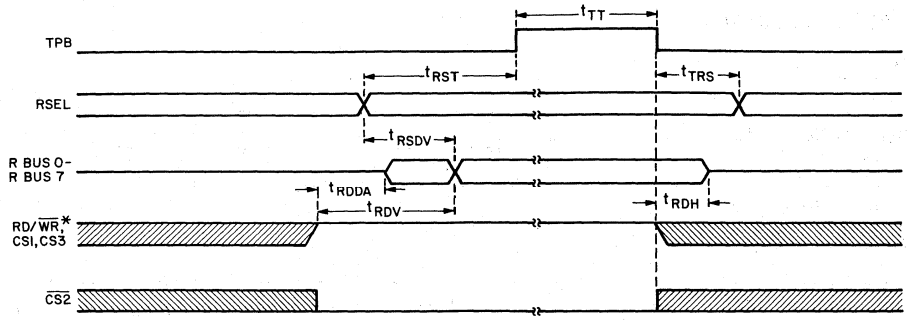


Fig. 9 – MODE 1 cpu interface (READ) timing diagram.

TABLE II – Interrupt Set and Reset Conditions

SET* (INT = LOW)	RESET (INT = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
PSI (Negative edge)	Read of status	TPB trailing edge
CTS (Positive edge when THRE · TSRE	Read of status	TPB leading edge

*Interrupts will occur only after the IE bit in the Control Register (see Fig. 6) has been set.
▲THRE will cause an interrupt only after the TR bit in the Control Register (see Fig. 6) has been set.

FUNCTIONAL DEFINITIONS FOR CDP1854A TERMINALS – CDP1802 and CDP1804 COMPATIBLE – MODE 1

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage

MODE SELECT (MODE):
A high-level voltage at this input selects CDP1802 and CDP1804 Mode operation.

V_{SS}:
Ground

CHIP SELECT 2 (CS2):
A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals).

INTERRUPT (INT):
A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table 2.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):
A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Fig. 7).

REGISTER SELECT (RSEL):
This input is used to choose either the Control/Status Registers (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table 1.

CDP1854A, CDP1854AC Types

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

TPB:
A positive input pulse used as a data load or reset strobe.

DATA AVAILABLE ($\overline{DA}$):
A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

CLEAR ($\overline{CLEAR}$):
A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

TRANSMITTER HOLDING REGISTER EMPTY ($\overline{THRE}$):
A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):
A high-level voltage at this input together with $\overline{CS2}$ and CS3 selects the UART.

REQUEST TO SEND ($\overline{RTS}$):
This output signal tells the peripheral to to get ready to receive data. CLEAR TO SEND ($\overline{CTS}$) is the response from the peripheral. $\overline{RTS}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop bit(s) are serially shifted out on this output. When no character is being transmitted, at high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals.

RD/$\overline{WR}$:
A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 ($\overline{CS3}$):
With high-level voltage at this input together with CS1 and $\overline{CS2}$ selects the UART.

PERIPHERAL STATUS INTERRUPT ($\overline{PSI}$):
A high-to-low transition on this input line sets a bit in the Status Register and causes an INTERRUPT ($\overline{INT}$ = low).

EXTERNAL STATUS ($\overline{ES}$):
A low-level voltage at this input sets a bit in the Status Register.

CLEAR TO SEND ($\overline{CTS}$):
When this input from peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

STANDARD MODE 0 OPERATION (MODE INPUT = V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected together. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

CDP1854A, CDP1854AC Types

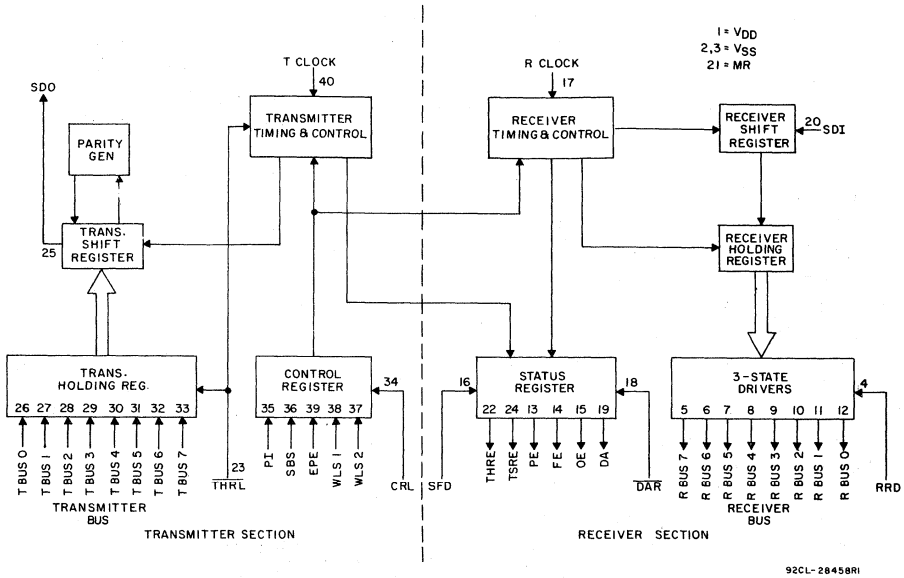


Fig. 10 – Standard Mode 0 block diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Fig. 11.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.●	Max.▲	Typ.●	Max.▲	
Standard Timing – MODE 0							
Minimum Pulse Width: CRL	t_{CRL}	5 10	100 50	150 75	100 –	150 –	ns
Minimum Setup Time: Control Word to CRL	t_{CWC}	5 10	200 100	300 150	200 –	300 –	ns
Minimum Hold Time: Control Word after CRL	t_{CCW}	5 10	100 50	150 75	100 –	150 –	ns
Propagation Delay Time: SFD High to SOD	t_{SFDH}	5 10	200 100	300 150	200 –	300 –	ns
SFD Low to SOD	t_{SFDL}	5 10	75 40	120 60	75 –	120 –	ns
RRD High to Receiver Register High Impedance	t_{RRDH}	5 10	200 100	300 150	200 –	300 –	ns
RRD Low to Receiver Register Active	t_{RRDL}	5 10	100 50	150 75	100 –	150 –	ns

●Typical values are for T_A = 25°C and nominal voltages.

▲Maximum limits of minimum characteristics are the values above which all devices function.

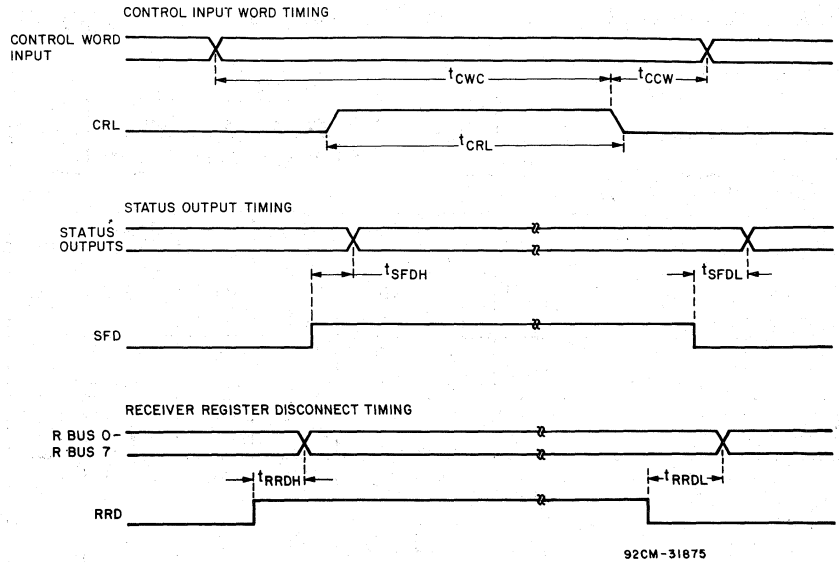


Fig. 11 – Standard MODE 0 timing diagram.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 13. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter Holding Register by applying a low pulse to the TRANSMITTER HOLDING REGISTER LOAD ($\overline{THRL}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 12. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f_{CLOCK}.

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length

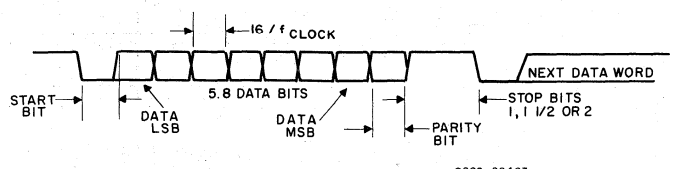


Fig. 12 – Serial data word format.

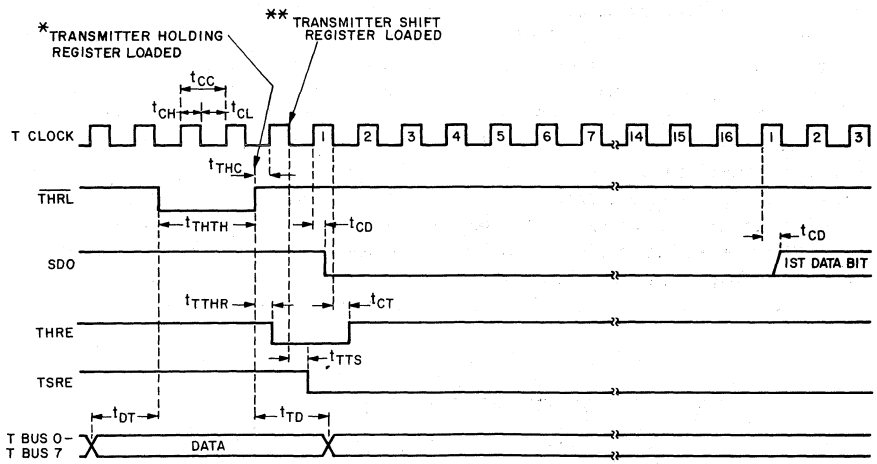
CDP1854A, CDP1854AC Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Fig. 13.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.●	Max.▲	Typ.●	Max.▲	
Transmitter Timing – MODE 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	–	–	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	–	–	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	–	–	
$\overline{THRL}$	t_{THTH}	5	100	150	100	150	ns
		10	50	75	–	–	
Minimum Setup Time: $\overline{THRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	–	–	
Data to $\overline{THRL}$	t_{DT}	5	−100	−75	−100	−75	ns
		10	−50	−35	–	–	
Minimum Hold Time: Data after $\overline{THRL}$	t_{TD}	5	75	125	75	125	ns
		10	40	60	–	–	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	–	–	
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	–	–	
$\overline{THRL}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	–	–	
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	–	–	

●Typical values are for T_A = 25°C and nominal voltages.

▲Maximum limits of minimum characteristics are the values above which all devices function.



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{THRL}$.

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD+t_{THC} AFTER THE TRAILING EDGE OF $\overline{THRL}$, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

Fig. 13 – MODE 0 transmitter timing diagram.

CDP1854A, CDP1854AC Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Fig. 14.

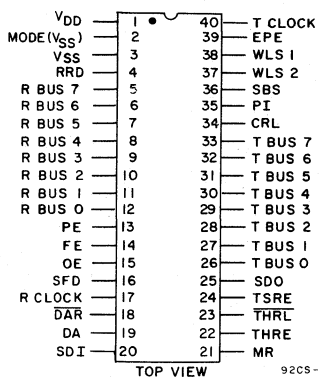
CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.●	Max.▲	Typ.●	Max.▲	
Receiver Timing – MODE 0							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 –	310 –	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 –	125 –	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 –	125 –	ns
$\overline{\text{DATA AVAILABLE RESET}}$	t_{DD}	5 10	50 25	75 40	50 –	75 –	ns
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5 10	100 50	150 75	100 –	150 –	ns
Propagation Delay Time: $\overline{\text{DATA AVAILABLE RESET}}$ to Data Available	t_{DDA}	5 10	150 75	225 125	150 –	225 –	ns
Clock to Data Valid	t_{CDV}	5 10	225 110	325 175	225 –	325 –	ns
Clock to Data Available	t_{CDA}	5 10	225 110	325 175	225 –	325 –	ns
Clock to Overrun Error	t_{COE}	5 10	210 100	300 150	210 –	300 –	ns
Clock to Parity Error	t_{CPE}	5 10	240 120	375 175	240 –	375 –	ns
Clock to Framing Error	t_{CFE}	5 10	200 100	300 150	200 –	300 –	ns

● Typical values are for T_A = 25°C and nominal voltages.

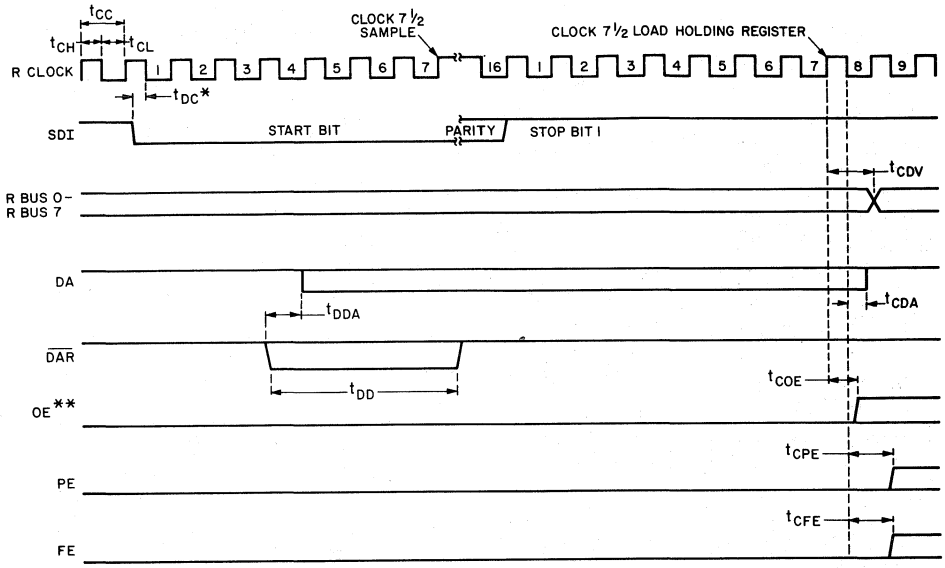
▲Maximum limits of minimum characteristics are the values above which all devices function.

is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significan bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0-R BUS 7) outputs. Applying a negative pulse to the $\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 14.

MODE 0
Terminal Assignment



CDP1854A, CDP1854AC Types



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

92CM-31877

Fig. 14 – MODE 0 receiver timing diagram.

FUNCTIONAL DEFINITIONS FOR CDP1854A TERMINALS – STANDARD MODE 0

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage.

MODE SELECT (MODE):
A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:
Ground.

RECEIVER REGISTER DISCONNECT (RRD):
A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS R BUS 7-R BUS 0):
Receiver parallel data outputs.

PARITY ERROR (PE):
A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register, PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT SFD) line.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):
A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):
A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

CDP1854A, CDP1854AC Types

DATA AVAILABLE RESET ($\overline{\text{DAR}}$):
A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):
A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIÁL DATA IN (SDI):
Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):
A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):
A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

TRANSMITTER HOLDING REGISTER LOAD ($\overline{\text{THRL}}$):
A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop (bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0-T BUS 7):
Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):
A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):
A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):
This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

WORD LENGTH SELECT 2 (WLS2):
WORD LENGTH SELECT 1 (WLS1):
These two inputs select the character length (exclusive or parity) as follows:

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):
A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

CDP1855, CDP1855C Types

8-Bit Programmable Multiply/Divide Unit

Preliminary Data

Features:

- **Cascadable up to 4 units for 32-bit by 32-bit multiply or 64 ÷ 32 bit divide**
- **8-bit by 8-bit multiply or 16 ÷ 8 bit divide in 5 μs at 5 V or 2.5 μs at 10 V typical**
- **Low power, static CMOS circuitry**
- **Single, non-critical voltage supply**
- **Direct interface to CDP1802 and CDP1804 microprocessors**
- **Easy interface to general 8-bit microprocessors**
- **Significantly increases throughput of microprocessor used for arithmetic calculations**

The RCA-CDP1855 and CDP1855C are 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiply or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1802 and CDP1804 microprocessors via the n-lines and can easily be configured to fit in either the memory or I/O space of generalized 8-bit microprocessors.

The multiply/divide unit is based on a method of multiplying by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

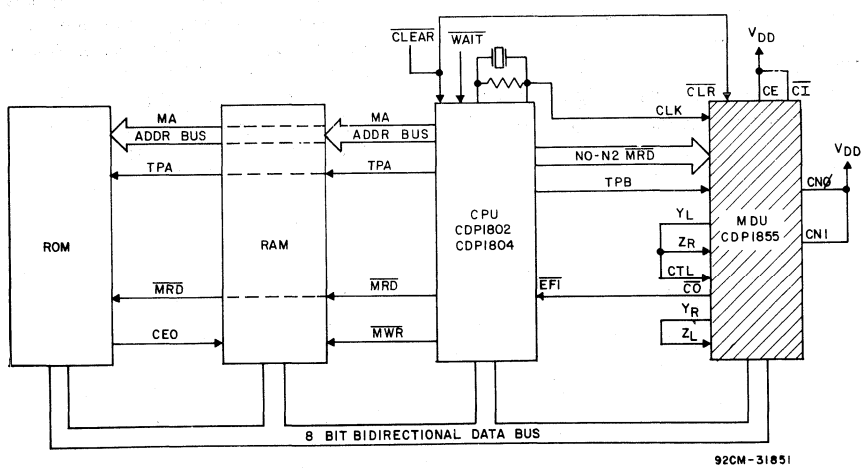


Fig. 1 – Typical 1800 system with CDP1855.

CDP1855, CDP1855C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal)
- CDP1855 . . . . . −0.5 to +11 V
- CDP1855C . . . . . −0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
- For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
- For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
- For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR T_A = FULL PACKAGE-TEMPERATURE RANGE . . . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A)
- PACKAGE TYPE D . . . . . −55 to +125°C
- PACKAGE TYPE E . . . . . −40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

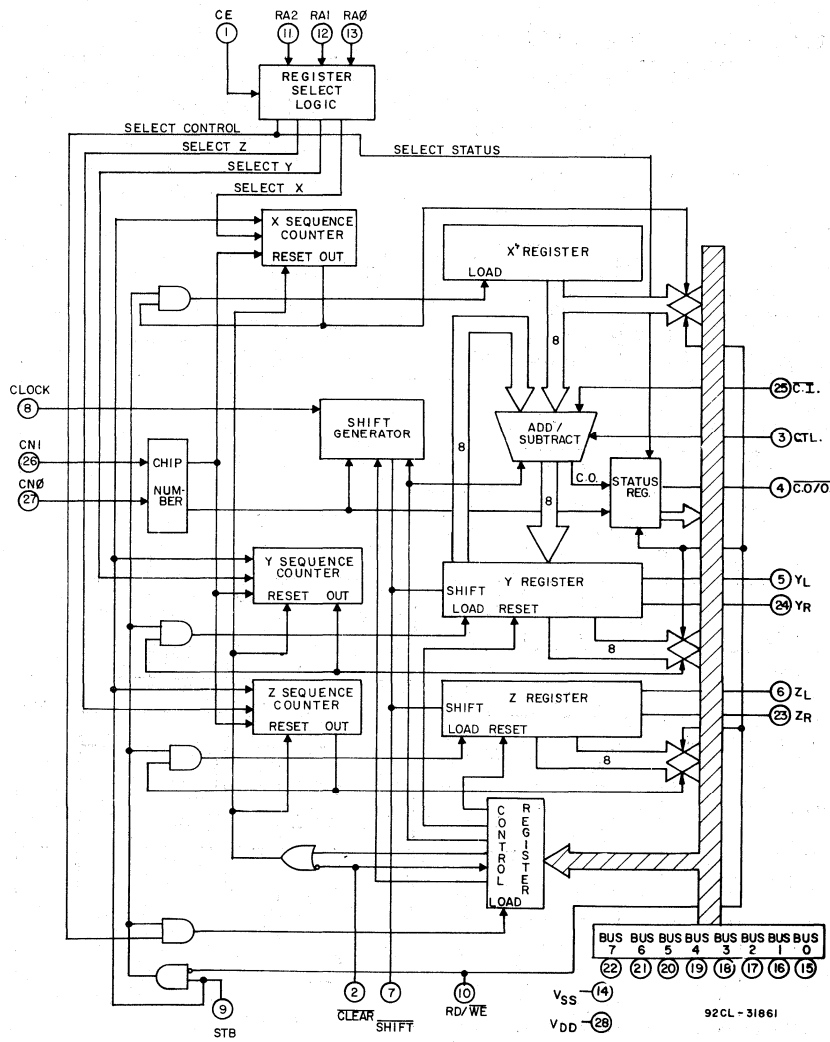


Fig. 2 – Block diagram of CDP1855 and CDP1855C.

CDP1855, CDP1855C Types

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4 – 10.5 volts, and the CDP1855C, a recommended operating voltage range of 4 – 6.5 volts.

The CDP1855 and CDP1855C types are supplied in a 28-lead hermetic dual-in-line ceramic package (D suffix) and in a 28-lead dual-in-line plastic package (E suffix).

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, nominal operating conditons should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1855		CDP1855C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1855			CDP1855C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	–	0.01	50	–	0.02	200	μA
	–	0,10	10	–	1	200	–	–	–	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	2.6	5.2	–	–	–	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	1.15	2.3	–	1.15	2.3	–	
	9.5	0,10	10	2.6	5.2	–	–	–	–	
Output Voltage:** Low-Level, V_{OL} Max.	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage:** High-Level, V_{OH} Min.	–	0,5	5	4.9	5	–	4.9	5	–	
	–	0,10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	–	–	1.5	–	–	1.5	
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	–	3.5	–	3.5	–	–	
	0.5,9.5	–	10	–	7	–	–	–	–	
Input Current, I_{IN} Max.	–	0,5	5	–	$\pm 10^{-4}$	±1	–	$\pm 10^{-4}$	±1	μA
	–	0,10	10	–	$\pm 10^{-4}$	±1	–	–	–	
3-State Output Leakage Current, I_{OUT} Max.	0,5	0,5	5	–	–	±15	–	–	±15	
	0,10	0,10	10	–	–	±15	–	–	–	
Operating Current, I_{DD}***	–	0,5	5	–	2	5	–	2	5	mA
	–	0,10	10	–	4	10	–	–	–	
Input Capacitance, C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	–	15	

*Typical values are for T_A = 25°C and nominal voltage.

**I_{OL} = I_{OH} = 1 μA.

***Operating current is measured at 2 MHz with open outputs.

CDP1855, CDP1855C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%
t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 5 and 6)

CHARACTERISTIC●	V_{DD} (V)	LIMITS CDP1855 Min.	CDP1855 Typ.*	CDP1855 Max.	CDP1855C Min.	CDP1855C Typ.*	CDP1855C Max.	UNITS
Write Cycle								
Minimum Clear Pulse Width $t_{\overline{CLR}}$	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Minimum Write Pulse Width t_{WW}	5	–	150	225	–	150	225	
	10	–	75	115	–	–	–	
Minimum Data-In Setup t_{DSU}	5	–	–75	0	–	–75	0	
	10	–	–40	0	–	–	–	
Minimum Data-In-Hold t_{DH}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Minimum Address to Write Setup t_{ASU}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Minimum Address after Write Hold t_{AH}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Read Cycle								
CE to Data Out Active t_{CDO}	5	–	200	300	–	200	300	ns
	10	–	100	150	–	–	–	
CE to Data Access t_{CA}	5	–	300	450	–	300	450	
	10	–	150	225	–	–	–	
Address to Data Access t_{AA}	5	–	300	450	–	300	450	
	10	–	150	225	–	–	–	
Data Out Hold after CE t_{DOH}	5	50	150	225	50	150	225	
	10	25	75	115	–	–	–	
Data Out Hold after Read t_{DOH}	5	50	150	225	50	150	225	
	10	25	75	115	–	–	–	
Read to Data Out Active t_{RDO}	5	–	200	300	–	200	300	
	10	–	100	150	–	–	–	
Read to Data Access t_{RA}	5	–	200	300	–	200	300	
	10	–	100	150	–	–	–	
Strobe to Data Access t_{SA}	5	50	200	300	50	200	300	
	10	25	100	150	–	–	–	
Minimum Strobe Width t_{SW}	5	–	150	225	–	150	225	
	10	–	75	115	–	–	–	
Operation Timing								
Maximum Clock Frequency+	5	3	4	–	3	4	–	MHz
	10	6	8	–	–	–	–	
Maximum Shift Frequency (1 Device)▲	5	1.5	2	–	1.5	2	–	
	10	3	4	–	–	–	–	
Minimum Clock Width t_{CLK0}, t_{CLK1}	5	–	100	150	–	100	150	ns
	10	–	50	75	–	–	–	

●Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25°C and nominal voltages.

+Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.

▲Shift period for cascading of devices is increased by an amount equal to the C.O. to C.I. Prop. Delay for each device added.

CDP1855, CDP1855C Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5%

t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Figs. 5 and 6) (Cont'd)

CHARACTERISTIC•	V_{DD} (V)	LIMITS						UNITS
		CDP1855			CDP1855C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Operation Timing (cont'd)								
Minimum Clock Period t_{CLK}	5	–	250	333	–	250	333	ns
	10	–	125	167	–	–	–	
Clock to Shift Prop. Delay t_{CSH}	5	–	200	300	–	200	300	
	10	–	100	150	–	–	–	
Minimum C.I. to Shift Setup t_{SU}	5	–	50	67	–	50	67	
	10	–	25	33	–	–	–	
C.O. from Shift Prog. Delay t_{PLH} t_{PHL}	5	–	450	600	–	450	600	
	10	–	225	300	–	–	–	
Minimum. C.I. from Shift Hold t_H	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Minimum Register Input Setup t_{SU}	5	–	−20	10	–	−20	10	
	10	–	−10	10	–	–	–	
Register after Shift Prop. Delay t_{PLH} t_{PHL}	5	–	400	600	–	400	600	
	10	–	200	300	–	–	–	
Minimum Register after Shift Hold t_H	5	–	50	100	–	50	100	
	10	–	25	50	–	–	–	
C.O. from C.I. Prop. Delay t_{PLH} t_{PHL}	5	–	100	150	–	100	150	
	10	–	50	75	–	–	–	
Register from C.I. Prop. Delay t_{PLH} t_{PHL}	5	–	80	120	–	80	120	
	10	–	40	60	–	–	–	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25°C and nominal voltages.

CONTROL TRUTH TABLE

INPUTS*						RESPONSE
CE	RA2 (N2)	RA1 (N1)	RA0 (N0)	RD/$\overline{WE}$ (MRD)	STB (TPB)	
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

* ( ) = 1800 system signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

CDP1855, CDP1855C Types

CONTROL REGISTER AND STATUS REGISTER BIT ASSIGNMENT TABLE

Control Register Bit Assignment

Bus 1	Bus 0	
LOW	HIGH	Multiply
HIGH	LOW	Divide
LOW	LOW	No operation (other than resets caused by bits 2, 3,6)
HIGH	HIGH	Illegal state

Bus 2 = HIGH ⇒ Reset Z register before operation

Bus 3 = HIGH ⇒ Reset Y register before operation

Bus 5	Bus 4	
HIGH	HIGH	One CDP1855
HIGH	LOW	Two CDP1855's
LOW	HIGH	Three CDP1855's
LOW	LOW	Four CDP1855's

Bus 6 = HIGH ⇒ Reset sequence counters

Bus 7 = { LOW ⇒ Shift Rate = Clock Frequency
HIGH ⇒ Select Shift Rate Options:
One CDP1855 ⇒ Shift = Clock ÷ 2
Two CDP1855's ⇒ Shift = Clock ÷ 4
Three or Four CDP1855's ⇒ Shift = Clock ÷ 8

Status Byte

Bit	7	6	5	4	3	2	1	0
Output	0	0	0	0	0	0	0	O.F.

O.F. = 1 if overflow (only valid after a divide has been done)

FUNCTIONAL DESCRIPTION

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Fig. 8). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding an 8N-bit result plus and 8N-bit remainder. The multipy is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represents the number of cascaded CDP1855's and can be 1,2,3, or 4. All operations require 8N + 1 shift pulses.

The CDP1855 contains three registers, X,Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide. There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER AND STATUS REGISTER BIT ASSIGNMENT TABLE". The register address lines (RA0-RA1) are used to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (see "Control truth table").

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (see "CONTROL REGISTER AND STATUS REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (see "CONTROL REGISTER AND STATUS REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

OPERATION

1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the Y_L, Y_R and Y_L, Z_R terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (see "CONTROL REGISTER AND STATUS REGISTER BIT ASSIGNMENT TABLE").

CDP1855, CDP1855C Types

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X,Y, and Z registers can be loaded as defined in the "TRUTH CONTROL TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Successive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described. Resetting the sequence counters selects the most significant MDU. In a four–MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again. In all other configurations (1,2, or 3 MDU's), the sequence counter must be reset prior to each series or register reads or writes.

2. Divide Operation (Fig. 3)

For the divide operation, the divisor is loaded in the X register. The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and the Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{\text{C.O./O.F.}}$ of the most significant MDU and can also be determined by reading the status byte.

The overflow indicator will be set at the start of a divide operation if the resultant will exceed the size of the Z register (8N bits).

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

3. Multiply Operation (Fig. 4)

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers. The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed.

The original contents of the Y register are added to the product of X and Z. Bit 3 of the control word will reset register Y to 0 if desired.

	Before Divide	After Divide
Register X	$3C_{16}$	$3C_{16}$
Register Y	01_{16}	03_{16}
Register Z	$6B_{16}$	06_{16}

Fig. 3 – Divide example.

	Before Multiply	After Multiply
Register X	$3C_{16}$	$3C_{16}$
Register Y	03_{16}	01_{16}
Register Z	06_{16}	$6B_{16}$

Fig. 4 – Multiply example.

Programming Example

For a 24-bit x 24-bit multiply using the system shown in Figure 7, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$:

```
MEMORY LOCATION  OP CODE  LINE NO.  LEVEL 1 ASSEMBLY LANGUAGE
0000             F830;     0001     LDI  #30
0002             A2;       0002     PLO  R2      . .LOAD 30 INTO R2.0
0003             F800;     0003     LDI  #00
0005             B2;       0004     PHI  R2      . .LOAD 00 INTO R2.1 (R2 = 0030)
0006             6750;     0005     OUT  7,#50   . .LOAD CONTROL REGISTERS
                                                    SPECIFYING
0008             ;         0006                  . .THREE MDU's AND RESETTING
                                                    THE
0008             ;         0007                  . .SEQUENCE COUNTERS
0008             6420;     0008     OUT  4,#20   . .LOAD MSB OF X REGISTER
                                                    WITH 20
000A             641F;     0009     OUT  4,#1F   . .LOAD NEXT MSB OF X REG
                                                    WITH 1F
000C             647C;     0010     OUT  4,#7C   . .LOAD LSB OF X REGISTER
                                                    WITH 7C;
000E             ;         0011                  . .X REGISTER CONTAINS #201F7C
```

CDP1855, CDP1855C Types

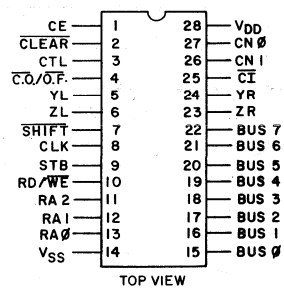
Programming Example (continued)

MEMORY LOCATION	OP CODE	LINE NO.	LEVEL 1 ASSEMBLY LANGUAGE
000E	6572;	0012	OUT 5,=72 . .LOAD MSB OF Z REGISTER WITH 72
0010	653C;	0013	OUT 5,=3C . .LOAD NEXT MSB OF Z REG WITH 3C
0012	6509;	0014	OUT 5,=09 . .LOAD LSB OF Z REGISTER WITH 09;
0014	;	0015	. .Z REGISTER CONTAINS #723C09
0014	6759;	0016	OUT 7,=59 . .LOAD CONTROL REGISTERS RESETTING
0016	;	0017	. .Y REGISTERS AND SEQUENCE COUNTERS
0016	;	0018	. .AND STARTING MULTIPLY OPERATION
0016	E2;	0019	SEX R2
0017	6E60;	0020	INP 6; IRX . .MSB OF RESULTS IS STORED AT
0019	;	0021	. .LOCATION 0030
0019	6E60;	0022	INP 6; IRX
001B	6E60;	0023	INP 6; IRX
001D	6D60;	0024	INP 5; IRX
001F	6D60;	0025	INP 5; IRX
0021	6D;	0026	INP 5; . .COMPLETE LOADING RESULT INTO
0022	;	0027	. .MEMORY LOCATIONS 0030 TO 0035
0022	;	0028	. .RESULTS = 0E558DBA2B5C
0022	3022;	0029	STOP BR STOP

The result of $201F7C_{16} \times 723C09_{16}$ is $0E558DBA2B5C = 15760612797276_{10}$. It will be stored in memory as follows:

LOC	BYTE
0030	0E
31	55
32	8D
33	BA
34	2B
35	5C

TERMINAL ASSIGNMENTS



TOP VIEW

92CS-29965R2

CDP1855, CDP1855C Types

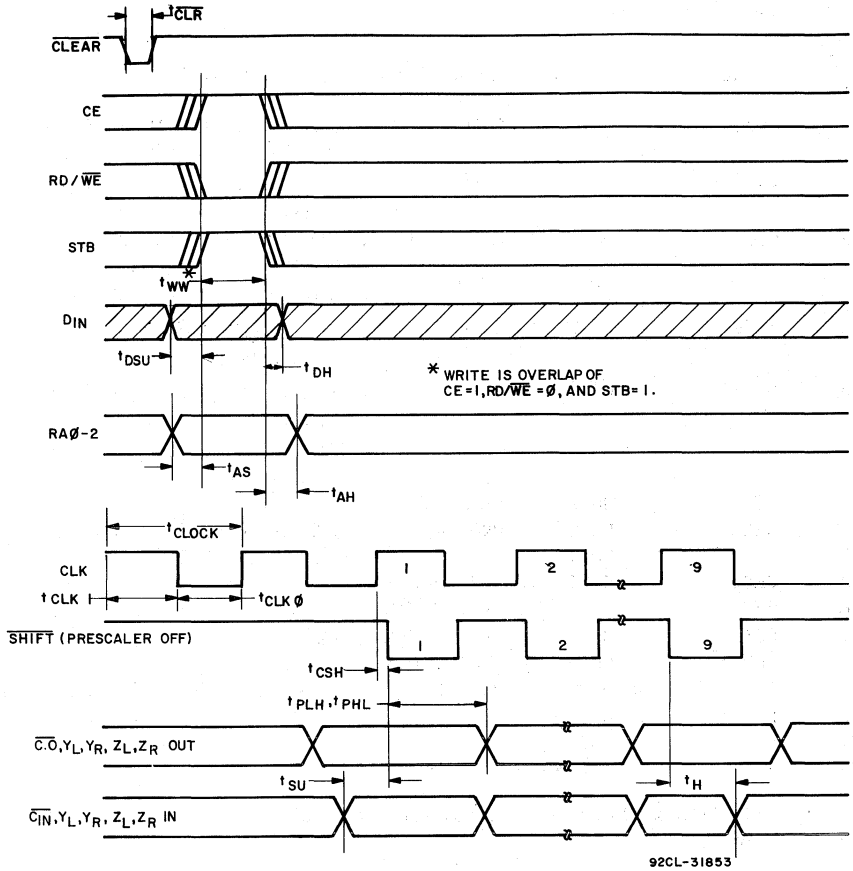


Fig. 5 – Write timing and operation timing.

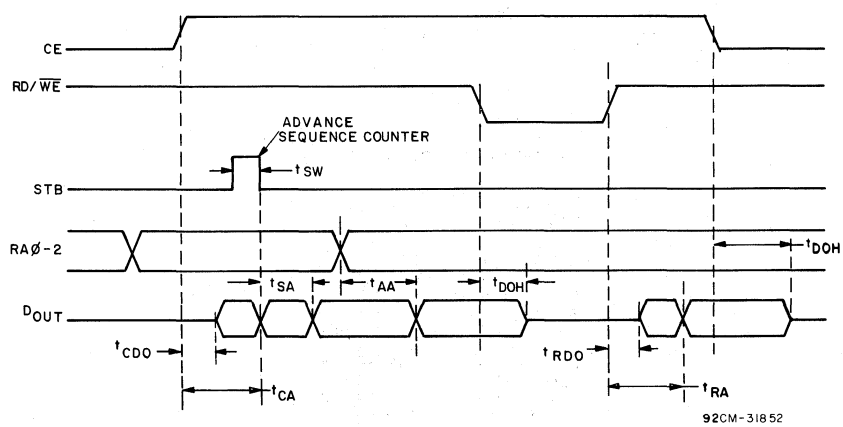


Fig. 6 – Read timing.

CDP1855, CDP1855C Types

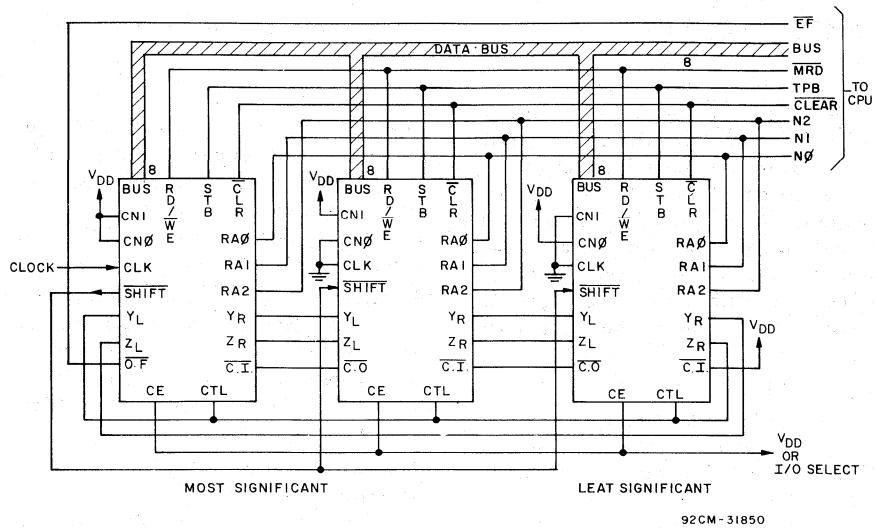


Fig. 7 — Cascading three MDU's (CDP1855) in an 1800 system with MDU's being accessed as I/O ports.

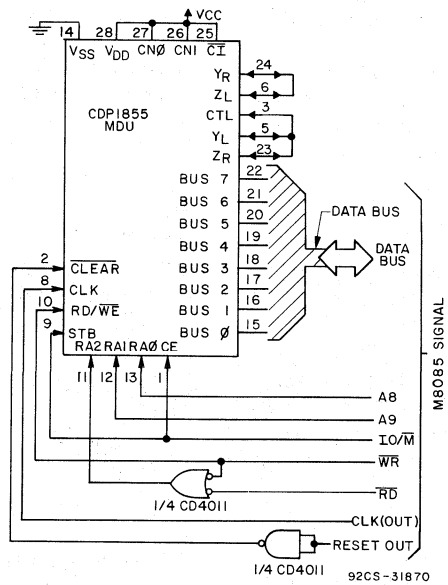


Fig. 8 — Interfacing the CDP1855 to an M8085 microprocessor as an I/O device.

FUNCTIONAL DESCRIPTION OF CDP1855 TERMINALS

CE - CHIP ENABLE (Input):
A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the tristate $\overline{C.O.}/\overline{O.F.}$ output of the most significant MDU.

$\overline{\text{CLEAR}}$ (Input):
The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL - CONTROL (Input):
This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant CDP1855 MDU and to the Z_R of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

CDP1855, CDP1855C Types

$\overline{C.O./O.F.}$ - $\overline{CARRY\ OUT/OVER\ FLOW}$ (Output):
This is a tristate output pin. It is the CDP1855 $\overline{Carry\ Out}$ signal and is connected to $\overline{CI}$ ($\overline{CARRY\text{-}IN}$) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enable is true. A low on this pin indicates that an overflow has occurred. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R - Y-LEFT, Y-RIGHT:
These are tristate bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The Y_R pin is an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is that the Y_L pin of the most significant CDP1855 MDU must be connected to the Z_R pin of the least significant MDU and to the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tied to the Z_L pin of the most significant MDU.

Z_L, Z_R - Z-LEFT, Z-RIGHT:
These are tristate bi-directional pins for data transfers between the "Z" registers of cascaded MDU's. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. The Z_L pin must be tied to the Y_R pin of the next more significant MDU. An exception is that the Z_L pin of the most signification MDU must be connected to the Y_R pin of the least significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

$\overline{SHIFT}$ - $\overline{SHIFT\ CLOCK}$:
This is a tristate bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All $\overline{SHIFT}$ pins must be connected together for cascaded operation. A maximum of the 8N +1 shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

CLK - CLOCK (Input):
This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

STB - STROBE (Input):
When pin 10 is low data is latched from bus lines on the falling edge of this signal. It may by asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

RD/$\overline{WE}$ - READ/$\overline{WRITE\ ENABLE}$ (Input):
This signal defines whether the selected register is to be read from or written to. In 1800 systems use $\overline{MRD}$ if MDU's are addressed as I/O devices, $\overline{MWR}$ is used if MDU's are addressed as memory devices.

RA2, RA1, RA0 - REGISTER ADDRESS (Input):
These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identical to the $\overline{CE}$ pin, except only CE controls the tristate $\overline{C.O./O.F.}$ on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

V_{SS} - GROUND:
Power supply line.

BUS 0–, BUS 7 - BUS LINES:
Tristate bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

Z_R - Z-RIGHT:
See Pin 6.

Y_R - Y-RIGHT:
See Pin 5.

$\overline{CI}$ - $\overline{CARRY\ IN}$ (Input):
This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high (V_{DD}) on all others it must be connected to the $\overline{CO}$ pin of the next less significant MDU.

CN1, CN0 - CHIP NUMBER (Input):
These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

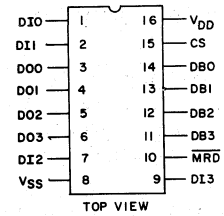
V_{DD} - V^+:
Power supply line.

CDP1856, CDP1857 Types

4-Bit Bus Buffers/Separators

Features:

- **Static Silicon-Gate CMOS circuitry — CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Provides easy connection of memory and I/O devices to CDP1800-series microprocessor data bus.**
- **Single voltage supply**
- **Full military-temperature range of −55°C to +125°C (ceramic package)**
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**

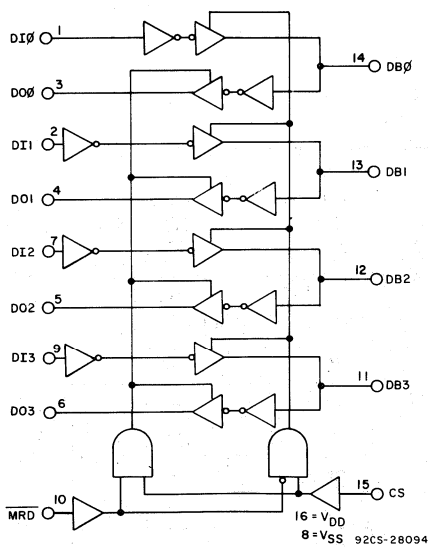


TERMINAL ASSIGNMENT

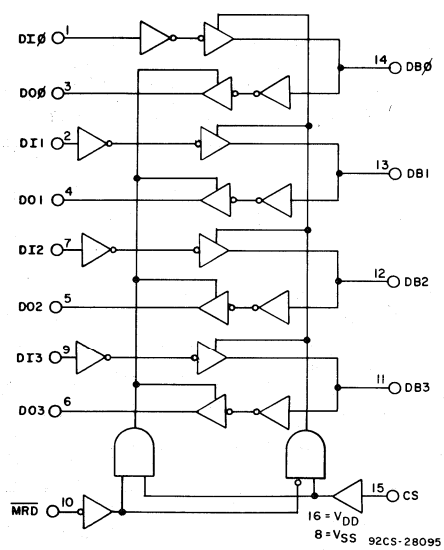
The RCA-CDP1856, CDP1856C, CDP1857, and CDP1857C are 4-bit COS/MOS non-inverting bus separators designed for use in CDP1800-series microprocessor systems. They can be controlled directly by CDP1802 or CDP1804 microprocessor without the use of additional components.

The CDP1856 is designed for use as a bus buffer or separator between the CDP1802 or CDP1804 data bus and memories. The CDP1857 is designed for use as a bus buffer or separator between the CDP1802 or CDP1804 data bus and I/O devices. Both types provide a chip-select (CS) input signal which, when high (1), enables the bus-separator three-state output drivers. The direction of data flow, when enabled, is controlled by the $\overline{MRD}$ input signal.

In the CDP1856, when the $\overline{MRD}$ signal = 0 (low), it enables the three-state bus drivers



CDP1856 — Functional Diagram



CDP1857 — Functional Diagram

CDP1856, CDP1857 Types

(DB0 – DB3) and outputs data from the DATA-IN terminals to the data bus. When $\overline{MRD}$ = 1 (high), it disables the three-state bus drivers and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

In the CDP1857, when $\overline{MRD}$ = 1, it enables the three state bus drivers (DB0-DB3) and transfers data from the DATA-IN lines onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB0-DB3) and enables the three-state data output drivers (DO0-DO3), thus transferring data from the data bus to the DATA-OUT terminals.

The CDP1856 or CDP1857 can be used as a bi-directional bus buffer by connecting the corresponding DI and DO terminals (Fig.2). The $\overline{MRD}$ output signal from the CDP1802 or CDP1804 microprocessor has the correct polarity to control the CDP1856 when this device is used as a memory data bus buffer/separator, or the CDP1857 when it is used as I/O bus buffer/separator. Therefore, the CDP1802 or CDP1804 $\overline{MRD}$ signal can be connected directly to the $\overline{MRD}$ input of either device. See Function Tables 1 and 2 in Fig. 3 for use of the CDP1856 as a memory data bus buffer/separator and CDP1857 as an I/O bus buffer/separator.

The CDP1856 and CDP1857 are functionally identical to the CDP1856C and CDP1857C, respectively. The CDP1856 and CDP1857 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1856C and CDP1857C have a recommended operating-voltage range of 4 to 6.5 volts. The CDP1856 CDP1856C, CDP1857 and CDP1857C are supplied in 16-lead hermetic, dual-in-line ceramic (D suffix) or plastic (E suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1856, CDP1857 . . . . . −0.5 to +11 V
CDP1856C, CDP1857C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) . . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} = ±5%, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, t_r,t_f = 20 ns, C_L = 100 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1856 CDP1857		CDP1856C CDP1857C		
			Typ.	Max.	Typ.	Max.	
Propagation Delay Time: $\overline{MRD}$ or CS to DO,	t_{ED}	5	150	225	150	225	ns
		10	75	125	–	–	
$\overline{MRD}$ or CS to DB,	t_{EB}	5	150	225	150	225	ns
		10	75	125	–	–	
DI to DB,	t_{IB}	5	100	150	100	150	ns
		10	50	75	–	–	
DB to DO	t_{BD}	5	100	150	100	150	ns
		10	50	75	–	–	

Note: Typical values are for TA = 25°C and nominal voltages.

CDP1856, CDP1857 Types

OPERATING CONDITIIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1856 CDP1857		CDP1856C CDP1857C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1856 CDP1857			CDP1856C CDP1857C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.+	Max.	Min.	Typ.+	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	10	–	5	50	μA
	–	–	10	–	10	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source) Current I_{OH}	4.6	0,5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0,10	10	−2.6	−5.2	–	–	–	–	
Output Voltage Low-Level▲ V_{OL}	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage V_{IH}	0.5,9.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Leakage Current, I_{IN}	Any Input	0,5	5	–	–	±1	–	–	±1	μA
		0,10	10	–	–	±1	–	–	–	
Operating Current, I_{DD1}*	0,5	0,5	5	–	50	100	–	50	100	μA
	0,10	0,10	10	–	150	300	–	–	–	
Input Capacitance, C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	10	15	pF

+Typical values are for T_A = 25°C and nominal voltage.

*Operating current measured in a CDP1802 system at 2 MHz with outputs floating.

▲$I_{OL} = I_{OH} = 1$ μA.

CDP1856, CDP1857 Types

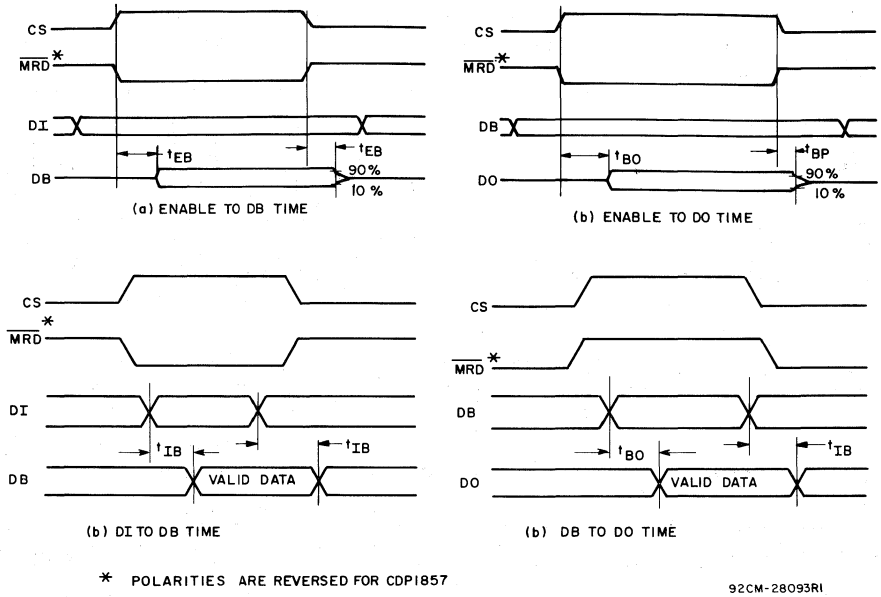


Fig. 1 – Timing Diagrams for CDP1856.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

CDP1856, CDP1857 Types

TYPICAL APPLICATIONS

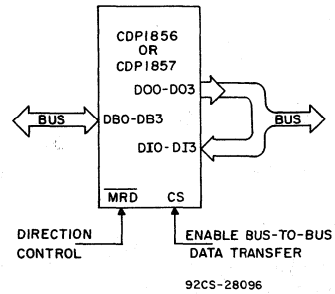
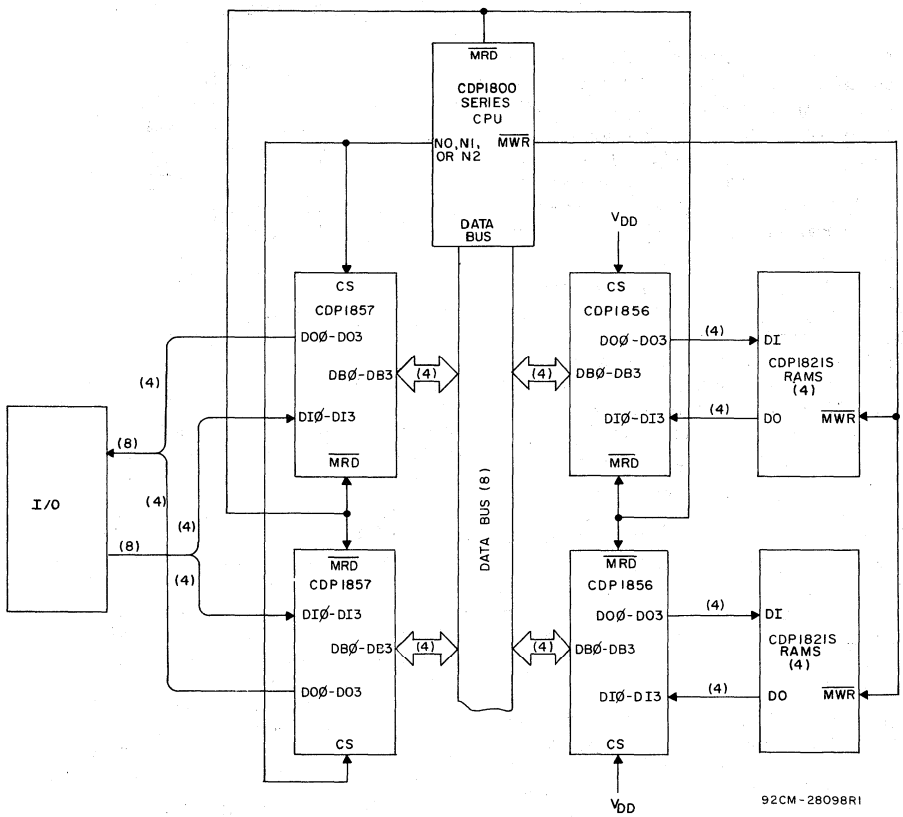


Fig. 2 – CDP1856, CDP1857 Bidirectional Bus Buffer Operation.



CDP1857 FUNCTION TABLE
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

CDP1856 FUNCTION TABLE
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB0 – DB3	DATA OUT DO0 – DO3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

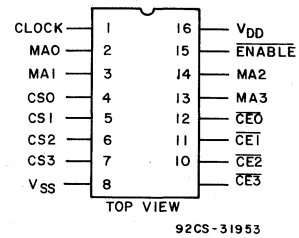
Fig. 3 – CDP1856 and CDP1857 Bus Separator Operation.

CDP1858, CDP1859 Types

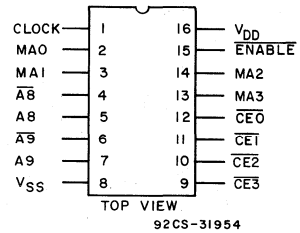
COS/MOS 4-Bit Latch With Decode

Features:

- **Static silicon-gate CMOS circuitry – CD4000-series compatible**
- **Provides easy connection of memory devices to CDP1802 microprocessor**
- **Single voltage supply**
- **Operating temperature range;**
  –55°C to +125°C (ceramic-package types)
  –40°C to +85°C (plastic-package types)
- **Low quiescent and operating power**
- **Non-inverting fully buffered data transfer**



CDP1858
TERMINAL ASSIGNMENT



CDP1859
TERMINAL ASSIGNMENT

RCA-CDP1858, CDP1858C, CDP1859, and CDP1859C are COS/MOS 4-bit latch decode circuits designed for use in CDP1800 series microprocessor systems. These devices have been specifically designed for use as memory-system decoders and interface directly with the CDP1802 or CDP1804 microprocessor multiplexed address bus at maximum clock frequency.

The CDP1858 and CDP1859 are functionally identical to the CDP1858C and CDP-1859C, respectively. The CDP1858 and CDP-1859 have a recommended operating-voltage range of 4 to 10.5 volts, and the CDP1858C and CDP1859C have a recommended operating-voltage range of 4 to 6.5 volts.

The CDP1858 interfaces the CDP1802 or CDP1804 address bus and up to 32 CDP-1822 256 x 4 RAM's to provide a 4K byte RAM system. No additional components are required. The CDP1858 generates the chip selects required by the CDP1822 RAM. The chip select outputs are a function of the address bits connected to inputs MA0 through MA3.

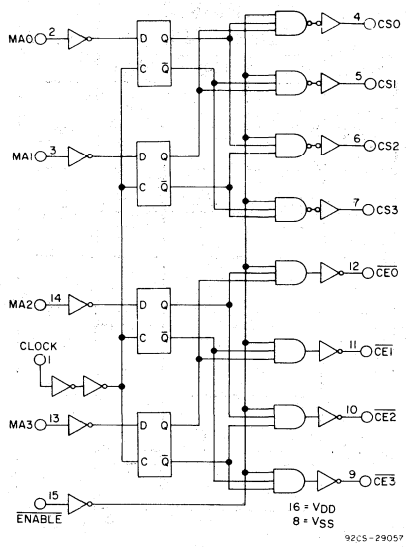
The MA0-MA3 address bits are latched at the trailing edge of TPA (generated by the CDP-1802). When $\overline{\text{ENABLE}}$=1 (V_{DD}), the CS outputs=0 (V_{SS}), and the CE outputs=1. When $\overline{\text{ENABLE}}$=0, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{\text{ENABLE}}$ input can be used for memory system expansion.

The CDP1858 is also compatible with non-multiplexed address bus microprocessors. By connecting the CLOCK input to 1 (V_{DD}), the latches are in the data following mode and the decoded outputs can be used in general-purpose memory-system applications.

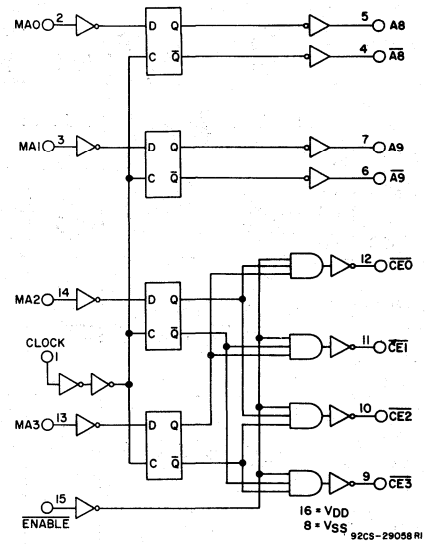
The CDP1859 interfaces the CDP1802 or CDP1804 address bus and up to 32 CDP-1821 1024 x 1 RAM's to provide a 4K byte RAM system. The CDP1859 generates the chip selects required by the CDP1821 RAM. The chip select outputs are a function of the address bits connected to inputs MA2 and MA3. The address bits connected to inputs MA0 and MA1 are latched by the trailing edge of TPA (generated by the CDP1802 or CDP1804) to provide the two additional address lines required by the CDP1821 when used in a CDP1800 series microprocessor-based system. When $\overline{\text{ENABLE}}$=1, the CE outputs are 1's; when $\overline{\text{ENABLE}}$=0, and CE outputs are enabled and correspond to the binary decode of the MA2 and MA3 inputs. $\overline{\text{ENABLE}}$ does not affect the latching or state of outputs A8, $\overline{\text{A8}}$, A9, or $\overline{\text{A9}}$.

CDP1858, CDP1859 Types

The CDP1858, CDP1858C, CDP1859, and CDP1859C are supplied in 16-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).



CDP1858 — Functional diagram.



CDP1859 — Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1858, CDP1859 . . . . . −0.5 to +11 V
CDP1858C, CDP1859C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1858 CDP1859		CDP1858C CDP1859C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

CDP1858, CDP1859 Types

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, Except as Noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1858 CDP1859			CDP1858C CDP1859C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	—	0,5	5	—	0.1	10	—	5	50	μA
	—	0,10	10	—	1	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source Current), I_{OH}	4.6	0,5	5	−1.15	−2.3	—	−1.15	−2.3	—	mA
	9.5	0,10	10	−2.6	−5.2	—	—	—	—	
Output Voltage• Low-Level V_{OL}	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage• High-Level V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	V
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any Input	0,5	5	—	10^{-4}	±1	—	10^{-4}	±1	μA
		0,10	10	—	10^{-4}	±2	—	—	—	
Operating Current, I_{DDI}▲	—	0,5	5	—	50	100	—	50	100	μA
	—	0,10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	—	—	pF

*Tyical values are for $T_A = 25$ °C and nominal voltage.

•$I_{OL} = I_{OH} = 1$ μA.

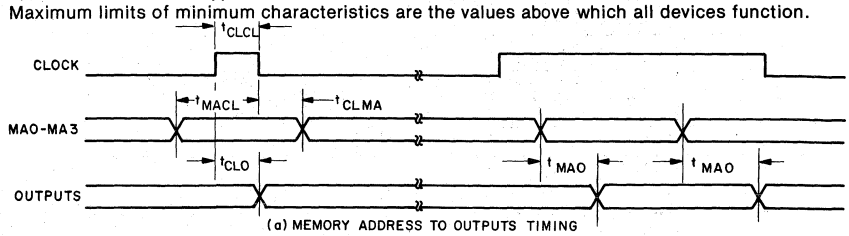
▲Measured in a CDP1802 or CDP1804 system at 2 MHz with open outputs.

CDP1858, CDP1859 Types

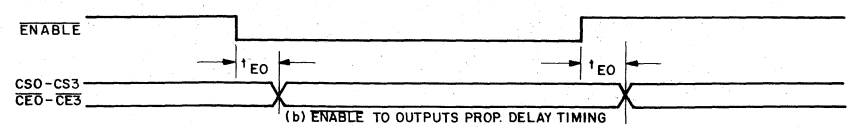
DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85$ °C, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, see Figs. 4 and 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1858			CDP1858C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
	10	—	10	25	—	—	—	
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	5	—	0	25	—	0	25	ns
	10	—	0	10	—	—	—	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
Propagation Delay Times:								
Clock to Outputs, t_{CLO}	5	—	150	225	—	150	225	ns
	10	—	75	125	—	—	—	
Memory Address to Outputs, t_{MAO}	5	—	150	225	—	150	225	
	10	—	75	125	—	—	—	
$\overline{\text{ENABLE}}$ to Outputs, t_{EO}	5	—	125	200	—	125	200	
	10	—	65	100	—	—	—	
		CDP1859			CDP1859C			
Minimum Setup Time, Memory Address to Clock, t_{MACL}	5	—	25	40	—	25	40	ns
	10	—	10	25	—	—	—	
Minimum Hold Time, Memory Address After Clock, t_{CLMA}	5	—	0	25	—	0	25	ns
	10	—	0	10	—	—	—	
Minimum Clock Pulse Width, t_{CLCL}	5	—	50	75	—	50	75	ns
	10	—	25	40	—	—	—	
Propagation Delay Times:								
Clock to Address, t_{CLA}	5	—	125	200	—	125	200	ns
	10	—	65	100	—	—	—	
Clock to $\overline{\text{CHIP ENABLE}}$, t_{CLCE}	5	—	175	275	—	175	275	
	10	—	90	140	—	—	—	
Memory Address to Address, t_{MAA}	5	—	100	150	—	100	150	
	10	—	50	75	—	—	—	
Memory Address to $\overline{\text{CHIP ENABLE}}$, t_{MACE}	5	—	150	225	—	150	225	
	10	—	75	125	—	—	—	
$\overline{\text{ENABLE}}$ to $\overline{\text{CHIP ENABLE}}$, t_{ECE}	5	—	125	200	—	125	200	
	10	—	65	100	—	—	—	

Typical values are for $T_A = 25$ °C and nominal voltages.
Maximum limits of minimum characteristics are the values above which all devices function.



(a) MEMORY ADDRESS TO OUTPUTS TIMING



(b) $\overline{\text{ENABLE}}$ TO OUTPUTS PROP. DELAY TIMING

Fig. 1 – CDP1858 timing diagram.

92CM-31956

CDP1858, CDP1859 Types

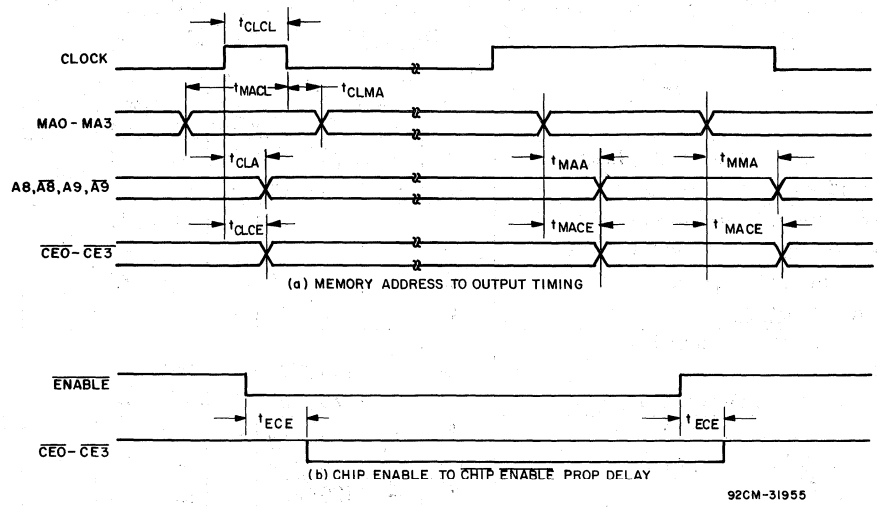


Fig. 2 – CDP1859 timing diagram.

CDP1858 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		CSO	CS1	CS2	CS3	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1859 DECODE TRUTH TABLE

$\overline{ENABLE}$	DATA INPUTS		A8	A9	$\overline{A8}$	$\overline{A9}$	$\overline{CE0}$	$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY $\overline{ENABLE}$				1	1	1	1

X = MA3, MA2, MA1, MA0 DON'T CARE

CDP1858, CDP1859 Types

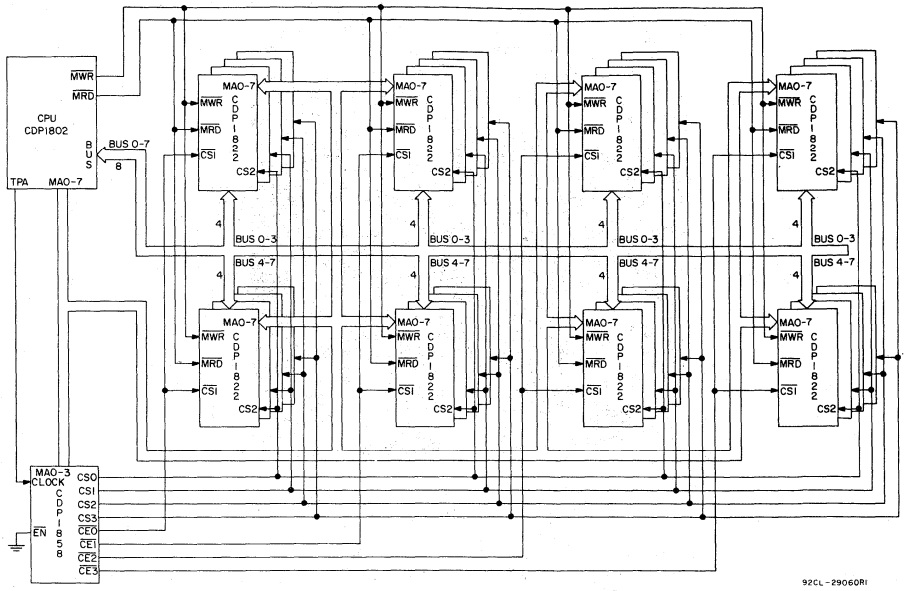


Fig. 3 – 4K byte RAM system using the CDP1858 and CDP1822.

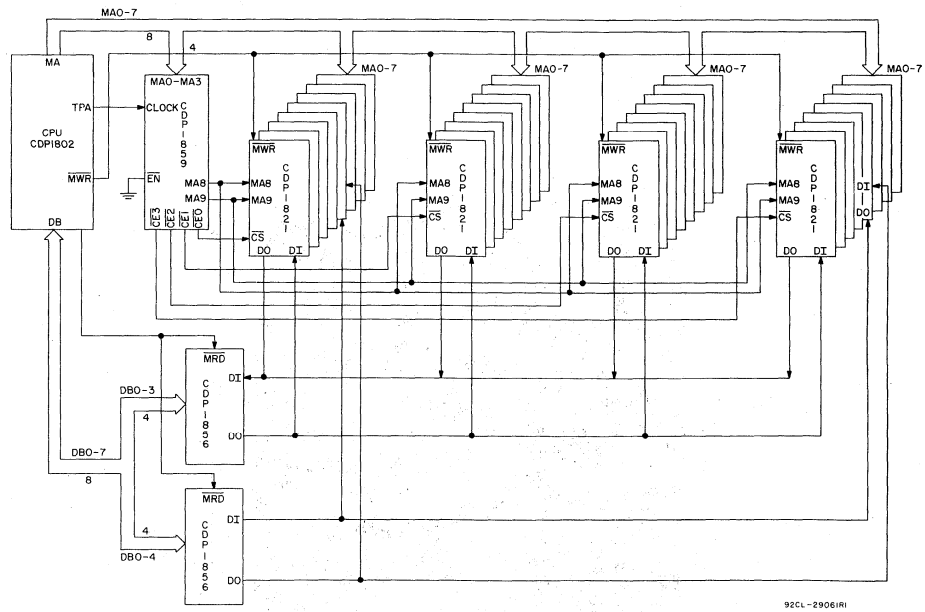
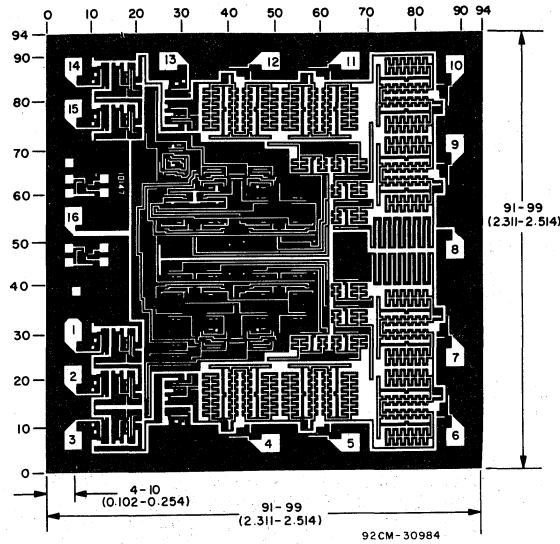


Fig. 4 – 4K byte RAM system using the CDP1859, CDP1856, and CDP1821.

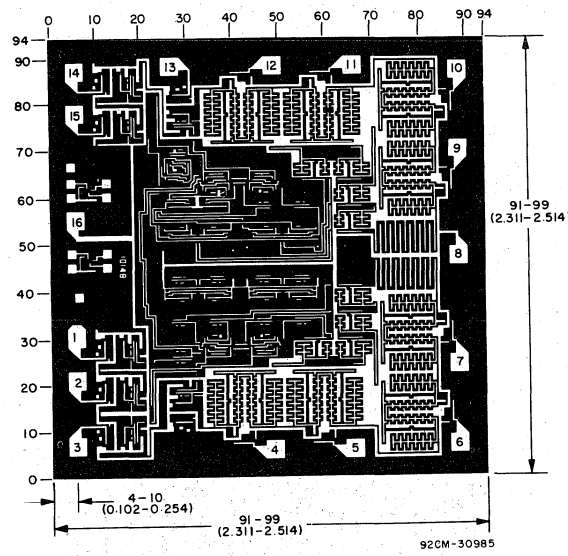
CDP1858, CDP1859 Types



DIMENSIONS AND PAD LAYOUT FOR CDP1858

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



DIMENSIONS AND PAD LAYOUT FOR CDP1859

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CDP1861C
Video Display Controller
Preliminary Data

Features:

- Static silicon-gate CMOS circuitry
- Interfaces directly with CDP1802 microprocessor
- Supports bit-mapped video display for graphic flexibility
- Generates composite horizontal and vertical sync
- Programmable vertical resolution for matrix display of up to 64 x 128 segments
- Real-time interrupt generator
- Clear input
- External display control
- Single voltage supply (4 - 6 volts)
- Low quiescent and operating power
- Full military operating temperature range (−55 to +125°C)

The RCA-CDP1861C is a video display controller designed for use in CDP1800-series microprocessor systems. It is compatible with the CDP1802 microprocessor and will interface directly with the CDP1802 as shown in the system diagram (Fig. 1).

The CDP1861C utilizes many of the features of the CDP1802 to simplify control and minimize the need for external components. The DMA feature of the CDP1802 may be used for direct data transfers from memory to the CDP1861C. The INTERRUPT input and the I/O command lines may be used to perform the necessary handshaking between the CDP1802 and the CDP1861C. Timing may be simplified by operating the microprocessor at a clock frequency of 1.76064-MHz (the standard color frequency of 3.58 MHz, divided by 2, may also be used in some applications). The clock and the CDP1802 timing signals (TPA and TPB) may then be used to set the interface timing as shown in the system diagram. In general, the clock frequency equals the number of fields per second (60), times the number of lines per field (262), times the number of machine cycles per line (14), times the number of bits per byte (8). In DMA operation, each machine cycle is a memory access.

Flexibility in vertical resolution may be obtained by synchronizing the CDP1861C with the CDP1802, and employing direct program control over the DMA process in real time. The actual video display takes place during a "window" of 4.6 milliseconds out of each 16.7-millisecond TV field. Throughout each such display window, a CDP1802 interrupt program may be used to manipulate the DMA pointer, re-issuing a given line of the display several times to save memory storage at the expense of reduced vertical resolution.

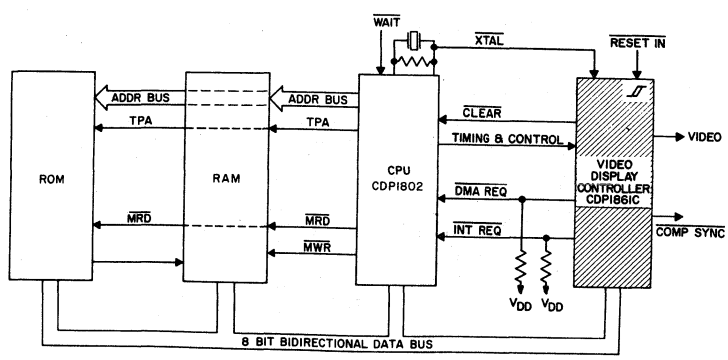


Fig. 1 – Typical CDP1802 microprocessor system.

CDP1861C

The CDP1861C generates composite vertical and horizontal sync plus luminance signals which can be combined externally to create an NTSC compatible composite video signal. This composite vertical and horizontal sync output signal ($\overline{\text{COMP SYNC}}$) is generated from the sync reference (SYNC REF) and LOAD inputs. Vertical sync is derived from horizontal sync by dividing the horizontal sync frequency by 262. The composite sync signal generates timing for a non-interlace video display of 262 lines per field.

The CDP1861C generates an interrupt request ($\overline{\text{INT REQ}}$) once per field, 60 lines after the trailing edge of vertical sync and two lines before the raster has reached a "display window" (see Fig. 5). This request alerts the CDP1802 (or other control system) to prepare for DMA (direct memory access) activity. The CDP1861C DISP STATUS output goes low during the 4 lines before the display window, and again during the last 4 lines of the window. This signal may be used to give early warning of the display window and to release the control system from monitoring the DMA activity.

Beginning in the third machine cycle of each line of the display window, and lasting for 8 cycles, the CDP1861C asserts the $\overline{\text{DMA REQ}}$ output to request a sequence of eight 8-bit bytes, which are then used to generate the $\overline{\text{VIDEO}}$ signal. Then, when control signals A and B are low and high respectively, each assertion of the LOAD input causes the CDP1861C to read a byte from the BUS lines, and immediately to shift it out on the $\overline{\text{VIDEO}}$ output, high-order bit first. A DMA pointer defines an area of memory which is accessed by the CDP1861C to provide a bit-mapped display.

The display on (DISP ON) and display off (DISP OFF) inputs set and reset an internal control flip-flop in the CDP1861C. When this flip-flop is set, $\overline{\text{DMA REQ}}$ and $\overline{\text{INT REQ}}$ are enabled; when reset, they are disabled.

The reset input ($\overline{\text{RESET IN}}$) is a Schmitt trigger input that resets the CDP1861C. The $\overline{\text{CLEAR}}$ output is a conditioned output pulse which can be used to reset the external system.

The CDP1861C is supplied in a 24-lead dual-in-line ceramic package.

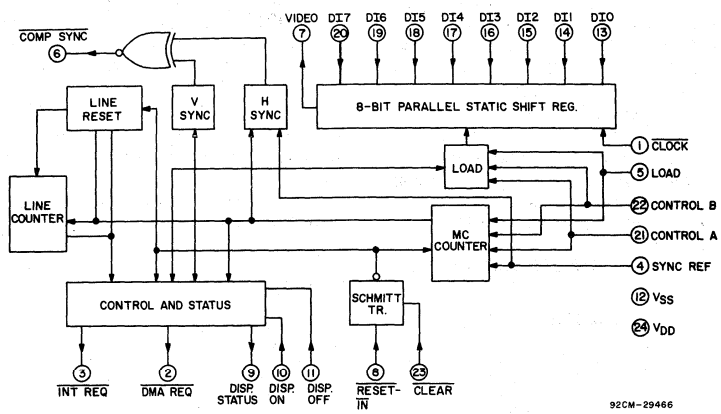
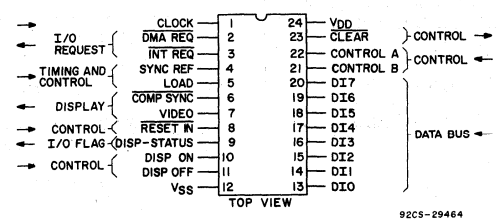


Fig. 2 – CDP1861C block diagram.



TERMINAL ASSIGNMENT

CDP1861C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal) ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = −55°C to +125°C ..... 100 mW
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A) ..... −55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4 - 6	V
Input Voltage Range	–	$V_{SS} - V_{DD}$	V
Input Signal Rise or Fall Time	5	5	μs
Clock Input Frequency, f_{CL}	5	0 - 2.5	MHz

ELECTRICAL CHARACTERISTICS AT T_A = 25 °C

CHARACTERISTIC		CONDITIONS V_O (V)	CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Maximum Quiescent Device Current, I_L		–	5	500	μA
Minimum Output Drive Current:					
Video or Sync	N-Channel (Sink), I_{DN}	0.4	5	1.2	mA
	P-Channel (Source), I_{DP}	4.5	5	1	
Reset Out or Flag	N-Channel (Sink), I_{DN}	0.4	5	−0.4	mA
	P-Channel (Source), I_{DP}	4.5	5	0.4	
I/O Requests;	N-Channel (Sink), I_{DN}	0.4	5	−0.2	mA
Reset-In:					
Positive Trigger Threshold, V_P		–	5	2.5	V
Negative Trigger Threshold, V_N		–	5	1.7	V
Hysteresis Voltage, V_H		–	5	0.8	V

CDP1861C

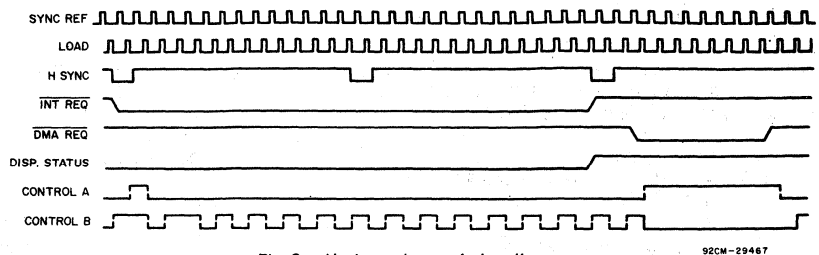


Fig. 3 – Horizontal sync timing diagram.

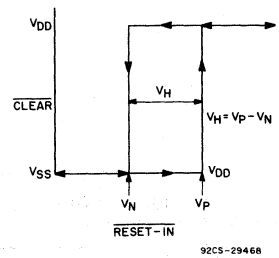


Fig. 4 – Reset transfer characteristics.

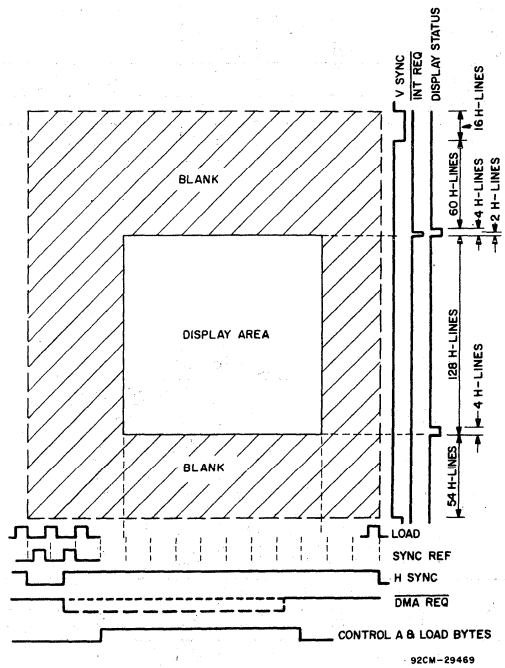


Fig. 5 – Spatial diagram of one video display field (not to scale).

Application Information (CDP1861C directly controlled by the CDP1802 microprocessor)

Figure 6 shows a simple graphic display system using the CDP1802 and the CDP1861C. The CDP1861C uses both the INTERRUPT and direct memory access (DMA) output channel of the microprocessor for display refresh. The microprocessor specifies the area of memory displayed via the interrupt routines, and the DMA output channel is the mechanism which transfers the data from memory to the CDP1861C via the 8-bit data bus. The data are then shifted out one bit at a time at the clock frequency to generate the video ($\overline{\text{VIDEO}}$) signal.

The composite sync (COMP SYNC) signal creates a 262-line-per-field, 60-field-per-second non-interlace video picture. The non-interlaced picture frame for this display consists of two even fields of 262 horizontal lines each. This format differs slightly from the National Television Standard (NTSC) which has a 525-line interlaced picture frame of one odd field and one even field. The vertical sync pulse generated at COMP SYNC of the CDP1861C has no equalizing pulses but is serrated to maintain horizontal synchronization during the vertical blanking time. The VIDEO and COMP SYNC pulses are resistively coupled to create the composite video, which can be supplied directly to a video monitor, a modified TV receiver, or an FCC approved rf modulator.

A clock source of 3.58 MHz, the NTSC color frequency, if divided by 2, may be used for some applications in place of the 1.76-MHz crystal shown in Fig. 6. Deviations from the NTSC frequencies are as follows:

upper left-most spot that can be displayed on the video screen is the most significant bit of the first byte in the display refresh memory buffer. The starting location of the display buffer is initialized in the INTERRUPT routine and may be anywhere in addressable memory (ROM, RAM, or both). The lower right-most spot that can be displayed is the least significant bit of the last byte of the display bit map. For each of the 128 horizontal display lines, 8 bytes of memory are sequentially accessed and displayed from left to right on the video screen. Adjacent illuminated spots appear contiguous both in the horizontal and in the vertical directions. All display manipulations are accomplished by changing the data within the display buffer or by changing display buffers.

To control the CDP1861C as shown in Fig. 6, the CDP1802 must be in synchronization with the CDP1861C during the display window. Exactly six machine cycles must be executed beyond the eight DMA cycles during

NTSC		Clock Frequencies (MHz)		
		1.76064	1.764000	3.579545/2
Line Freq.	15750	15720	15750	15980
Field Freq.	60	60	60.11	60.99

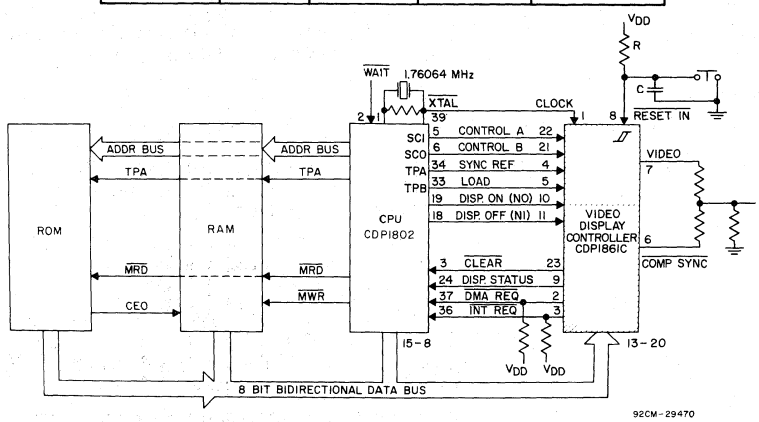


Fig. 6 – Typical CDP1802/CDP1861C video display system.

The user should determine which choice of frequencies provides an optimal cost/performance trade-off for his application. Generally, video CRT's are more sensitive to line frequency accuracy than to field frequency accuracy.

The display is a bit map of memory. Each bit in the display memory corresponds to one spot on the video screen. Logical 1 (V_{DD}) bits in memory correspond to white or lighted spots in the display. The highest resolution that may be produced without any hardware modifications is 128 vertical by 64 horizontal segments. This resolution requires 1024 bytes of memory for the display. The

each line, and an even number of cycles (262 x 14) must be executed from the start of one display window to the start of the next. These requirements insure that the DMA bursts will not be delayed one cycle waiting for an instruction to finish—this delay would cause jitter on the screen. These requirements can be accomplished in two steps: 1) the main program must not execute any 3-cycle instructions (i.e., SKIPS, LONG BRANCHES, and NOP), and 2) the interrupt routine, including the interrupt cycle itself, must employ an even number of cycles, and must be synchronized with the DMA bursts. There must be 29 cycles between the INTERRUPT cycle (S3) and the first burst of

CDP1861C

eight DMA cycles. This timing is accomplished by executing an early 3-cycle instruction to compensate for the INTERRUPT cycle. Furthermore, exactly three 2-cycle instructions must be executed between each successive burst. Occasionally these restrictions may be ignored at the expense of jitter on the screen.

For the 128 x 64 display, the CDP1802 software requirement is straightforward. The DISP STATUS/$\overline{EF1}$ line is not required, and EF1 may be used for other purposes. A simple interrupt routine merely resets the DMA pointer, RO, to the beginning of the display buffer area (see Fig. 5)—note the 3-cycle NOP instruction at the beginning which compensates for the 1-cycle interrupt. The first burst of eight DMA cycles occurs just as this routine finishes, as indicated by the bracket following the RETURN instruction (70). Exactly 29 cycles separate the interrupt request cycle and the first DMA burst. The interrupt routine must last at least 28 cycles, because the interrupt request line is held up that long by the CDP1861C.

When less RAM is to be used (less resolution), a more complicated interrupt routine is used. The interrupt routine is protracted for the full duration of the display window, and the six free cycles in each line are used to execute three instructions, which maintain control over the DMA pointer, RO.1. In the simplest cases, each line of 8 bytes is repeated n times to give 128/n vertical resolution. With n = 4, for example, 64 x 32 resolution is obtained. Such an interrupt routine is shown in Fig. 8. The code from the entry at INTERRUPT to DISPLAY is as in the last example. The use of three instructions per line does not leave time to control a loop, so each of four copies of the line corresponds to three instructions in the main loop, starting at DISPLAY STATUS. The DISPLAY STATUS signal, applied to EF1, is used to RO.1 in the last pass through the loop, when RO advances into the next page after each burst.

For other values of n, similar routines can be devised. For n = 2, the 64 x 64 format, the last 4 lines need special treatment (see Fig. 7). Other schemes are possible, resulting in other resolutions which vary on command from the main program, or even resolutions which vary through the display window.

In general, additional functions may be implemented in the routine before returning to the main program. For example, a real-time clock can be maintained by incrementing a counter once on each interrupt, i.e., once per 1/60 second. Another example is vertical "scrolling" of the display, wherein the starting address in a display file is incremented or reincremented at regular intervals.

Signal Definitions

Signal	Term.No.	Definition
$\overline{\text{RESET IN}}$	8	An input signal which, when low (V_{SS}), initializes the counters, inhibits the display, and places all control outputs in the high (V_{DD}) state. The $\overline{\text{RESET IN}}$ terminal is a Schmitt-trigger-type input which permits the use of an external RC network to provide a power-on reset.
$\overline{\text{CLEAR}}$	23	The output of the Schmitt trigger (reset input circuitry) provides high speed transitions that may be used to reset other devices. It may be connected to the $\overline{\text{CLEAR}}$ terminal of the CDP1802 microprocessor.
DISPLAY-ON DISPLAY-OFF	10 11	Positive input signals that control the display. When enabled (DISPLAY-ON = V_{DD}), data transfers, DMA, and interrupt requests are permitted. These operations are inhibited by the low-to-high transition of the DISPLAY-OFF input signal if DISPLAY-ON = V_{SS}. The $\overline{\text{RESET IN}}$ signal also inhibits the display. When inhibited, the internal counters remain operational. Sync and display status signals are generated. Video output becomes low when the register is emptied. Table I indicates the enable/disable conditions.

Table I

STATE	SIGNAL		
	$\overline{\text{RESET-IN}}$	DISPLAY-ON	DISPLAY-OFF
RESET	L	L	X
INVALID	L	H	X
TV ENABLE	H	H	X
TV DISABLE	H	L	⌐

Signal Definitions (Cont'd)

Signal	Term.No.	Definition
		The DISPLAY-ON and DISPLAY-OFF signals may be provided by the I/O commands (N bits) of the CDP1802 microprocessor.
CLOCK	1	The input for an externally generated single-phase clock which determines the clock rate for the 8-bit data shift register. Data are shifted on the high-to-low transition of the CLOCK input signal, most significant bit first. A low level ("0") is shifted into the least significant bit. The CLOCK signal may be derived directly from the CDP1802 microprocessor by connecting the CLOCK terminal of the CDP1861C to the XTAL terminal of the CDP1802.
SYNC REFERENCE LOAD	4 5	Positive timing pulses each occurring once for every 8 clock pulses. The SYNC REFERENCE signal precedes the LOAD signal. The SYNC REFERENCE signal is used as the clock for the horizontal line counter. The LOAD signal is used as a strobe for gating the output of the counter and for loading data into the data register. They are normally connected to the TPA and TPB terminals of the CDP1802 microprocessor.
$\overline{\text{COMP SYNC}}$	6	Negative (high going low) output signal resulting from the exclusive "OR" of the output of the horizontal and vertical counters. $\overline{\text{COMP SYNC}}$ can be combined with the $\overline{\text{VIDEO}}$ output to form a composite video signal. The $\overline{\text{COMP SYNC}}$ output frequency and pulse duration are determined by the SYNC REFERENCE and LOAD input signals. A horizontal sync pulse is initiated by the trailing edge of the LOAD input signal following the thirteenth or fourteenth SYNC REFERENCE input, as determined by the status of the CONTROL A and CONTROL B input signals, and is terminated on the leading edge of the subsequent second count of the SYNC REFERENCE input. Vertical timing is generated coincident with the 262 horizontal timing pulse and is present for six horizontal clock cycles. Idealized timing is illustrated in Figs. 3 and 5.
$\overline{\text{INTERRUPT REQUEST}}$	3	A low (V_{SS}) output signal two horizontal cycles prior to the display, as shown in Figs. 3 and 5. This signal is the output of the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. The $\overline{\text{INTERRUPT REQUEST}}$ output signal is normally connected to the INTERRUPT input terminal of the CDP1802 microprocessor. In a CDP1802-based system 29 machine cycles occur from initiation of an $\overline{\text{INTERRUPT REQUEST}}$ until the $\overline{\text{DMA REQUEST}}$.
DISPLAY STATUS	9	A low (V_{SS}) output signal which occurs for a period of four horizontal cycles prior to the beginning and end of the 128-line display window, as illustrated in Figs. 3 and 5. The signal can be used by the program software routines to indicate the boundaries of the display area. It is normally connected to a CDP1802 FLAG input terminal.

CDP1861C

Signal Definitions (Cont'd)

Signal	Term.No.	Definition
$\overline{\text{DMA REQUEST}}$	2	A low output (V_{SS}) that requests an 8-bit data transfer. The output signal is from the "open drain" of an n-channel transistor and requires an external pull-up resistor to V_{DD}. Depending upon the status of the CONTROL A and CONTROL B input signals at horizontal sync time, DMA requests are initiated on the leading edge of the second SYNC REFERENCE input signal following the horizontal sync output. This feature is necessary in order to reference the data requests to the program's ability to respond to them, insuring that data will always be initiated at the same point on the display. The system should respond to a $\overline{\text{DMA REQUEST}}$ by setting CONTROL B high (V_{DD}), and CONTROL A low (V_{SS}) permitting data transfer. Data will be loaded on the subsequent 8 LOAD input signals. $\overline{\text{DMA REQUEST}}$ will be terminated on the ninth sync pulse, at which time CONTROL B should be set low (V_{SS}) prior to the next LOAD command. Timing is illustrated in Figs. 3 and 5. The $\overline{\text{DMA REQUEST}}$ output signal may be connected to the DMA IN terminal of the CDP1802 microprocessor, which responds as discussed above.
CONTROL A CONTROL B	22 21	Input signals used to synchronize the operation of the CDP1861C with its controller. They should be initiated prior to the SYNC REFERENCE input and terminate after the LOAD input pulse. The CONTROL signals are sampled at two different times: 1) During the horizontal sync output when the SYNC REFERENCE input is present, the CDP1861C expects to see CONTROL A = 1 (V_{DD}), and CONTROL B = 0 (V_{SS}). Any other combination will result in the skipping of one of the normal 14 cycles per line. This feature allows the CDP1802 to force initial instruction fetch/execute sync with the CDP1861C, and assures sync in case it is later lost for any reason. 2) In the 8 cycles following the CDP1861C $\overline{\text{DMA REQUEST}}$ assertion, the CDP1861C expects to see CONTROL A = 0, and CONTROL B = 1. Any other combination will prevent the CDP1861C from loading data from the bus. These signals may be connected to the STATE CODE outputs of the CDP1802 microprocessor; CONTROL A to SC0 and CONTROL B to SC1.
DI7 - DI0	13-20	Input signals to the data register. Data are loaded during the high-to-low transition of the CLOCK only when LOAD = V_{DD} and the CDP1861C is enabled. DISPLAY-ON = 1 (V_{DD}), CONTROL A = 0 (V_{SS}), and CONTROL B = 1 (V_{DD}). The data input signals are normally connected to the 8-bit microprocessor data bus.
VIDEO	7	Output from the most significant bit of the data register. It is used to determine the luminance level and may be combined externally with the $\overline{\text{COMP SYNC}}$ output signal to form a composite video signal.

Machine Code	Assembly Language		Comments
72	INTRET:	LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT :	NOP	. . 3 CYC.INSTR.FOR PGM.SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T → STACK
22		DEC R2	
52		STR R2	. . D → STACK
F8__B0		A.1(DISMEM) → RO.1	. . DISMEM IS START ADDR
F8__A0		A.0(DISMEM) → RO.0	. . OF DISPLAY MEMORY
C4, C4		NOP; NOP	. . NOPS FOR PGM SYNC
E2		SEX2	
80]	DISP :	GLO RO	. . NEW LINE
E2		SEX2	. . NOP
20		DEC RO	. . RESTORES RO.1 IF PASS PG
A0]		PLO RO	. . REPEATS SAME LINE
E2		SEX2	. . NOP
3C__		BN1 DISP	. . LOOP 60 TIMES
80]	DISEF :	GLO RO	. . LAST 4 VIDEO LINES
E2		SEX2	. . NOP
20 A0]		DEC RO; PLO RO	
E2		SEX2	. . NOP
34__		B1 DISEF	
30__		BR INTRET	. . END OF DISPLAY

Fig. 7 — Interrupt routine for 64 x 64 format (2 pgs mem).

Machine Code	Assembly Language		Comments
72	INTRET:	LDXA	. . RESTORE D
70		RET	. . RETURN
C4	INT :	NOP	. . 3 CYC. INSTR. USED . . FOR PGM. SYNC
22		DEC R2	. . R2 IS STACK PTR
78		SAV	. . T → STACK
22		DEC R2	
52		STR R2	. . D → STACK
F8__B0		A.1(DISMEM) → RO.1	. . LOAD RO WITH
F8__A0		A.0(DISMEM) → RO.0	. . START.ADDR.OF DISP.MEM
C4, C4		NOP; NOP	. . NOPS USED FOR SYNC
E2	DISP :	SEX2	
80]		GLO RO	. . LINE START ADDR. → D
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR. → RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0]		PLO RO	. . LINE START ADDR. → RO.0
E2		SEX2	. . NOP
20		DEC RO	. . RESET RO.1 IF PASS PG
A0		PLO RO	. . REPEATS SAME LINE
3C__		BN1 DISP	. . LOOPS 32 TIMES
30__		BR INTRET	. . END OF DISPLAY

Fig. 8 — Interrupt routine for 64 x 32 format (1 pg mem).

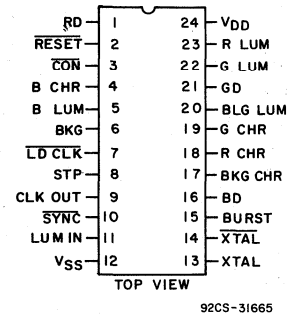
CDP1862C Types

COS/MOS Color Generator Controller

Preliminary Data

Features:

- Static silicon-gate CMOS circuitry
- Interfaces directly with CDP1802 Microprocessor
- Interfaces directly with CDP1861 Video Dispaly Controller
- Programmable background color
- Programmable video (dot) color
- Single voltage supply (4 to 6.5 volts)
- Low quiescent and operating power
- On-chip crystal controlled oscillator
- NTSC compatible color and RGB compatible



TERMINAL ASSIGNMENT

The RCA-CDP1862C is a color generator controller designed for use in CDP1800-series microprocessor systems. It is intended for use with the RCA-CDP1861C video display controller and will interface directly with the CDP1802C/CDP1861C as shown in the system diagram below.

The CDP1862C utilizes many features of the CDP1802C and CDP1861C to simplify control and minimize the need for external components. The CDP1862C is NTSC color compatible. Red, blue and green luminance signals are also available for directly controlling the red, blue and green amplifiers of a video monitor. A 7.15909-MHz on-chip crystal-controlled oscillator or an external 7.15909-MHz clock is used to generate multiple phases of the 3.579545-MHz color burst frequency for NTSC-compatible color. The color burst is further divided by 2 to provide system timing for the CDP1802C and the CDP1861C. This frequency (1.789773 MHz) is available at CLK OUT. Two inputs, STP (Synchronous timing pulse) and $\overline{SYNC}$, are used to maintain system synchronization. The $\overline{RESET}$ input resets the CDP1862C and sets the background color to blue and the dot color to white

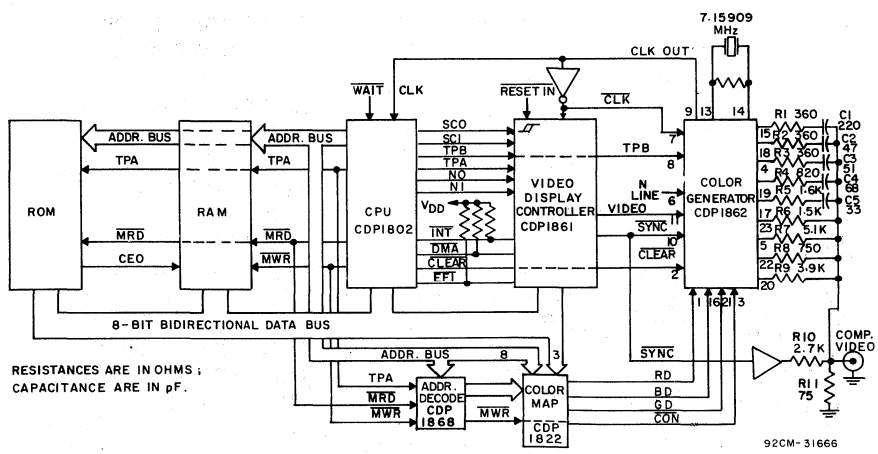


Fig. 1 – Typical CDP1802 microprocessor system using the CDP1862.

Background color: Four background colors are available. The colors are changed each time STP is pulsed high when BKG = high. The sequence is from blue to black to green to red and return to blue (see Fig. 2).

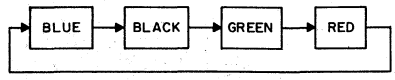


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Fig. 2 – Background Color Sequencing.

Dot color: Color data (RD, BD, GD) is latched internally on the high-to-low transition of $\overline{\text{LD CLK}}$ when STP = high. Eight colors are available as shown in Table I. The color is overlayed onto the LUM IN data (video output from CDP1861C). Each

TABLE I – Color Table

RD	BD	GD	COLOR
0	0	0	Black
0	0	1	Green
0	1	0	Blue
0	1	1	Cyan
1	0	0	Red
1	0	1	Yellow
1	1	0	Purple
1	1	1	White

color corresponds to eight horizontal bits of video information. Only the selected background color appears at the output if LUM IN = low. When used with the CDP1861C and set for the maximum resolution of 64X128, 1024 color blocks (8X128) are possible, and would require a 1K X 3 random-access memory storage area. This area would appear to be a write-only memory to the microprocessor because, in the programmed state, this area occupies an unique, unused 1K block of memory space. However, when it is read, this area responds to the same address space occupied by the CDP1861C refresh RAM. This is accomplished with proper decoding and requires the memory to have separate I/O lines.

The $\overline{\text{CON}}$ input enables the RD, BD and GD input latches. After a $\overline{\text{RESET}}$ condition, the dot color is set to white and any color change is inhibited until the $\overline{\text{CON}}$ input is pulsed low, which normally occurs when data is written into the color map. The $\overline{\text{CON}}$ input provides a means of inhibiting erroneous color data until the color map is properly loaded.

The color luminance (R LUM, B LUM, G LUM), color chrominance (R CHR, B CHR, G CHR), background luminance (BKG LUM), background chrominance (BKG CHR), color burst (BURST), and $\overline{\text{SYNC}}$ are combined by an external RC network to generate the composite video (see Fig. 1).

The BURST signal is normally high and oscillates at 1/2 the XTAL frequency from the low-to-high transition of $\overline{\text{SYNC}}$ until STP = high.

The CDP1862C types are supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4	6.5	V
Input Voltage Range	–	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time	5	–	5	μs
Clock Input Frequency, f_{CL}	5	7.15909		MHz

CDP1862C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
				CDP1862CD CDP1862CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	0, 5	5	–	100	500	μA
Output Low Drive (Sink) Current, I_{OL} (Except $\overline{XTAL}$)	0.4	0, 5	5	2	2.4	–	mA
$\overline{XTAL}$ Output, I_{OL}	0.4	0, 5	5	150	200	–	μA
Output High Drive (Source) Current, I_{OH} (Except $\overline{XTAL}$	4.6	0, 5	5	−1.6	−1.8	–	mA
$\overline{XTAL}$ Output, I_{OH}	4.6	0, 5	5	−150	−200	–	μA
Output Voltage Low-Level, V_{OL}	–	0, 5	5	–	0	0.05	V
Output Voltage High Level, V_{OH}	–	0, 5	5	4.95	5	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	–	5	3.5	–	–	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	–	±0.1	±1	μA

* Typical values are for T_A = 25°C.

CDP1862C Types

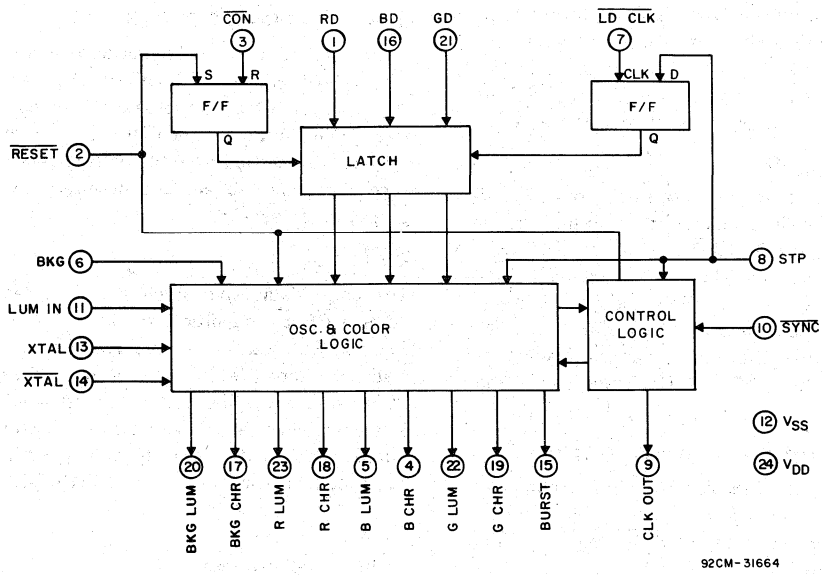


Fig. 3 – Functional block diagram.

SIGNAL DESCRIPTIONS

$\overline{\text{RESET}}$

A low level on this input initializes the internal counters, sets the background color to blue, and sets the dot color to white.

BKG

A high level on this input enables the background color to be changed when STP is pulsed high. This signal is normally connected to an I/O line of the CDP1802C microprocessor.

$\overline{\text{LD CLK}}$

An input signal used to latch the color data information. Color data (RD, BD, GD) is latched on the high-to-low transition of $\overline{\text{LD CLK}}$ when STP = high. This signal is normally connected to CLK OUT through an inverter.

STP

A high level on this input enables color data latching and sequences background color when BKG = high. This signal is normally connected to the TPB terminal of the CDP1802C microprocessor.

CLK OUT

An output signal, equal to the XTAL frequency divided by four, that provides the overall system synchronization. This signal is normally connected to the CLOCK terminal of the CDP1802C microprocessor. The inverse of this signal is normally connected to the $\overline{\text{CLOCK}}$ terminal of the CDP1861C and the $\overline{\text{LD CLK}}$ terminal of the CDP1862C.

$\overline{\text{SYNC}}$

An input signal used to provide horizontal line synchronization between the CDP1861C and the CDP1862C color signals. This signal is normally connected to the $\overline{\text{SYNC}}$ terminal of the CDP1861C.

LUM IN

The luminance video input, to which the color information is added. One color block corresponds to eight serial bits of data from this input. This input is normally connected to the VIDEO terminal of the CDP1861C.

V_{SS}

Negative supply voltage; ground.

XTAL, $\overline{\text{XTAL}}$

Terminal connections for an external crystal, in parallel with a resistance (10 megohms typ.) if the on-chip oscillator is utilized. Frequency trimming capacitors may be required at terminals 13 and 14. XTAL is the input for an externally generated single-phase clock.

BURST

The color reference output, which oscillates at the XTAL frequency divided by 2. This

CDP1862C Types

signal provides approximately 11 cycles of 3.579545 MHz from the low-to-high transition of $\overline{SYNC}$ until STP = high. This signal is coupled through an external series RC circuit to the $\overline{SYNC}$ output of the CDP1861C.

RD, BD, GD

The red, blue, and green color data inputs. One of eight colors is latched on the high-to-low transition of $\overline{LD\ CLK}$ when STP = high, forming a color block of eight horizontal LUM IN data bits. Only the selected background color appears at the output if LUM IN = low. These inputs are normally connected to the DATA OUT terminals of the color map memory.

BKG LUM, R LUM, B LUM, G LUM

These output signals provide background and color luminance information. They are resistively added to the $\overline{SYNC}$ output of the CDP1861C.

BKG CHR, R CHR, B CHR, G CHR

These output signals provide background and color chrominance information. They are coupled through an external series RC circuit to the $\overline{SYNC}$ output of the CDP1861C. Each signal is phase-shifted from the BURST reference signal by the amount necessary for proper color operation.

$\overline{CON}$

The color data input latch enable signal. After a $\overline{RESET}$ condition, the internal RD, BD, and GD input latches are held in a reset state, providing a white color output. When $\overline{CON}$ is pulsed low, the reset state is removed and the latches are enabled, providing color output. This input is normally connected to the gated $\overline{MWR}$ signal from the CDP1802C.

V_{DD}

Positive supply voltage.

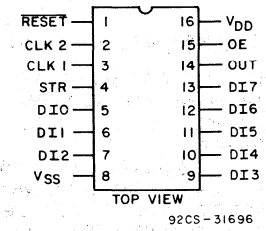
CDP1863, CDP1863C Types

COS/MOS 8-Bit Programmable Frequency Generator

Preliminary Data

Features:

- Static silicon-gate CMOS circuitry
- Interfaces directly with CDP1802 microprocessor
- 256 possible programmable frequencies
- Single voltage supply (4 to 10.5 volts)
- Two clock input predividers (÷ 4 and ÷ 8)
- Gated square-wave output



TERMINAL ASSIGNMENT

The RCA-CDP1863 and CDP1863C COS/MOS integrated circuits are programmable frequency generators designed to produce 256 possible frequencies from a single-frequency input clock. They will interface directly with the CDP1802 microprocessor as shown in the system diagram (see Fig. 1).

The CDP1863 and CDP1863C consist of a programmable up-counter and an 8-bit latch (see Fig. 2). An input clock is predivided by a fixed internal counter chain in addition to the programmable counter. The final stage of the device divides the output of the up-counter by two to provide a square-wave output. The input clock may be applied to either of two inputs; CLK1 provides a divide-by-four predivide, and CLK2 a divide-by-eight. The unused input must be tied to V_{DD} to avoid interference with the true clock. After the programmable up-counter has reached its maximum count, the next pre-divided clock pulse will cause it to go to zero. At this time the output flip-flop toggles and the load flip-flop is turned on. The output of the load flip-flop is fed into the NOR gates which allow the divide rate stored in the 8-bit latch to preset the up-counter. Before the next predivided clock pulse clocks this up-counter, the load flip-flop is reset and the NOR gates are turned off. The counter then resumes its up-count. The data at the eight data inputs is latched into the device by the high-to-low transition of CLK1, when STR(STROBE) is high, or by the high-to-low transition of STR, when CLK1 is high.

When using CLK2, CLK1 must be tied to V_{DD} to permit the STR input to generate the internal latch clock. The 8-bit data in the latch determines the divide rate of the programmable up-counter in the device. This rate may range from divide-by-one to divide-by-256.

A low level on the $\overline{\text{RESET}}$ input resets the up-counter, predividers, and flip-flops, and forces an initial state into the 8-bit data latch. This initial state provides a fixed

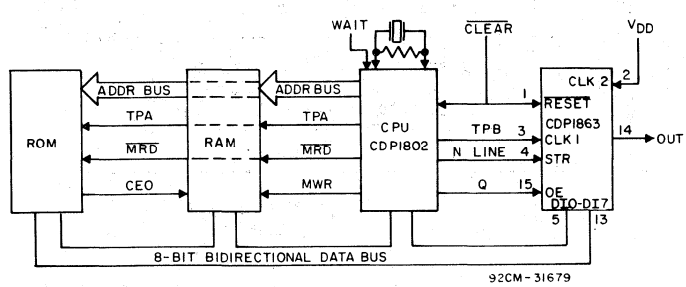


Fig. 1 – Typical CDP1802 microprocessor system using the CDP1863.

CDP1863, CDP1863C Types

divide rate for the device prior to running the system. A high level on the $\overline{\text{RESET}}$ input enables the up-counter, predividers, and flip-flops and allows programming a new divide rate into the device.

The CDP1863 and CDP1863C are functionally identical. They differ in that the CDP1863 has an operating voltage range of 4 to 10.5 volts and the CDP1863C has an operating voltage range of 4 to 6.5 volts. Both are supplied in 16-lead hermetic dual-in-line ceramic packages (D suffix) and in 16-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1863 . . . . . −0.5 to +11 V
CDP1863C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. . . . . +265°C

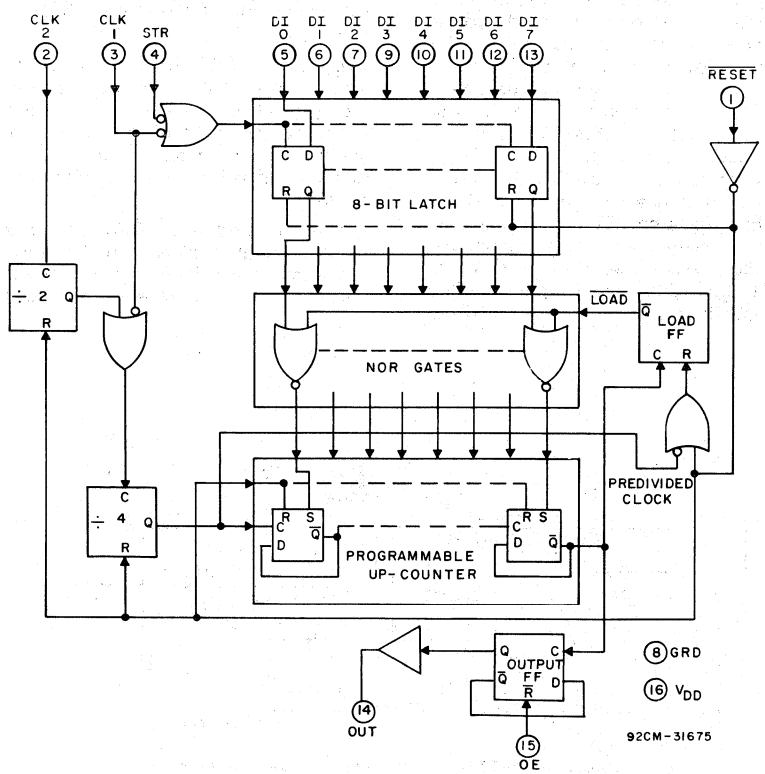


Fig. 2 – Block diagram for the CDP1863 and CDP1863C.

CDP1863, CDP1863C Types

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	LIMITS				UNITS
	CDP1863D		CDP1863CD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	5	–	5	μs

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1863D CDP1863E			CDP1863CD CDP1863CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	–	5	–	100	500	–	100	500	μA
	–	–	10	–	500	1000	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	2.2	–	1.6	2.2	–	mA
	0.4	0,10	10	3	3.6	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.5	0,5	5	−1	−1.6	–	−1	−1.6	–	mA
	9.5	0,10	10	−3	−3.6	–	–	–	–	
Output Voltage Low-Level, V_{OL}	–	0,5	5	–	0	0.05	–	0	0.05	V
	–	0,10	10	–	0	0.05	–	–	–	
Output Voltage High-Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5,4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5,9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5,4.5	–	5	3.5	–	–	3.5	–	–	
	0.5,9.5	–	10	7	–	–	–	–	–	
Input Leakage Current, I_{IN}	Any Input	0,5	5	–	±0.1	±1	–	±0.1	±1	μA
		0,10	10	–	±0.1	±1	–	–	–	

* Typical values are for T_A = 25°C.

SIGNAL DESCRIPTIONS

CLK1, CLK2

Input clock which is divided-down by the device to provide an output frequency. The divide rate of the device is composed of a fixed predivide, the programmable divider, and a divide-by-two output flip-flop which provides a square-wave output. CLK1 is pre-divided by four and CLK2 is predivided by eight. The unused CLOCK input must be tied to V_{DD} to avoid interference with the true CLOCK signal. CLK1 may also be used to latch the eight data inputs.

OUT

Square-wave output which is the result of the divided-down input CLOCK. The OUTPUT toggles after the programmable up-counter reaches its maximum value and goes to zero. OUT is held low when OE is low.

OE

A high on this input allows OUT to toggle freely. A low on OE holds OUT low.

CDP1863, CDP1863C Types

DIO-DI7

Data inputs for programming the divide rate of the device. The divide rates programmed into the device are inversely proportional to the output frequencies generated. For example, programming the device with 00_{16} causes the programmable up-counter to divide by one, providing the maximum output frequency for any given input clock. Programming an FF_{16} results in the maximum divide rate and the minimum output frequency. To determine the frequency generated by a given programmed divide rate, divide the input clock frequency by the decimal equivalent of the programmed divide rate plus one, times the fixed predivide which is 8 for CLK1 or 16 or CLK2:

Input Clock Frequency/[Programmed Divide Rate + 1)$_{10}$ (Fixed Predivide)]

STR

Positive pulse used to latch data at the eight inputs into the device. This pulse is gated with CLK1 to form the internal latch clock. When CLK1 is the input clock, the STR input must be positive during the high-to-low transition of CLK1. When CLK2 is the input clock, CLK1 must be tied to V_{DD} so that the STR input produces the latch clock.

$\overline{\text{RESET}}$

A low on the $\overline{\text{RESET}}$ input resets all the stages of the predividers and the programmable up-counter and sets an initial divide rate into the latch. This is to provide a standard initial divide rate at the moment the system begins running. A high on $\overline{\text{RESET}}$ enables the counter to run freely and allows programming a new divide rate. The initial state of the up-counter is a divide-by-54 resulting in a total divide rate of 432 when using CLK1 and 864 when using CLK2.

V_{DD}

Positive supply voltage.

V_{SS}

Negative supply voltage; ground.

APPLICATION

The programmable frequency generator is directly compatible with the CDP1802 COSMAC microprocessor. In Fig. 1 a simple CDP1802 system using this device is shown. TPB may be used as the input clock. At typical CDP1802 system clock frequencies, using TPB as an input to CLK1 results in nearly every possible output of the device being in the audio range. The Q output of the CDP1802 may be used as the OUTPUT ENABLE (OE) of the device. The eight data inputs are connected to the bidirectional data bus which allows the system memory to provide divide rate data to the device. A single N bit or some decoded output of all the N bits may be used as the STR input to latch data into the device. This involves designating some output instruction of the CDP1802 for providing the STR. The output instruction places the data pointed to by the X register on the bus, while simultaneously pulsing the appropriate N bits. By the internal gating of TPB and STR, when TPB is fed into CLK1, the resulting latch clock terminates while the data is still valid on the 8-bit bus. If TPB is fed into CLK2, it is necessary to provide an external AND gate for the appropriate N bits and TPB, to preserve this timing feature. The same signal that feeds the $\overline{\text{CLEAR}}$ input of the CDP1802 may be used as the $\overline{\text{RESET}}$ signal to this device.

As an example of programming the frequency generator, assume a 64 instruction is selected as the output code used to pro-

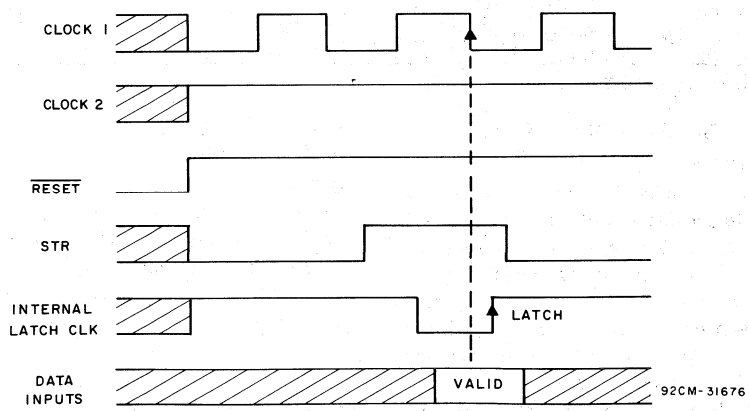


Fig. 3 – General CLOCK 1 timing diagram.

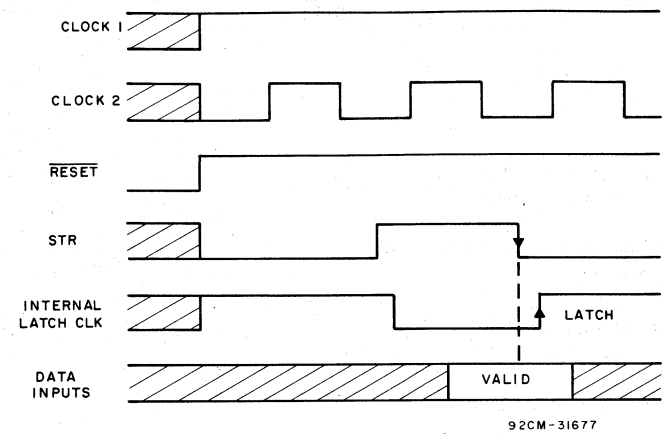


Fig. 4 – General CLOCK 2 timing diagram.

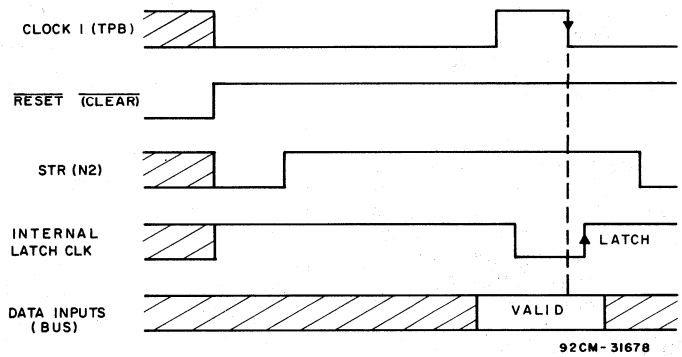


Fig. 5 – General CDP1802 system timing diagram.

gram the device. Let machine register E point to the data to be latched. N2 is the only N bit pulsed by a 64 instruction and may be fed directly to the STR input if TPB is fed to CLK1. An EE instruction makes RE the X register. Following this with a 64 instruction puts the data pointed to by RE onto the data bus and raises the N2 bit. TPB, which is within the duration of the N2 pulse, causes the internal latch clock to terminate before the data bus loses validity. The latch in the device continually passes the data inputs through to the outputs of the latch as long as CLK1 and STR are high. Once CLK1 goes low, data is locked in. A 7B instruction then sets the Q line high which, if connected to OE, allows the OUT to toggle at the desired rate.

Code:

EE	RE is the X register
64	M(E)→BUS N2 pulsed high
7B	Q turned on

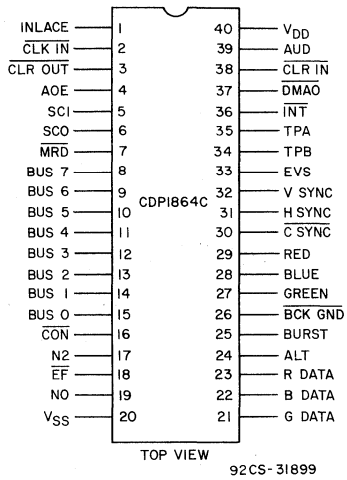
CDP1864C Types

COS/MOS PAL Compatible Color TV Interface

Objective Data

Features:

- Single chip contains circuitry for video, sync, RGB color, and programmable frequency for tone generation
- Programmable 1-of-8 dot colors plus 1-of-4 background colors
- Bit-mapped display with maximum resolution of 192 vertical x 64 horizontal
- Directly interfaces with CDP1800 series microprocessors
- Interlaced or non-interlaced displays
- Schmitt trigger clear input and output for power-on reset of CDP1800 system
- 1.75-MHz crystal operation
- Single 4.75 to 6.5 V supply
- Low-power static CMOS circuitry
- High noise immunity



TERMINAL ASSIGNMENT

The RCA-CDP1864C is an LSI CMOS color or black and white PAL-compatible video controller designed for use in CDP1800 microprocessor systems. It interfaces directly with the CDP1802 and CDP1804 as shown in Figs. 1 and 2. The DMA feature of these processors is used for direct data transfers of luminance information for display refresh. The INTERRUPT input and a flag line (EF1, EF2, EF3, or EF4) are used for handshaking.

The CDP1864C generates vertical sync, horizontal sync, and composite sync. These signals, combined with the RED, BLUE, GREEN, BURST, and BACKGROUND signals, can be used to generate a composite video signal, or they can be used directly inside a TV set.

In addition to generating a bit-mapped video display the CDP1864C contains a programmable frequency generator designed to produce 256 tones that range from 107 Hz to 13672 Hz.

The CDP1864C is supplied in the 40-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

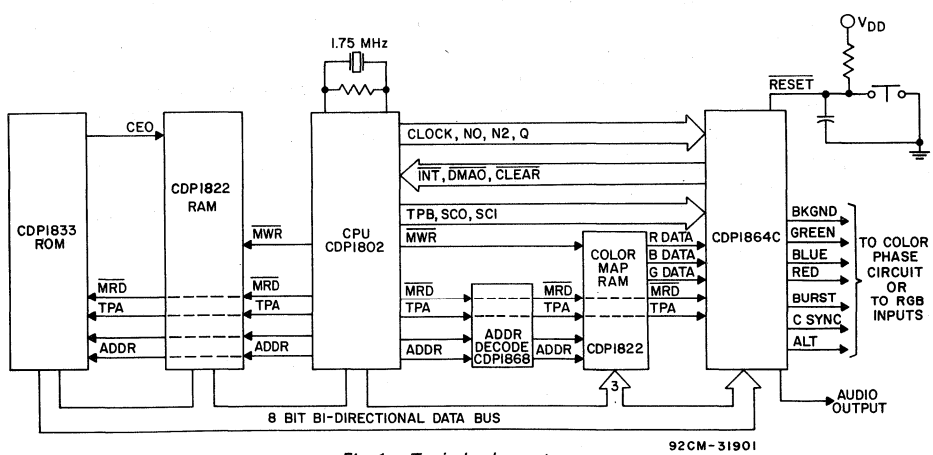


Fig. 1 – Typical color system.

CDP1864C Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1864C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
DC Operating-Voltage Range	–	4 to 6	V
Input Voltage Range	–	V_{SS} to V_{DD}	V
Maximum Input Pulse Rise or Fall Time, t_r,t_f	5	5	μs
Maximum Input Clock Frequency, f_{CL}	5	2	MHz

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V ±5%

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	V_O (V)	V_{IN} (V)	CDP1864C			
			Min.	Typ.	Max.	
Quiescent Device Current, I_{DD}	–	0,5	–	100	500	μA
Output Voltage:*						
Low-Level, V_{OL}	–	0,5	–	0	0.05	V
High-Level, V_{OH}	–	0,5	4.95	5	–	V
Input Low Voltage, V_{IL}	0.5,4.5	Any Input	–	–	1.5	V
Input High Voltage, V_{IH}	0.5,4.5	Any Input	–	–	3.5	V
Output Low (Sink) Current, I_{OL}	0.4	0,5	2	2.4	–	mA
Output High (Source) Current, I_{OH}	4.5	0,5	−1.6	−1.8	–	mA
Input Leakage Current, I_{IL},I_{IH}	–	Any Input	–	±0.1	±1	μA
3-State Output Leakage Current, I_{OUT}	0.5	0,5	–	±0.2	±2	μA

*$I_O \leqslant 1$ μA.

CDP1864C Types

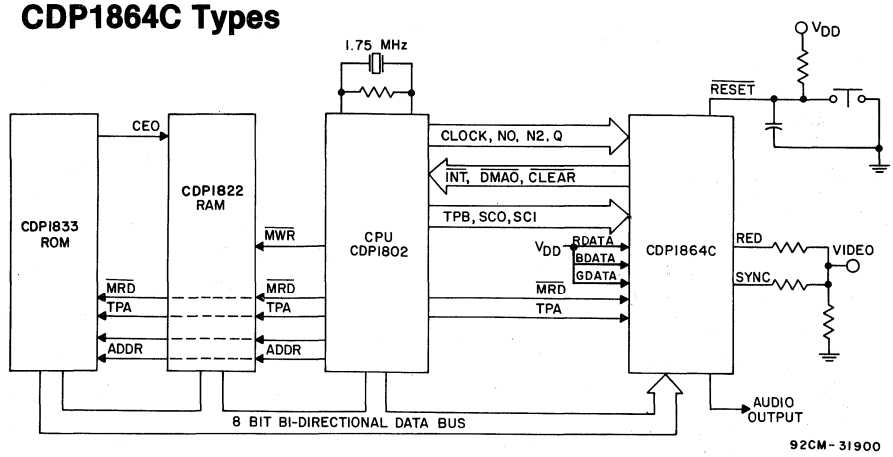


Fig. 2 – Typical black and white system.

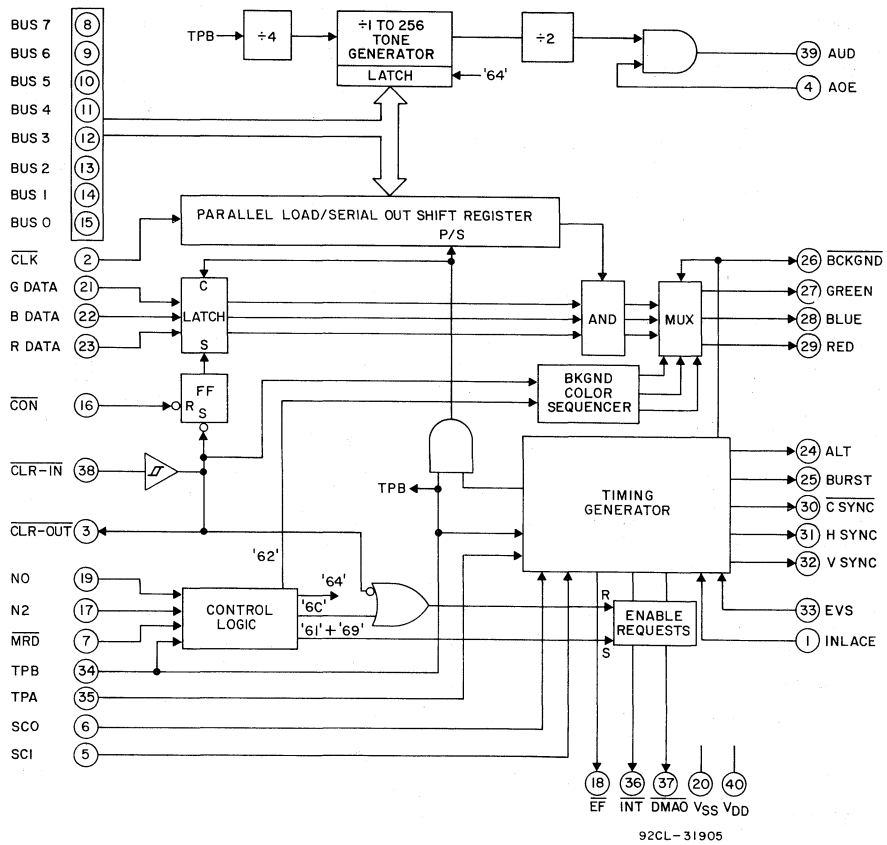


Fig. 3 – CDP1864C block diagram.

CDP1864C Types

CIRCUIT OPERATION

The CDP1864C consists of four major sections: a timing generator that produces the necessary signals for video interface, a parallel-in/serial out shift register for dot generation, a tone generator for one of 256 frequencies, and control logic for software control of the first three sections (see Fig. 3). In a typical CDP1800 system, control of the CDP1864C is accomplished with I/O commands as shown in Fig. 5.

The CDP1864C display is a bit-mapped, color or black and white display with a maximum resolution of 192 lines vertically and 64 dots (eight 8-bit bytes) horizontally. This resolution, which requires 1.5 kbytes of refresh RAM, is seldom used because of the poor aspect ratio of the resultant picture element. An approximately square picture element is obtained by repeating each horizontal line 6 times (this is done in software by the CPU) for a 32-row by 64-dot display. This lower resolution display requires 256 bytes of refresh RAM.

The CDP1864C generates both composite and separate horizontal and vertical sync, RED, BLUE, GREEN, BURST, and BACKGROUND signals. These signals may be used directly (inside the TV), or they may be used to generate the composite video signal. The sync signals generate either a 625 line-per-frame interlaced display or a 312 line-per-frame non-interlaced display. This is selectable by connecting the INTERLACE input to either V_{DD} or GND.

The video refresh is accomplished via the DMA channel of the microprocessor, and synchronization is provided by $\overline{INT}$, $\overline{EF}$, SCO, and SC1. The $\overline{EF}$ signal goes low 4 horizontal lines prior to the start of display and again 4 lines prior to the end of the display. This signal alone can be used by the CPU to initialize R(O) for DMA refresh. Alternatively, the $\overline{INT}$, which goes low 2 lines prior to the start of the display, may be used to enter an interrupt routine that initializes R(O), and the $\overline{EF}$ signal can be used to indicate the end of the display. The combination of $\overline{INT}$ and $\overline{EF}$ allows for an interrupt routine to oversee DMA refresh and repeat horizontal lines for configurations with less than the maximum 192-line resolution. $\overline{EF}$ can be sampled to detect the end of the display and cause a return to the main program from the interrupt routine.

SC1 and SC0 are used to provide CDP1864C-to-CPU synchronization for a jitter-free display. During every horizontal sync the CDP1864C samples SC0 and SC1 for SC0 = 1 and SC1 = 0 (CDP1800 execute state). Detection of a fetch cycle causes the CDP1864C to skip cycles to attain synchronization. Once in lock the system will remain locked if: (1) no 3-cycle instructions (e.g. NOP) are executed during the display (three 2-cycle instructions are executed each horizontal line); (2) an even number of cycles is performed between frames (easiest to do by avoiding 3-cycle instructions); or (3) exactly 29 cycles, beginning with a fetch and ending with an execute, are completed between the S3 interrupt response of the cpu and the first DMA in systems using $\overline{INT}$. The 29 cycles of interrupt should consist of an early 3-cycle instruction and thirteen 2-cycle instructions (or equivalent). Fig. 5 is an example of an interrupt routine for a 64 by 32 picture element display (each horizontal line is repeated 6 times).

Reset disables the color control, $\overline{INT}$, and $\overline{DMA}$ requests. A 61 or 69 instruction enables the requests, and a 6C instruction disables them (see Fig. 5). Color is enabled by $\overline{CON}$, which is normally connected to the gated $\overline{MWR}$ signal of the color RAM.

The background color is program-selected to be either blue, black, green, or red. The initial default is blue. The color selected is changed by a 61 instruction (see Fig. 5). This condition causes the color to step to the next color in the order shown above. From red it steps to blue. The BACKGROUND output may be used to lower the luminance of the color when it is background. This would, for instance, enable a blue spot to be used on a blue background and still be visible. The BACKGROUND signal and RGB outputs are internally blanked during the horizontal and vertical retrace.

The CDP1864C also contains a programmable tone generator designed to produce 256 frequencies. The frequency input to this generator is the TPB input (TPB frequency = 1.75 MHz ÷ 8 = 218.75 kHz). This frequency is further reduced by a divide-by-4 predivider, an 8-bit programmable up-counter, and a divide-by-2 output stage. The programmable up-counter is reloaded automatically from the 8-bit tone generator latch each time it reaches the terminal count. The tone generator latch is loaded by the CPU from the data bus during a 64 output instruction (see Fig. 5).

An AUDIO OUTPUT ENABLE (AOE) terminal is also provided. When this terminal is high the output of the generator (AUDIO OUT) is allowed to toggle freely. When this terminal is low the output is held low. AUDIO OUT may be connected to the Q line of the CDP1802/CDP1804. A low on the reset sets the 8-bit latch to a default state of 35 hex and resets the programmable counter. When reset is released a frequency output of 506 will be generated until a new value is loaded into the latch. The frequencies generated from the input to the 8-bit tone generator latch can be computed by:

$$f = \frac{27343.75}{(\text{Hex Code} + 1)_{10}} \text{ Hz.}$$

CDP1864C Types

FUNCTIONAL DESCRIPTION OF CDP1864C TERMINALS

INLACE – INTERLACE (Input):
A high level at this input results in the generation of a 625 line-per-frame interlaced display, and a low-level input results in the generation of a 312 line-per-frame non-interlaced display.

$\overline{\text{CLK IN}}$ – $\overline{\text{CLOCK INPUT}}$ (Input):
A 1.75 MHz clock input to the XTAL terminal of the CDP1802/CDP1804.

$\overline{\text{CLR OUT}}$ – $\overline{\text{CLEAR OUT}}$ (Output):
This is a post-Schmitt trigger output of the signal on CLR IN. It is connected to the CLEAR-N input of the CDP1802 to provide it with a clean, clear signal.

AOE – AUDIO OUTPUT ENABLE (Input):
A high level at this input allows the selected frequency to be generated at the AUDIO-OUT terminal. A low-level input holds AUDIO OUT low. AOE may be connected to Q output of the CDP1802/CDP1804.

SCO, SC1 – STATE CODES 0 AND 1 (Inputs):
These inputs are used to synchronize the CDP1864 to the microprocessor machine states and are connected to the SC1 and SC0 outputs of the CDP1802/CDP1804.

$\overline{\text{MRD}}$ – (Input):
This input selects the command issued to the CDP1864 (in conjunction with N2 and NO). It is connected to the MRD output of the CDP1802/CDP1804.

BUS 0 – BUS 7 (Inputs):
These inputs load the luminance information during the display interval, and the frequency generator divide byte when selected. They are connected to the DATA BUS.

$\overline{\text{CON}}$ – $\overline{\text{COLOR ON}}$ (Input):
A low level at this input enables the CDP1864 to begin loading color information form the RDATA, GDATA, and BDATA inputs. CON is connected to the gated MWR signal of the color memory.

N2 (Input):
This input is used in conjunction with $\overline{\text{MRD}}$ and TPB to load data into the tone generator latch ($\overline{\text{MRD}}$•N2•TPB) and disable the generation of INTERRUPT and DMA requests by the CDP1864 ($\overline{\text{MRD}}$•N2•TPB). For example, a 64 instruction would result in data being loaded into the tone-divider latch, while a 6C instruction would disable the INTERRUPT and DMA requests. N2 is connected to the N2 output of the CDP1802/CDP1804.

$\overline{\text{EF}}$ – $\overline{\text{EXTERNAL FLAG OUT}}$ (Output):
This output is connected to a CDP1802/CDP1804 $\overline{\text{EXTERNAL FLAG}}$ input. It maintains software synchronization with the display. Two pulses per field are generated on this line, each of which is four horizontal lines wide. The first pulse begins four horizontal lines before the display, and the second pulse begins four horizontal lines prior to the end of the display. The second pulse is used to indicate to the microprocessor that the display is ending.

NO (Input):
This input is used in conjunction with $\overline{\text{MRD}}$ and TPB to step the background color (MRD•NO•TPB) and to enable the INTERRUPT and DMA requests (NO•TPB). For example, a 61 instruction would step the background color, and a 61 or 69 instruction would enable the INTERRUPT and DMA requests. NO is connected to the NO output of the CDP1802/CDP1804.

V_{SS}:
Negative supply voltage.

GDATA, BDATA, RDATA – RED, GREEN, and BLUE DATA (Inputs):
These inputs carry color information from the color RAM. The data on these lines are latched concurrent with the latching of the luminance information from the data bus during the display interval if the $\overline{\text{CON}}$ input has gone low since reset.

ALT – ALTERNATE (Output):
This output toggles at each horizontal sync time and is used to perform the phase alternation.

BURST (Output):
This output applies a 4.57 us pulse to each horizontal sync back-porch (except for 24 lines during vertical sync when it is blanked) which gates in the color burst signal.

$\overline{\text{BCKGND}}$ – $\overline{\text{BACKGROUND}}$ (Output):
This output indicates that the color selected by the RGB outputs is due to background color select rather than a one bit in a display luminance byte. $\overline{\text{BCKGND}}$ may be used to lower the luminance of the background color so that the same color may be used for display of data. This output is blanked (held high) during horizontal and vertical blanking.

GREEN, BLUE, RED (Outputs):
These outputs are used either directly in the TV to generate the selected colors, or indirectly to generate a composite video signal. These outputs are used to indicate the selected color for an "on" spot or the background color for an "off" spot.

$\overline{\text{CSYNC}}$ – $\overline{\text{COMPOSITE SYNC}}$ (Output):
This output is the composite serrated horizontal and vertical sync signal.

HSYNC – HORIZONTAL SYNC (Output):
This output is a separate horizontal sync signal.

EVS – EXTERNAL VERTICAL SYNC (Input):
A high level at this input sets the line counters to the vertical sync state.

TPB – TIMING PULSE B (Input):
This input is connected to the TPB output of the CDP1802/CDP1804. It is used for strobing the $\overline{MRD}$ and N lines, for horizontal line timing, and as the input to the tone generator.

TPA – TIMING PULSE A (Input):
This input is connected to the TPA output of the CDP1802/CDP1804. It is used for horizontal line timing.

INT – INTERRUPT (Output):
This output is connected to the $\overline{INT}$ input of the CDP1802/CDP1804. One interrupt re-

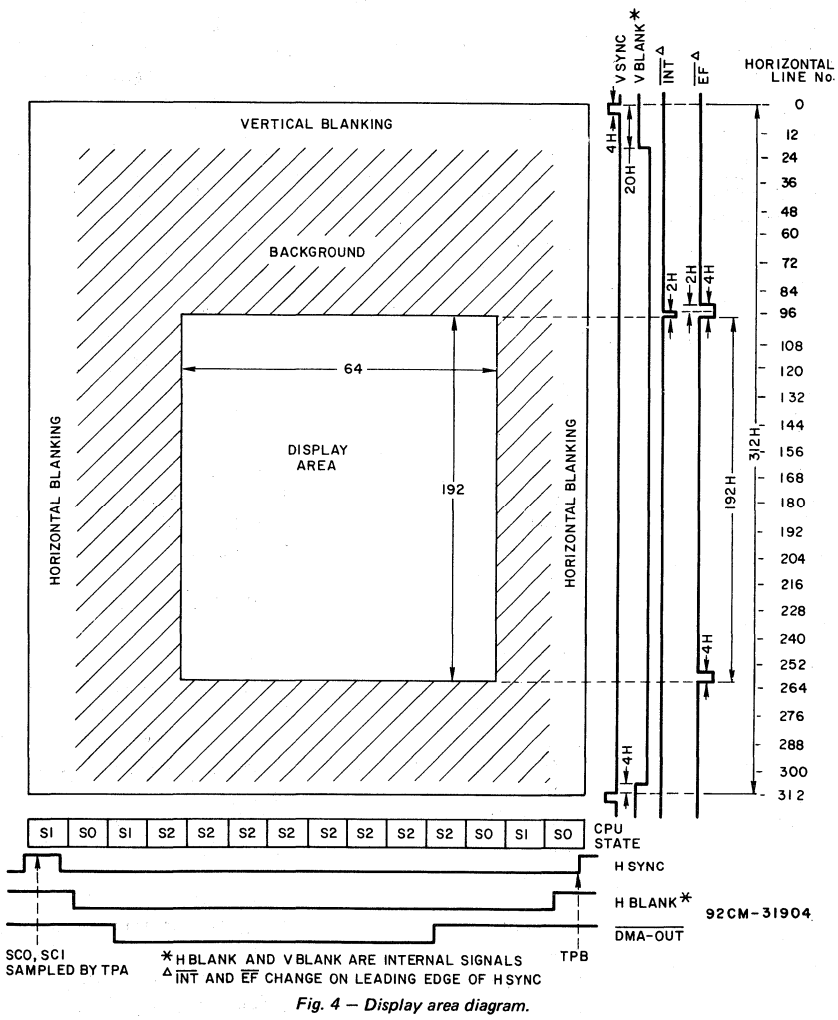


Fig. 4 – Display area diagram.

CDP1864C Types

quest is issued per field. The request is issued two horizontal lines before the display interval, and the signal remains active for two horizontal lines.

DMAO – DMA OUT REQUEST (Output):
This output is connected to the DMAOUT input of the CDP1802/CDP1804. During the display interval the CDP1864 issues this request for 6 machine cycles during the center of each horizontal line (each line time is 14 machine cycles).

CLRIN – CLEAR INPUT:
A low level at this input resets the CDP1864 and generates a low on the CLROUT output. The requests and the loading of color information are inhibited by reset. These remain inhibited until enabled by the appropriate signals. The line counters and horizontal counters are also held reset while CLRIN is low. The Schmitt trigger circuit at this input allows the use of an RC circuit for power-on reset and reset debounce.

AUD – AUDIO OUT:
This is the output of the programmable frequency generator.

V_{DD}:
Positive supply voltage.

CONTROL LINE TRUTH TABLE

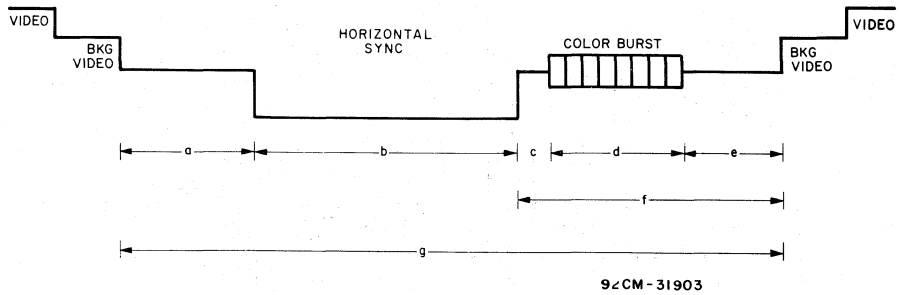
MRD	N2	N0	TPB	OP CODE*	OPERATION
X	0	0	X	–	NO ACTION
X	0	1	1	61 or 69	ENABLE REQUESTS
0	0	1	1	61	STEP BACKGROUND COLOR
0	1	0	1	64	LOAD TONE GENERATOR LATCH
1	1	0	1	6C	DISABLE REQUESTS
X	1	1	X	–	ILLEGAL COMMAND
X	X	X	0	–	NO ACTION

* The OP CODE column is given assuming that N1 = 0. It is actually a DON'T CARE because N1 from the microprocessor is not connected to the CDP1864C.

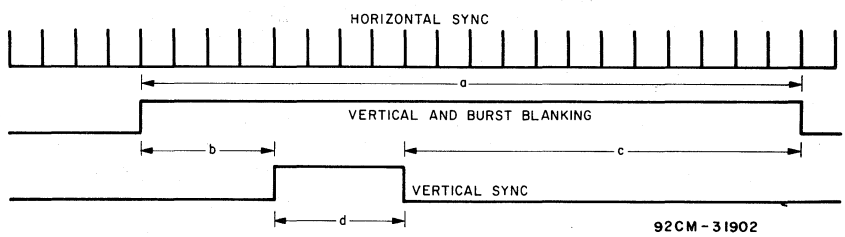
```
Machine Code   Assembly Language                      Comments

72             INTRET: LDXA                           .. RESTORE D
70                     RET                            .. RETURN
C4             INT   : NOP                            .. 3 CYC. INSTR. USED
                                                      .. FOR PGM. SYNC
22                     DEC R2                         .. R2 IS STACK PTR
78                     SAV                            .. T→STACK
22                     DEC R2
52                     STR R2                         .. D→STACK
F8–B0                  A.1(DISMEM)→RO.1               .. LOAD RO WITH
F8–A0                  A.0(DISMEM)→RO.0               .. START.ADDR.OF DISP. MEM
C4, C4                 NOP; NOP                       .. NOPS USED FOR SYNC
E2             DISP  : SEX2
80]                    GLO RO                         .. LINE START ADDR.→D
E2                     SEX2                           .. NOP
20                     DEC RO                         .. RESET RO.1 IF PASS PG
A0]                    PLO RO                         .. LINE START ADDR.→RO.0
E2                     SEX2                           .. NOP
20                     DEC RO                         .. RESET RO.1 IF PASS PG
A0]                    PLO RO                         .. LINE START ADDR.→RO.0
E2                     SEX2                           .. NOP
20                     DEC RO                         .. RESET RO.1 IF PASS PG
A0]                    PLO RO                         .. LINE START ADDR.→RO.0
E2                     SEX2                           .. NOP
20                     DEC RO                         .. RESET RO.1 IF PASS PG
A0]                    PLO RO                         .. LINE START ADDR.→RO.0
E2                     SEX2                           .. NOP
20                     DEC RO                         .. RESET RO.1 IF PASS PG
A0                     PLO RO                         .. REPEATS SAME LINE
3C_                    BN1 DISP                       .. LOOPS 32 TIMES
30–                    BR INTRET                      .. END OF DISPLAY
```

Fig. 5 – Interrupt routine for a 64 x 32 display.

CDP1864C Types



	PAL STANDARD	CDP1864
a	1.55 μs	3.14 μs
b	4.7 ± 0.1 μs	4.57 μs
c	900 ns ± 100 ns	857 ns
d	2.25 ns ± 0.25 μs	2.57 μs
e	2.6 μs	2.0 μs
f	5.8 μs	5.43 μs
g	12.05 μs	13.14 μs
HORZ. FREQ.	15625 Hz	15625 Hz



	PAL STANDARD	CDP1864
a	25 H	24 H
b	2.5 H	4 H
c	20 H	12 H
d	2.5 H	4 H
Burst Blanking	9 H	24 H
Vertical freq. (interlaced)	50 Hz	50
Vertical freq. (non-interlaced)	50 Hz	50.08 Hz

Fig. 6 – Timing diagrams.

CDP1864C Types

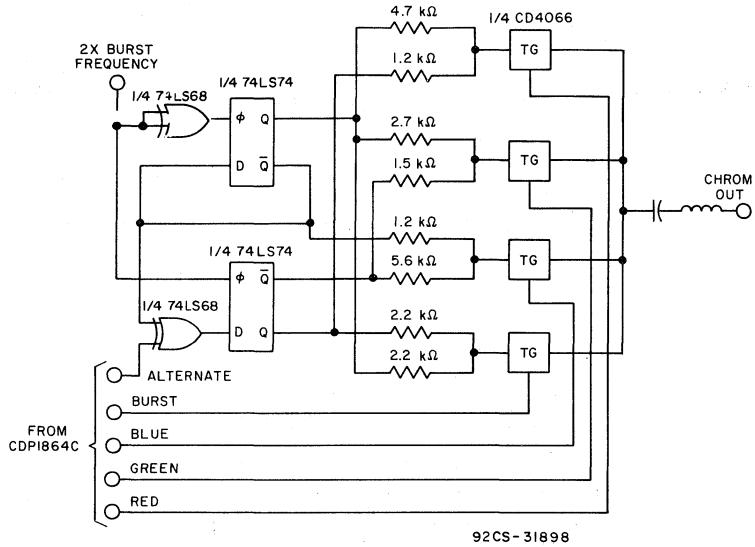


Fig. 7 — Typical color signal generator.

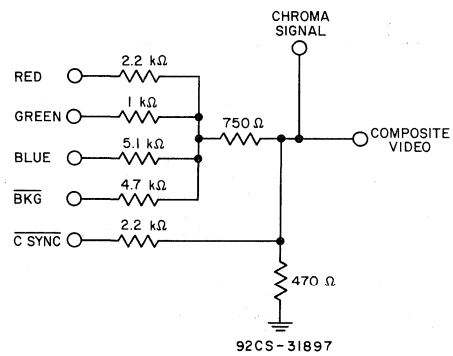


Fig. 8 — Typical composite video network.

CDP1866, CDP1867, CDP1868 Types

4-Bit Latch and Decoder Memory Interfaces

Preliminary Data

Features:

- **Low-power static CMOS technology**
- **Performs memory address latch and decoder functions multiplexed or non-multiplexed**
- **Interfaces directly with the CDP1802 and CDP1804**
- **Single supply voltage, V_{DD} = 4-10.5 V**
- **Allows decoding for systems larger than 4096-words by 8-bits**

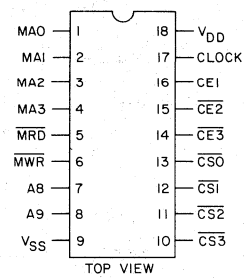
The RCA-CDP1866, CDP1867, and CDP1868 are CMOS 4-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to eight 4096-bit random-access memories to provide a 4096-byte RAM system. All the necessary chip selects are provided as outputs along with additional enable inputs so that in larger memory systems, the 9-chip 4096-byte blocks can be readily accessed.

These devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1866 and CDP1868 are intended for use with 1024-word RAMs and are identical except that in the CDP1868, CE1 and $\overline{CE2}$ are latched and $\overline{CS2}$ is valid on $\overline{MWR}$ only. This allows the CDP1868 to be used in a color display system with the CDP1861 and CDP1862 (see Fig. 9). The CDP1867 is intended for use with 4096-word RAMs.

The CDP1866, CDP1867, and CDP1868 are supplied in an 18-lead hermetic dual-in-line ceramic package (D suffix) and an 18-lead plastic package (E suffix).

TERMINAL DIAGRAM
CDP1866, CDP1868



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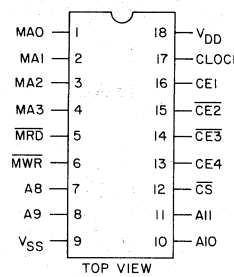
TERMINAL DIAGRAM
CDP1867



92CS-30798R1

CDP1866, CDP1867, CDP1868 Types

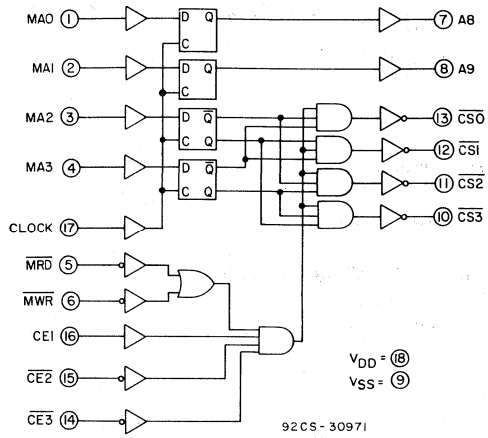


Fig. 1 – Functional diagram for the CDP1866.

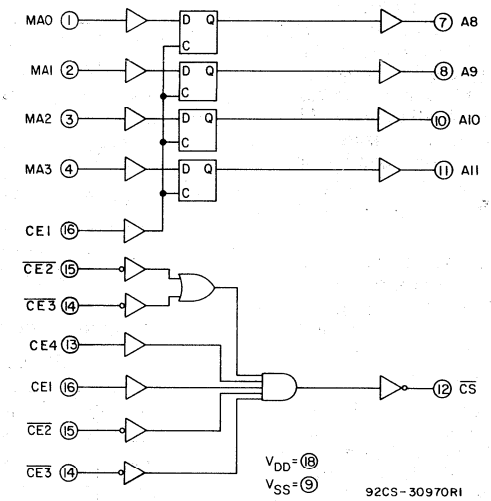


Fig. 2 – Functional diagram for the CDP1867.

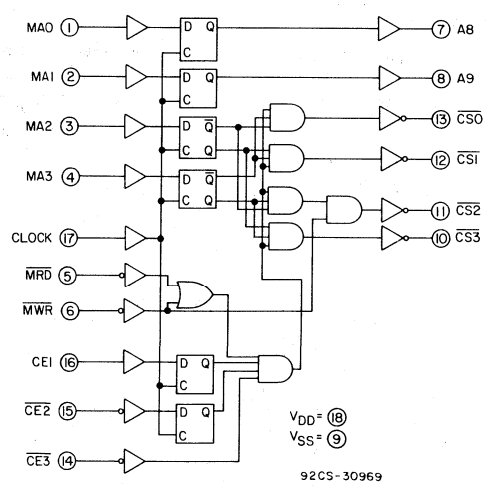


Fig. 3 – Functional diagram for the CDP1868.

CDP1866, CDP1867, CDP1868 Types

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1866, CDP1867, CDP1868		CDP1866C, CDP1867C, CDP1868C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1866 CDP1867 CDP1868			CDP1866C CDP1867C CDP1868C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.†	Max.	Min.	Typ.†	Max.	
Quiescent Device Current, I_L	–	–	5	–	1	10	–	5	50	μA
	–	–	10	–	10	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0,10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0,10	10	−2.6	−5.2	–	–	–	–	
Output Voltage Low Level, V_{OL}▲	–	0,5	5	–	0	0.1	–	0	0.1	V
	–	0,10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH}	–	0,5	5	4.95	5	–	4.95	5	–	
	–	0,10	10	9.95	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	–	–	1.5	V
	1,9	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5, 4.5	–	5	3.5	–	–	3.5	–	–	
	1,9	–	10	7	–	–	–	–	–	
Input Leakage Current, I_{IN}	Any Input	0,5	5	–	–	±1	–	–	±1	μA
		0,10	10	–	–	±1	–	–	–	
Data Retention Current, I_{DR}	V_{DD} = 2.4 V			–	0.01	1	–	0.5	5	μA
Min. Data Retention Voltage, V_{DR}	$V_{DD} = V_{DR}$			–	2	2.4	–	2	2.4	V
Operating Current, I_{DD}*	0,5	0,5	5	–	50	100	–	50	100	μA
	0,10	0,10	10	–	150	300	–	–	–	
Input Capacitance, C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	10	15	–	10	15	pF

† Typical values are for T_A = 25°C and nominal voltage.

* Operating current measured in a CDP1802 system at 2 MHz with outputs floating.

▲ $I_{OL} = I_{OH} = 1\ \mu A$.

CDP1866, CDP1867, CDP1868 Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^oC$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF. See Figs. 4 and 5.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1866			CDP1866C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Time, Memory Address to CLOCK, t_{MACS}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Minimum Hold Time, Memory Address After CLOCK, t_{CLMA}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Minimum CLOCK Pulse Width, t_{CLCL}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Propagation Delay Times:								
Chip Enable to Chip Select, t_{CECS}	5	–	150	225	–	150	225	ns
	10	–	75	125	–	–	–	
MRD or MRW to Chip Select, t_{MCS}	5	–	125	200	–	125	200	
	10	–	65	125	–	–	–	
CLOCK to Chip Select, t_{CLCS}	5	–	175	275	–	175	275	
	10	–	90	150	–	–	–	
CLOCK to Address, t_{CLA}	5	–	125	200	–	125	200	ns
	10	–	65	125	–	–	–	
Memory Address to Chip Select, t_{MACS}	5	–	150	225	–	150	225	
	10	–	75	125	–	–	–	
Memory Address to Address, t_{MAA}	5	–	80	125	–	80	125	
	10	–	40	60	–	–	–	
		CDP1867			CDP1867C			
Minimum Setup Time, Memory Address to CLOCK, t_{MACL}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Minimum Hold Time, Memory Address After CLOCK, t_{CLMA}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Minimum CLOCK Pulse Width, t_{CLCL}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Propagation Delay Times:								
Chip Enable to Chip Select, t_{CECS}	5	–	100	150	–	100	150	ns
	10	–	50	75	–	–	–	
MRD or MRW to Chip Select, t_{MCS}	5	–	80	125	–	80	125	
	10	–	40	60	–	–	–	
CLOCK to Address, t_{CLA}	5	–	125	200	–	125	200	ns
	10	–	65	100	–	–	–	
Memory Address to Address, t_{MAA}	5	–	75	125	–	75	125	
	10	–	40	60	–	–	–	

NOTE 1 = Typical values are for $T_A = 25^oC$ and nominal voltages.
NOTE 2 = Maximum limits of minimum characteristics are the values above which all devices function.

CDP1866, CDP1867, CDP1868 Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ± 5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Fig. 6.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1868			CDP1868C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Setup Times:								
Chip Enable to CLOCK, t_{CECL}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Memory Address to CLOCK, t_{MACL}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Minimum Hold Times:								
Chip Enable After CLOCK, t_{CLCE}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Memory Address After CLOCK, t_{CLMA}	5	–	50	75	–	50	75	
	10	–	25	40	–	–	–	
Minimum CLOCK Pulse Width, t_{CLCL}	5	–	50	75	–	50	75	ns
	10	–	25	40	–	–	–	
Propagation Delay Times:								
CLOCK to Chip Select, t_{CLCS}	5	–	175	275	–	175	275	ns
	10	–	90	150	–	–	–	
Chip Enable to Chip Select, t_{CECS}	5	–	150	225	–	150	225	
	10	–	75	125	–	–	–	
Chip Enable 3 to Chip Select, t_{C3CS}	5	–	150	225	–	150	225	ns
	10	–	75	125	–	–	–	
MRD or MRW to Chip Select, t_{MCS}	5	–	125	200	–	125	200	
	10	–	65	100	–	–	–	
CLOCK to Address, t_{CLA}	5	–	125	200	–	125	200	ns
	10	–	65	100	–	–	–	
Memory Address to Chip Select, t_{MACS}	5	–	125	200	–	125	200	
	10	–	65	100	–	–	–	
Memory Address to Address, t_{MAA}	5	–	80	120	–	80	120	
	10	–	40	60	–	–	–	

NOTE 1: Typical values are for T_A = 25°C and nominal voltages.
NOTE 2: Maximum limits of minimum characteristics are the values above which all devices function.

CDP1866, CDP1867, CDP1868 Types

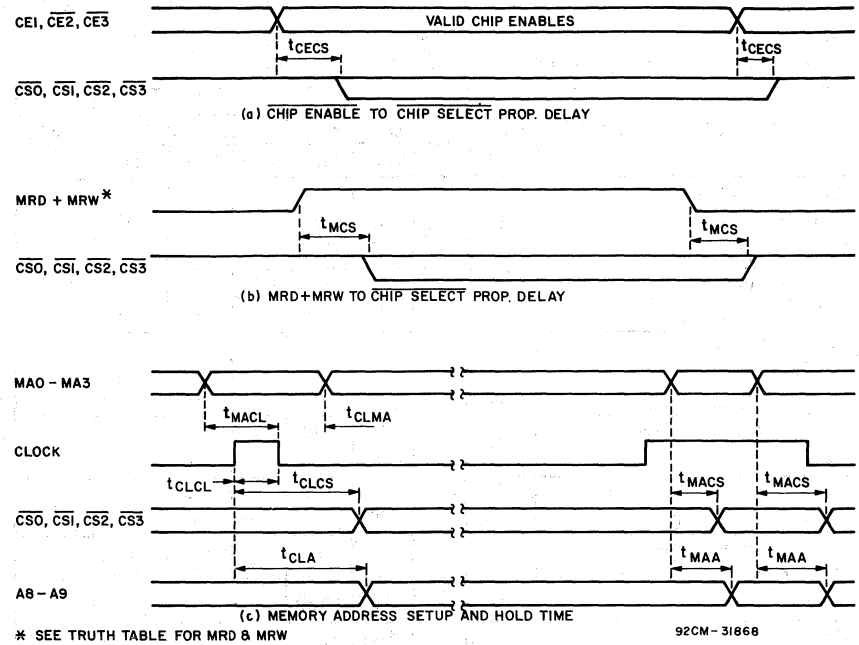
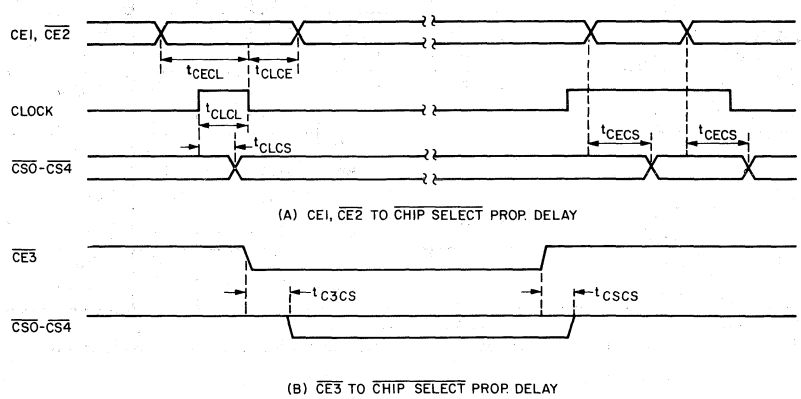
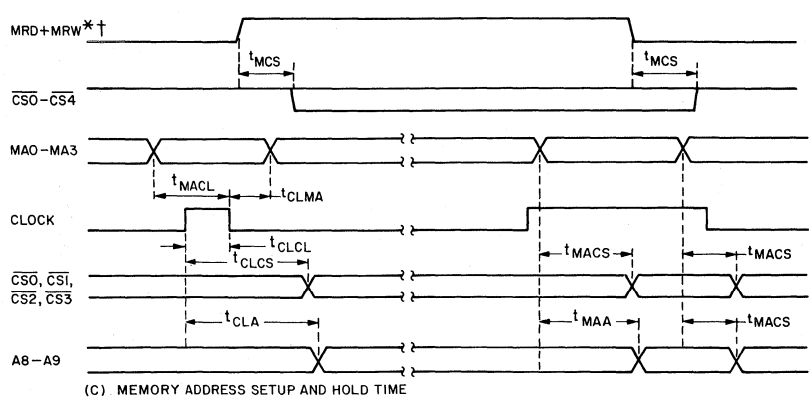


Fig. 4 — CDP1866 timing diagram.





*SEE TRUTH TABLE FOR MRD+MWR
† $\overline{CS2}$ WILL BE VALID ($\overline{CS2}$=0) ONLY IF $\overline{MRW}$ IS LOW REGARDLESS OF $\overline{MRD}$ SIGNAL POLARITY.

Fig. 5 — CDP1868 timing diagram.

CDP1866, CDP1867, CDP1868 Types

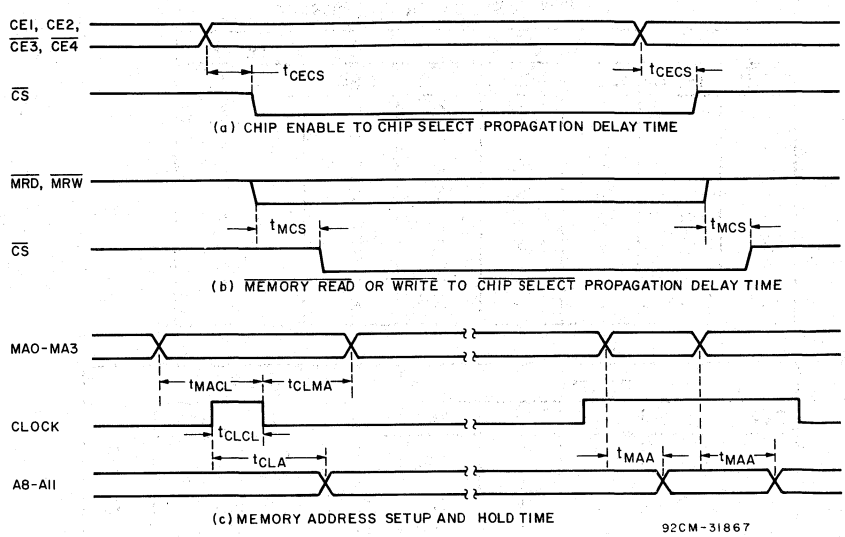


Fig. 6 – CDP1867 timing diagram.

TRUTH TABLES FOR THE CDP1866 AND CDP1868

INPUTS						OUTPUTS				
MRD or MWR	CE1	$\overline{CE2}$	$\overline{CE3}$	CLK	MA2	MA3	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
1	1	0	0	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	1	1
1*	1	0	0	1	0	1	1	1	0*	1
1	1	0	0	1	1	1	1	1	1	0
1	1	0	0	0	X	X	PREVIOUS STATE			
X	X	X	1	X	X	X	1	1	1	1
X	X	1	X	X	X	X	1	1	1	1
X	0	X	X	X	X	X	1	1	1	1
0	X	X	X	X	X	X	1	1	1	1

* In the CDP1868, $\overline{CS2}$ will be valid ($\overline{CS2}$=0) only if $\overline{MRW}$ is low, regardless of the polarity of $\overline{MRD}$.

INPUTS			OUTPUTS	
CLK	MA0	MA1	A8	A9
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1
0	X	X	PREVIOUS STATE	

$\overline{MRD}$	$\overline{MWR}$	MRD or MWR
0	0	1
0	1	1
1	0	1
1	1	0

CDP1866, CDP1867, CDP1868 Types

TRUTH TABLES FOR THE CDP1867

INPUTS						OUTPUT
$\overline{MRD}$	$\overline{MWR}$	CE1	$\overline{CE2}$	$\overline{CE3}$	CE4	$\overline{CS}$
0	0	1	0	0	1	0
0	1	1	0	0	1	0
1	0	1	0	0	1	0
1	1	X	X	X	X	1
X	X	X	X	X	0	1
X	X	X	X	1	X	1
X	X	X	1	X	X	1
X	X	0	X	X	X	1

INPUTS					OUTPUTS			
CLK	MA0	MA1	MA2	MA3	A8	A9	A10	A11
1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
1	0	0	1	0	0	0	1	0
1	0	0	1	1	0	0	1	1
1	0	1	0	0	0	1	0	0
1	0	1	0	1	0	1	0	1
1	0	1	1	0	0	1	1	0
1	0	1	1	1	0	1	1	1
1	1	0	0	0	1	0	0	0
1	1	0	0	1	1	0	0	1
1	1	0	1	0	1	0	1	0
1	1	0	1	1	1	0	1	1
1	1	1	0	0	1	1	0	0
1	1	1	0	1	1	1	0	1
1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1
0	X	X	X	X	PREVIOUS STATE			

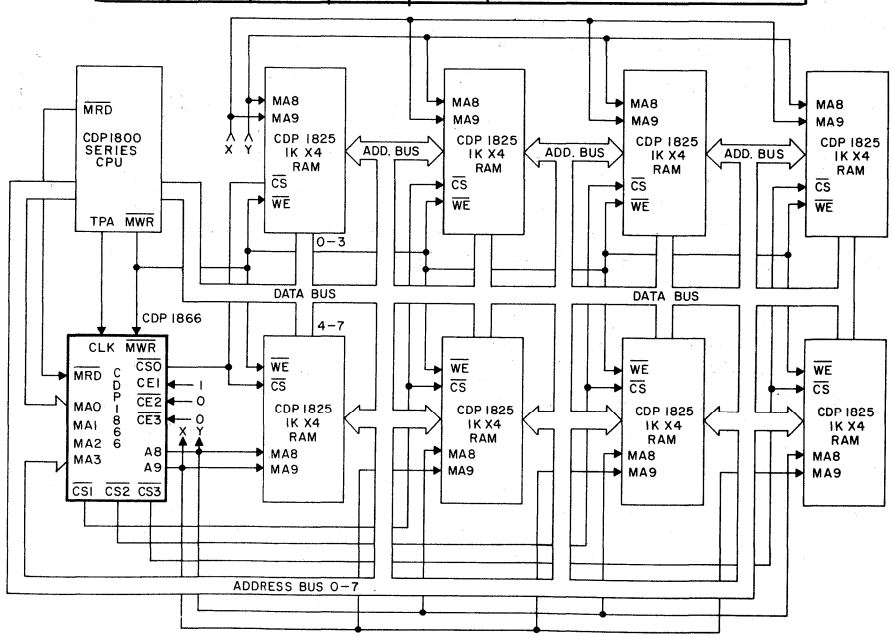


Fig. 7 — 4096-word by 4-bit random-access memory system using the CDP1866.

CDP1866, CDP1867, CDP1868 Types

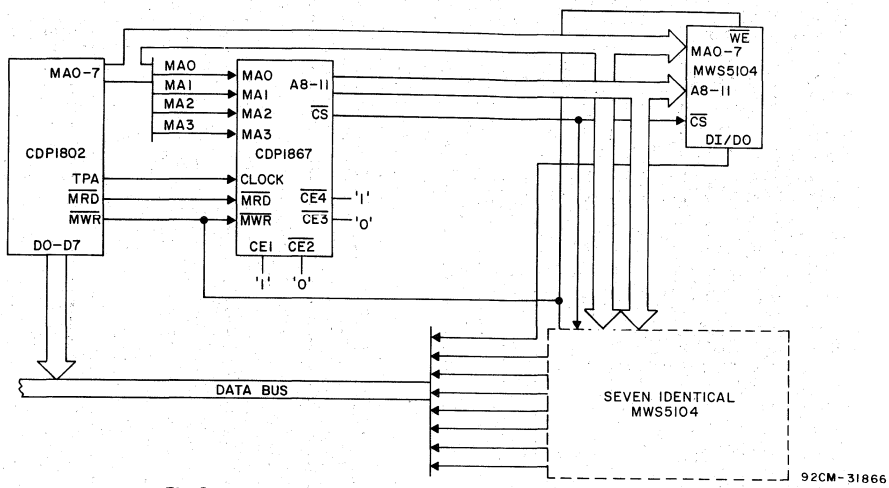
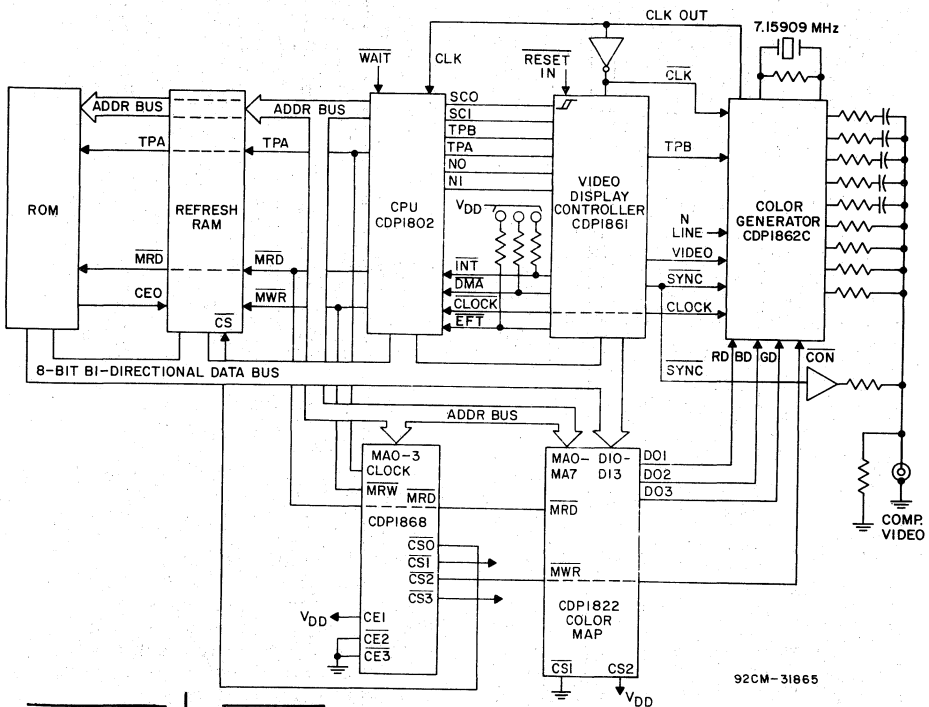


Fig. 8 — 4096-word by 8-bit RAM system using the CDP1867.



CHIP SELECT	ADDRESS
CS0	0000 - 03FF
CS1	0400 - 07FF
CS2	0800 - 0BFF
CS3	0C00 - 0FFF

Fig. 9 — Typical color display system using the CDP1868.

The CDP1868 can be used in a color display system to write to the refresh RAM and the color map RAM at different address locations, as shown in Fig. 9. Both the refresh RAM and the color map RAM are read from the same address. The purpose of reading from the same address is that when a byte of data from the refresh RAM is sent to the video display controller (CDP1861), an additional 3 bits of color information are needed from the color map RAM for the color generator (CDP1862). In Fig. 9, the bit display data are written into the refresh RAM at 0000-00FF. The color display data are written into the color map RAM at locations 0800-08FF. Both are read at locations 0000-00FF.

CDP1869C, CDP1870C Types

COS/MOS Video Interface System

Preliminary Data

Features:

- *CMOS technology*
- *Directly interfaces with CDP1800 series microprocessors*
- *Dot frequency = 5.67 MHz (PAL = 5.626 MHz). Produces maximum feasible resolution for antenna input*
- *CPU clock independent (½ dot rate provided)*
- *CPU not involved in screen refresh*
- *Produces extremely low chip-count systems for games and/or "intelligent" terminals*
- *Graphics and motion through character selection or bit map in character memory*
- *Up to 256 different characters*
- *Character memory may be any combination of ROM or RAM, allowing modification of characters and graphics*
- *Programmable for 24 lines × 40 char/line or 12 lines × 20 char/line*
- *6 × 8 or 6 × 16 char. matrix (6 × 9 for PAL)*
- *Character generation approach minimizes memory*
- *PAL and NTSC compatible*
- *Page memory is accessed as extension of CPU memory during non-display time*
- *Composite sync, composite luminance, and composite chrominance outputs*
- *Programmable background color*
- *Programmable color format control allowing several modes for high resolution color*
- *Hardware scroll capability*
- *Audio generator and white noise: 8 octaves, each able to select 128 tones; single freq. to white noise generator. Both tones and white noise can be enveloped from 0 volts to 0.75 V_{DD} in 16 steps*
- *External horizontal and vertical sync inputs allow for integration into existing chassis for character-on-picture overlays*
- *Teletext compatible*

The RCA-CDP1869C and CDP1870C video interface system is designed for use in CDP1800-Series Microprocessor systems. It consists of the CDP1869C address and sound generator and the CDP1870C color video generator. These two LSI COS/MOS circuits interface directly with the CDP1802 and CDP1804 to simplify control and minimize external components. (See Fig. 1.)

The VIS offers a variety of formats for the display and modification of data under software control, with either NTSC or PAL compatible output signals. The display device can be a video monitor or a standard TV receiver with an RF modulator. Composite sync, luminance, and chrominance are combined externally to form a single system-output. External sync inputs are also provided to allow picture overlays in existing TV chassis.

A sound output provides white noise and eight octaves of programmable tones. The output amplitude is variable in 16 steps from 0 V to 0.75 V_{DD}. This output is particularly useful in video game applications.

The CPU is clock independent of the VIS and is not involved in screen refresh, although a CPU clock output (½ dot rate) is provided. At this clock rate 787 instructions can be executed during non-display time. $\overline{\text{PRE DISPLAY}}$ provides synchronization between the CPU and the VIS. The system configurations for the CDP1869C/CDP1870C VIS are almost unlimited due to:

(Cont'd on page 2)

CDP1869C, CDP1870C Types

PAGE MEMORY

- 20 Characters x 12 Lines—Requires 240 Bytes of RAM
- 40 Characters x 24 Lines—Requires 960 Bytes of RAM

Character Memory—Can be RAM or ROM

- 32 Different (or any Combination of) Characters—Requires 256 Bytes (NTSC)
- 64 Different Characters—Requires 512 Bytes (NTSC)
- 128 Different Characters—Requires 1024 Bytes (NTSC)
- 256 Different Characters—Requires 2048 Bytes (NTSC)

Color

Color information may be stored in the two extra bits in each character byte (characters are only six dots wide), providing a choice of one of four colors for each character. With 128 different characters, seven bits are required in the page memory and the eighth bit expands color to essentially eight colors.

Graphics and Motion

Graphics and motion may be accomplished with several methods in this system. These methods may be divided into two basic techniques. The first is by character selection. In this approach the desired graphics and motion symbols are stored in ROM or RAM. In a system where the character memory is all ROM, all the possible required positions within a character space are stored in the ROM. Graphics and motion are accomplished by selecting the appropriate one for each screen position. If the character memory is RAM then all combinations need not be stored in the character memory since they can be modified as required during operation.

The second technique is basically for more sophisticated motion. In this technique a block of characters in the RAM character memory are treated as a continuous surface. These characters are placed in adjacent locations on the screen to provide a background. The object is moved through this background using a bit map approach. As the object ap-

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4	6.5	V
Input Voltage Range	–	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time	5	–	5	μs
Clock Input Frequency, f_{CL}	5	7.15909		MHz

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

CDP1869C, CDP1870C Types

proaches the "edge" of these characters as selected on the screen the background is moved. For example, if the object approaches the edge of the last background character on the left, then the background characters on the right are moved to the left side via the page memory. Thus as the object moves through these background characters (a continuous surface) it moves across the screen.

Operation

CDP1869C—Address and Sound Generator

This circuit formats and controls sound, page-memory addressing, and character-memory addressing. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1870C timing signals. Control and multiplexing is determined by internal registers, which are loaded by four CPU I/O instructions. Data to the command registers are loaded from the 8 multiplexed address inputs (MA0/8-MA7/15). The high-order byte (MA8-MA15) is latched by the high-to-low transition of TPA, to provide up to 16 internal data bits.The I/O instruction data are latched by the high-to-low transition of TPB (Fig. 2).

OUT 64 Instruction—This instruction uses 15 data bits(MA0-MA14) to control the tone output function. (Bit 15 is unused, but must be latched as a low). Bits MA0-MA3 control the tone output amplitude using an on-chip binary R/2R ladder network to produce a varying output amplitude in 16 steps. Bits MA4-MA6 control the tone output frequency range. Eight octaves are available (TABLE 1). Within each octave, the input frequency is divided by the N + 1 value on bits MA8-MA14, producing up to 128 different frequencies. The divided output is a square-wave signal gated on or off by bit MA7. A high on MA7 turns the tone output off. If both the tone and white noise are turned off, the sound output impedance is equal to 2.5R.

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
				CDP1869C CDP1870C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	0, 5	5	–	100	500	μA
Output Low Drive (Sink) Current, I_{OL} (Except $\overline{XTAL}$)	0.4	0, 5	5	2	2.4	–	mA
$\overline{XTAL}$ Output, I_{OL}	0.4	0, 5	5	150	200	–	μA
Output High Drive (Source) Current, I_{OH} (Except $\overline{XTAL}$	4.6	0, 5	5	−1.6	−1.8	–	mA
$\overline{XTAL}$ Output, I_{OH}	4.6	0, 5	5	−150	−200	–	μA
Output Voltage Low-Level, V_{OL}	–	0, 5	5	–	0	0.05	V
Output Voltage High Level, V_{OH}	–	0, 5	5	4.95	5	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	V
Input High Voltage, V_{IH}	0.5, 4.5	–	5	3.5	–	–	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	–	±0.1	±1	μA
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	–	±0.2	±2	μA

* Typical values are for T_A = 25°C and nominal voltage.

CDP1869C, CDP1870C Types

OUT 65 Instruction—This instruction uses 13 data bits. (Bits MA1, MA2, and MA4 are unused and need not be programmed). The higher-order byte (MA8-MA15) is used to control the white-noise output function. Bits MA8-MA11 control the white-noise output amplitude using an on-chip binary R/2R ladder network to provide a varying output amplitude in 16 steps. Bits MA12-MA14 control the white-noise output frequency range. Eight octaves are available (TABLE 2). The result is an explosion-type sound effect useful in TV game systems. The white-noise output is gated on or off by bit MA15. A high on MA15 turns the white-noise output off. If both the tone and white noise are on, a combined amplitude and frequency output results.

The lower-order byte (MA0-MA7) provides screen format control. The CMEM ACCESS MODE Bit (MA0) is used in conjunction with the OUT 66 instruction to control the character memory READ/WRITE functions. A high on MA0 enables the character access mode.

The NTSC bit (MA3) is used to select either NTSC or PAL compatible signal timing (TABLE 7). A high on MA3 selects NTSC operation.

The 16-ROW HI-RES bit (MA5) is used to control the vertical resolution of each character. A low on MA5 defines each character as a 6 x 8 dot matrix. a high on MA5 defines each character as a 6 x 16 dot matrix, with each of the 16 vertical rows able to contain different data. The 16-ROW HI-RES bit (MA5) must be low if the double-page bit (MA6) is high.

The DOUBLE-PAGE bit (MA6) is used to select the function of the CMA3/PMA10 output. A low on MA6 selects the single-page mode, in which the maximum page memory size is limited to 960 bytes. The VIS will normally do a roll screen operation when the end of the display page is reached. In the single-page mode, the CMA3/PMA10 output functions as CMA3 to expand the character memory if the 16-bit HI-RES bit is high. A high on MA6 selects the double-page mode. In this mode, the CMA3/PMA10 output functions as PMA10 to expand the page-memory ad-

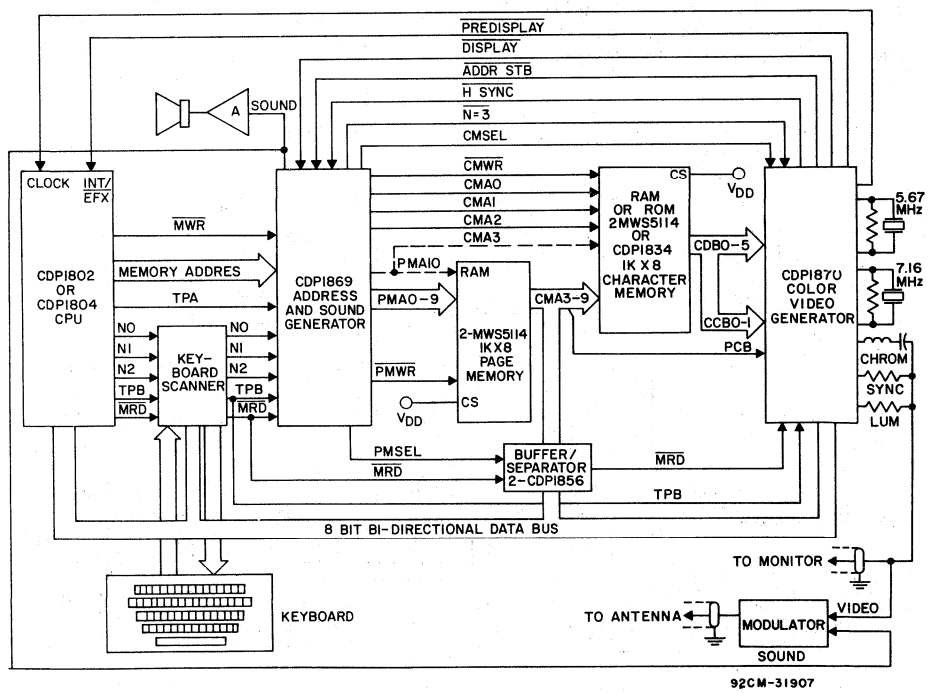


Fig. 1 - System diagram.

CDP1869C, CDP1870C Types

dressing. The maximum page-memory size is extended to 1920 bytes. At the end of the first page a hardware scroll automatically occurs. The next line entered is displayed at the bottom of the screen, with the previous page shifted up one line. The old top line is no longer displayed, but is still in memory.

The FRES VERT bit (MA7) controls the full screen vertical resolution of the display. A low on MA7 sets the maximum resolution to 12 lines of characters. A high on MA7 sets the maximum resolution to 24 lines of characters.

All valid display format combinations are shown in TABLE 6, along with the page and character-memory requirements. Fig. 4 shows the relative character matrix sizes.

OUT 66 Instruction—This instruction uses 11 data bits (MA0-MA10) to load the page-memory address-register bits (PMA0-PMA10). If the CMEM ACCESS MODE is set (high), the page-memory address data are latched to provide character selection during a character-memory READ/WRITE operation. If the DOUBLE-PAGE bit is not set (low), PMA10 is not used and does not have to be programmed.

If the CMEM ACCESS MODE is not set (low), the 8 multiplexed inputs (MA0/8-MA7/15) are multiplexed to the page-memory address outputs (PMA0-PMA10) and the page memory functions as an extension of the CPU memory. When the page memory is selected (F800-FFFF), the $\overline{\text{CMWR}}$ output and the PMSEL output are enabled. The CMWR output is connected to the WRITE input of the page memory. When using memories with a common READ/WRITE input (RCA MWS5114), the PMSEL output is connected to the select input of the data-bus buffer/separator (Fig. 1).

When the character memory is selected (F400-F7FF), the 8 multiplexed inputs (MA0/8-MA7/15) are multiplexed to the character memory address outputs (CMA0-CMA3), and the $\overline{\text{CMWR}}$ and CMSEL outputs are enabled. The $\overline{\text{CMWR}}$ output is connected to the WRITE input of the character memory. The CMSEL output is connected to the CMSEL input of the CDP1870C to provide data bus multiplexing. If the DOUBLE-PAGE bit is set (high), CMA3 is not used and bit MA3 does not have to be programmed.

Out 67 Instruction—This instruction uses 9 data bits (MA2-MA10) to load the home-address register bits (HMA2-HMA10). The home address determines which line of characters, from the page memory, is displayed at the top left-hand corner of the screen. In the FULL RES HORZ MODE (CDP1870C), the home address must be an even multiple of 40. In the HALF RES HORZ MODE (CDP1870C), the home address must be an even multiple of 20. Therefore, the HMA0 and HMA1 bits are not used and do not have to be programmed.

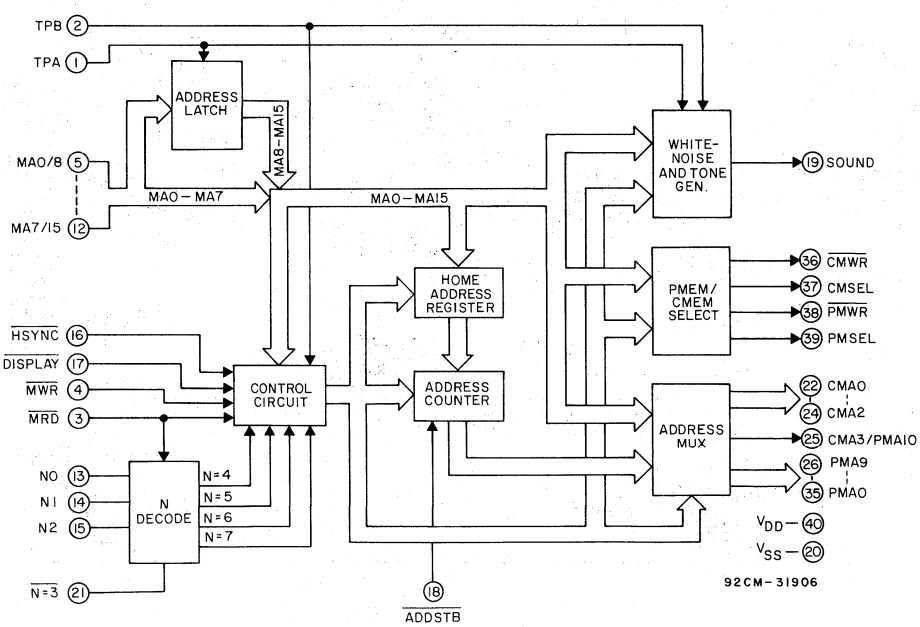


Fig. 2 - CDP1869C block diagram.

CDP1869C, CDP1870C Types

After the last line of characters has been displayed, the home address is reloaded into the page-memory address counter to begin the next display frame. When final page memory address count (maximum page-memory size in TABLE 6) is reached prior to the end of the display, zero is loaded into the address counter. Changing the home address can be used to scroll through the page memory. In the double-page mode, line zero will scroll onto the screen after the final line, as described above.

CDP1870C—Color Video Generator

This circuit formats and controls the TV sync, video, and color information. It also provides synchronization timing to the CDP1869C and the CPU. The character-memory data I/O lines are multiplexed through the CDP1870C to the CPU 8-bit bidirectional data bus. This is accomplished by software instructions, data from the CPU, and hardware interaction with the CDP1869C timing signals. Control and multiplexing is determined by a single internal command register, which is loaded by a CPU I/O instruction. Data to the command register are loaded from the 8-bit bidirectional data bus, which is latched by the high-to-low transition of TPB when the $\overline{MRD}$ and the $\overline{N=3}$ inputs are at a logic 0 (Fig. 3).

OUT 63 Instruction—This instruction uses 8 data bits to control the internal format and timing functions. The BKG GREEN, BKG BLUE, BKG RED bits (BUS0-BUS2) provide a binary selection of eight screen background colors, as shown in TABLE 5. The CFC bit (BUS 3) selects the color format control function (TABLE 4) When the CFC bit is low, the background luminance and chrominance are selected by the BKG GREEN, BKG BLUE, and BKG RED control bits. The dot chrominance and luminance are selected by CCBO, CCBI, and PCB inputs. Operation is the same when the CFC bit is high, except that the dot chrominance is now selected by the BKG GREEN, BKG BLUE, and BKG RED control bits. The DISP OFF bit (BUS 4) is used to turn the screen display off. When the DISP-OFF bit is high, the PAL CHROM, NTSC CHROM, and LUM outputs are held at the background color and the $\overline{ADDSTB}$, $\overline{PREDISPLAY}$, and $\overline{DISPLAY}$ outputs are held at a high level. However, the $\overline{COMPSYNC}$, $\overline{HSYNC}$, and CPUCLK outputs continue to supply synchronization timing. This display-off condition allows the CPU to access the VIS, page memory, and character memory asynchronously. Any change in this bit is only recognized at the end of the frame. The COLB0 and COLB1 bits (BUS 5, BUS 6) provide a binary selection of 4 character-color control modes, as shown in TABLE 3. These 4 modes control which color bit inputs (CCB0, CCB1, PCB) select a particular character color (TABLE 5). The FRES HORZ bit (BUS 7) controls the full screen horizontal resolution of the display. A low on BUS 7 sets the maximum resolution to 20 characters per line. A high on BUS 7 sets the maximum

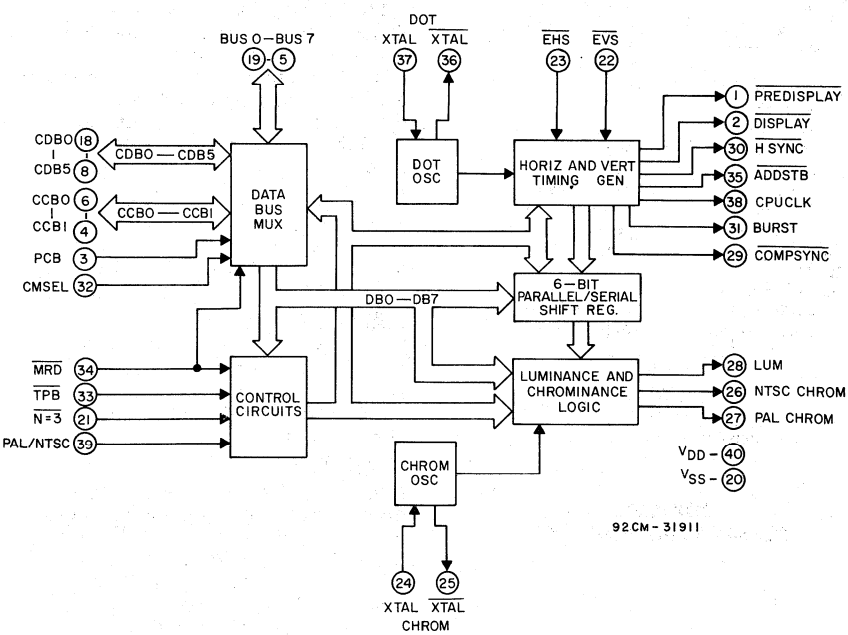


Fig. 3 - CDP1870C block diagram.

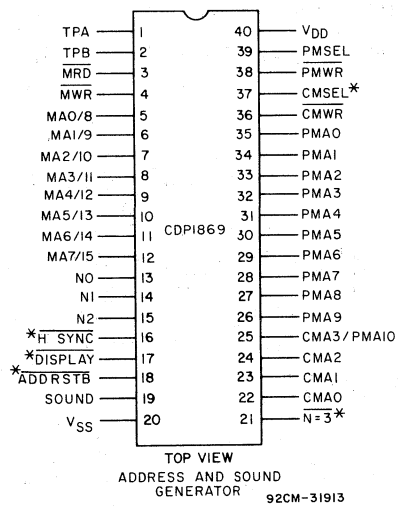
CDP1869C, CDP1870C Types

resolution to 40 characters per line. All valid display format combinations are shown in TABLE 6.

The CDP1870C uses two separate input frequencies. On-chip oscillators are provided, requiring only external crystal circuits. One input circuit provides the dot clock frequency, from which SYNC and ADDSTB timing is derived. The dot frequency, divided by two, provides a CPU CLK output. The other input circuit provides the color reference and chrominance frequencies. The NTSC CHROM, PALCHROM, and LUM outputs include on-chip summing resistors to reduce the external components required. The outputs are connected to the COMPSYNC output to provide a single video signal, which may be used to drive a video monitor directly or a standard TV receiver through an RF modulator circuit.

The EVS and EHS inputs may be used to sync the VIS from an existing TV chassis to provide picture overlay and teletext operations. The PAL/NTSC input is used to select either European or U.S. Operation (TABLE 7).

The VIS does not provide for an external system reset. All command and format instructions must be executed before proper operation in initiated.



*INTERCHIP CONNECTIONS

CDP1869C TERMINAL ASSIGNMENT

FUNCTIONAL DESCRIPTION OF CDP1869C TERMINALS

TPA (Input):

A positive pulse from the CPU that occurs once in each machine cycle. The trailing edge of TPA is used to latch the higher-order byte of the 16-bit memory address. TPA is also one of the frequency generator input clocks.

TPB (Input):
A positive pulse from the CPU that occurs once in each machine cycle, following TPA. It is used to latch the various internal command registers. TPB is also one of the frequency generator input clocks.

MRD (Input):
A low level from the CPU, indicating a memory read cycle. It is used to provide various latch and control functions.

MWR (Input):
A negative pulse from the CPU, appearing in a memory write cycle after the address lines have stabilized. It is used to gate various latch and control functions.

MA0/8-MA7/15 (Inputs):
The 8 memory address lines. The higher-order byte of a 16-bit CDP1802 or CDP1804 memory address appears on the memory address lines MA0-MA7 first, and is latched by the high-to-low transition of TPA. These 8-lines serve a dual purpose. They can be used to provide direct address information to the page or character memories or they can be used to provide data to the command registers.

N0 to N2 (Inputs):
These lines are used to issue command codes during an I/O instruction from the CPU. Their state is the same as the corresponding bits in the CPU N register. The three N bits are internally decoded with MRD to provide various latch and control functions.

HSYNC (Input):
The horizontal sync signal from a CDP1870C. This signal provides synchronization between the CDP1869C and the CDP1870C timing signals.

DISPLAY (Input):
This signal from the CDP1870 indicates that a screen refresh is in progress. This signal provides synchronization between the CDP1869C and the CDP1870C timing signals.

ADDSTB (Output):
Negative pulses from a CDP1870C that provide page and character-memory address clock timing. ADDSTB = dot clock ÷ 6 (40 character display). ADDSTB = dot clock ÷ 12 (20 character display). Only 40 or 20 pulses are generated per horizontal line, and no pulses occur during non-display time.

CDP1869C, CDP1870C Types

SOUND (Output):
This output provides two types of frequency signals that can be selected either individually or in combination. The first type provides single frequency tones in 8 selectable ranges, with 128 different tones in each range (TABLE 1). The second type provides a white-noise output in 8 selectable ranges, with the white noise consisting of all 128 tones of each range (TABLE 2). Both tone and white-noise outputs are programmable from 0 volts to 0.75 V_{DD} in 16 steps.

V_{SS}:
Ground

$\overline{N=3}$ (Output):
This output from the internally decoded N bits is normally connected to a CDP1870C. It is used to select the CDP1870C command register.

CMA0-CMA2—CHARACTER-MEMORY ADDRESS (Outputs):
The character memory address outputs. These three outputs function as character-row selects. During a screen refresh the address data are provided by an internal counter, which is controlled by $\overline{HSYNC}$, to provide character information in one of eight formats (Fig. 4). During non-refresh periods the address data are provided by the MA0-MA2 inputs as an extension of the CPU memory.

CMA3/PMA10 (Output):
This output signal serves a dual purpose. In the 16-ROW HIGH-RESOLUTION character mode (command bit 16 = 1) this output represents CMA3 and its function is identical to the CMA0-CMA2 outputs. In the double-page mode (command bit DP = 1) this output represents PMA10 and its function is identical to the PMA0-PMA9 outputs.

PMA0-PMA9—PAGE-MEMORY ADDRESS (Output):
These ten page-memory address outputs access the page memory data, 7 bits of which are used to address the character memory. The spare bit (Bit 8) may be used to expand the color information. During a screen refresh the address data are provided by an internal counter, which is controlled by $\overline{ADDSTB}$ to provide page-memory information in one of four formats (TABLE 6). During non-refresh periods the address data are provided by the MA0/8-MA9/15 inputs as an extension of the CPU memory.

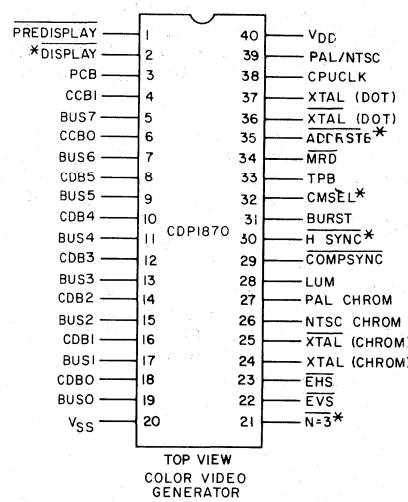
$\overline{CMWR}$—CHARACTER-MEMORY WRITE (Output):
CHARACTER-MEMORY WRITE is an output signal that is connected to the WRITE input of the character memory. This output provides a delayed $\overline{MWR}$ pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF).

CMSEL—CHARACTER-MEMORY SELECT (Output):
CHARACTER-MEMORY SELECT is an output signal that is connected to the CDP1870C CMSEL input. This output provides a delayed positive pulse during non-display periods, when the character memory is selected by the MA10-MA15 inputs (F400-F7FF) and $\overline{MRD}$ or $\overline{MWR}$ is low.

$\overline{PMWR}$—PAGE-MEMORY WRITE (Output):
PAGE-MEMORY-WRITE is an output signal that is connected to the WRITE input of the page memory. This output provides a delayed $\overline{MWR}$ pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800-FFFF).

PMSEL—PAGE-MEMORY SELECT (Output):
PAGE-MEMORY SELECT is an output signal that is connected to an external bus separator. This output provides a delayed positive chip enable pulse during non-display periods, when the page memory is selected by the MA11-MA15 inputs (F800-FFFF) and $\overline{MRD}$ or $\overline{MWR}$ is low.

V_{DD}:
POSITIVE SUPPLY VOLTAGE.



TOP VIEW
COLOR VIDEO GENERATOR

92CM-31913

*INTERCHIP CONNECTIONS

CDP1870C TERMINAL ASSIGNMENT

CDP1869C, CDP1870C Types

FUNCTIONAL DESCRIPTION OF CDP1870C TERMINALS

$\overline{\text{PREDISPLAY}}$ (Output):
An output signal that goes low one horizontal line before the start of the display field. This output may be connected to the CPU to provide advance warning of a refresh operation.

$\overline{\text{DISPLAY}}$ (Output):
An output signal that is low during the display field. This signal is connected to the CDP1869C to provide synchronization timing during a screen refresh.

PCB—PAGE-MEMORY COLOR BIT (Input):
The page-memory color bit expands the character color information to 3 bits (8 colors). (Table 3)

CCB0, CCB1—CHARACTER-MEMORY COLOR BITS (Inputs):
The character memory color bit inputs provide character color data. These two inputs select one of four colors (Table 3) during screen refresh periods. When the CMSEL input is low during non-display periods, CCB0 and CCB1 are multiplexed to the CPU data bus (BUS 6, BUS 7) to provide character READ/WRITE data.

CDB0-CDB5—CHARACTER-MEMORY DATA BITS (Inputs):
The character-memory data bit inputs provide character data during screen refresh periods. When the CMSEL input is high during non-display periods, CDB0-CDB5 are multiplexed to the CPU data bus (BUS 0-BUS 5) to provide character READ/WRITE data.

BUS 0-BUS 7:
The 8-bit bidirectional data bus that is normally connected directly to the CPU. During non-display periods, these I/O lines serve a dual function. If the CMSEL input is high, BUS 0-BUS 7 provide character-memory READ/WRITE data. If the $\overline{N=3}$ input (OUT 3 instruction) is low, BUS 0-BUS 7 provide input data to the CDP1870C command register. These data are latched on the high-to-low transition of TPB when $\overline{\text{MRD}}$ is low.

VSS:
GROUND.

$\overline{N=3}$ (Input):
An input signal from the CDP1869C that is low during an OUT 3 instruction from the CPU. This input is used to select the CDP1870C command register.

$\overline{\text{EVS}}$, $\overline{\text{EHS}}$—EXTERNAL VERTICAL SIGNAL, EXTERNAL HORIZONTAL SIGNAL (Inputs):
The external vertical and horizontal sync signals synchronize the VIS to an external system. When not used, these inputs must be connected high.

XTAL, $\overline{\text{XTAL}}$ (CHROM)—COLOR CHROMINANCE CRYSTAL (Inputs):
The color chrominance crystal inputs are normally connected to a 7.15909-MHz crystal (NTSC) or an 8.867236-MHz crystal (PAL) to provide a burst and color data input clock. The XTAL input may be connected to an external generator.

NTSC CHROM (Output):
The United States Standard Color Video Signal (NTSC). This output provides a composite signal containing chrominance information and 11 cycles of the color reference signal.

PAL CHROM (Output):
The European standard color video signal (PAL). This output provides a composite signal containing chrominance information and 14 cycles of the color reference signal.

LUM—LUMINANCE (Output):
The luminance output signal provides video dot brightness information.

$\overline{\text{COMPSYNC}}$ (Output):
The composite TV synchronization signal provides negative pulses at the line (horizontal) and frame (vertical) rates.

$\overline{\text{HSYNC}}$ (Output):
The horizontal synchronization signal provides a negative pulse at the line rate. It is connected to the CDP1869C to control timing synchronization.

BURST (Output):
This output provides a positive pulse following the horizontal sync pulse. It indicates when the color reference signal is being outputted.

CMSEL—CHARACTER-MEMORY SELECT (Input):
The character-memory select input, from the CDP1869C, indicates a character-memory READ/WRITE operation. When CMSEL is high, the 8-bit bidirectional data bus from the CPU is multiplexed to the CCB0, CCB1, and CDB0-CDB5 I/O lines to provide character-memory data. This input is active only during non-display periods.

TPB (Input):
A positive pulse from the CPU that occurs once in each machine cycle, following the TPA pulse. This input pulse is used to latch the CDP1870C command register data on the high-to-low transition, when the $\overline{N=3}$ and $\overline{\text{MRD}}$ inputs are low.

$\overline{\text{MRD}}$—MEMORY READ (Input):
A low-level input from the CPU indicating a memory READ cycle. This signal enables the command register clock and selects the direction of data flow in the data bus multiplexer. When this signal is low, a READ operation is in progress.

CDP1869C, CDP1870C Types

ADDSTB—MEMORY ADDRESS STROBE (Output):
The MEMORY ADDRESS STROBE output signal is connected to the CDP1869C to provide the page and character-memory address counter clock.

XTAL, XTAL (DOT)—DOT CRYSTAL (Inputs):
The dot crystal inputs are normally connected to a 5.67-MHz crystal (NTSC) or a 5.626-MHz crystal (PAL) that is used to provide horizontal, vertical, and control timing. The XTAL input may be connected to an external generator.

CPUCLK—CLOCK (Output):
A clock output equal to ½ the dot frequency. It may be connected to the CPU CLOCK input terminal. At this frequency, 2947 instructions per frame are available, with 787 instructions occurring during the non-display period.

PAL (Input):
This input selects either PAL or NTSC operation. When the PAL/NTSC input is high, the VIS provides PAL compatible output signals. When the PAL/NTSC input is low, the VIS provides NTSC compatible output signals.

VDD:
POSITIVE SUPPLY VOLTAGE.

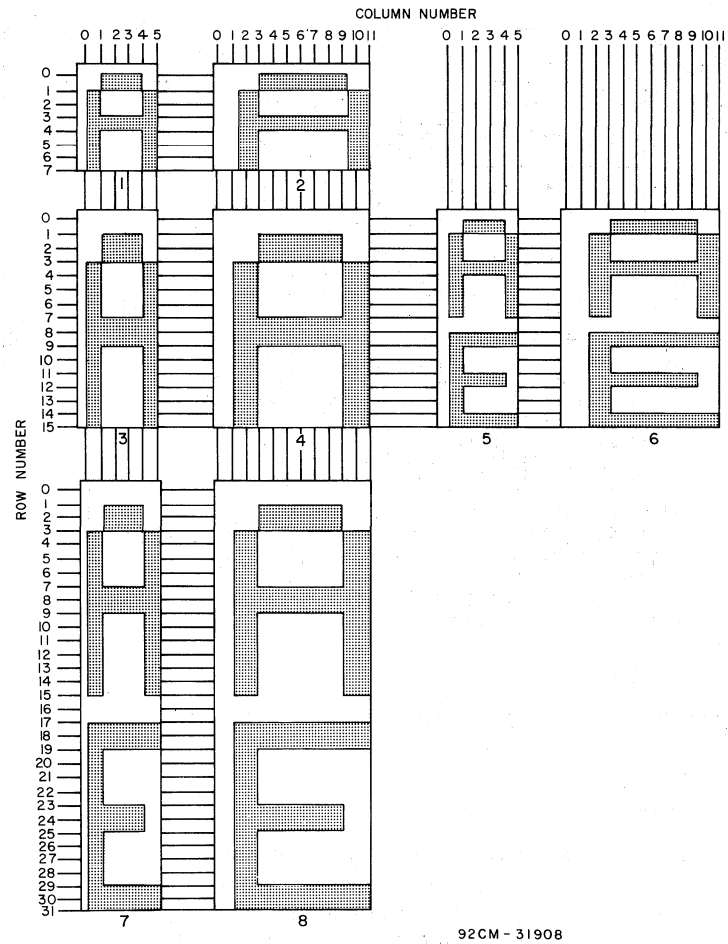


Fig. 4 - Character display matrix size.

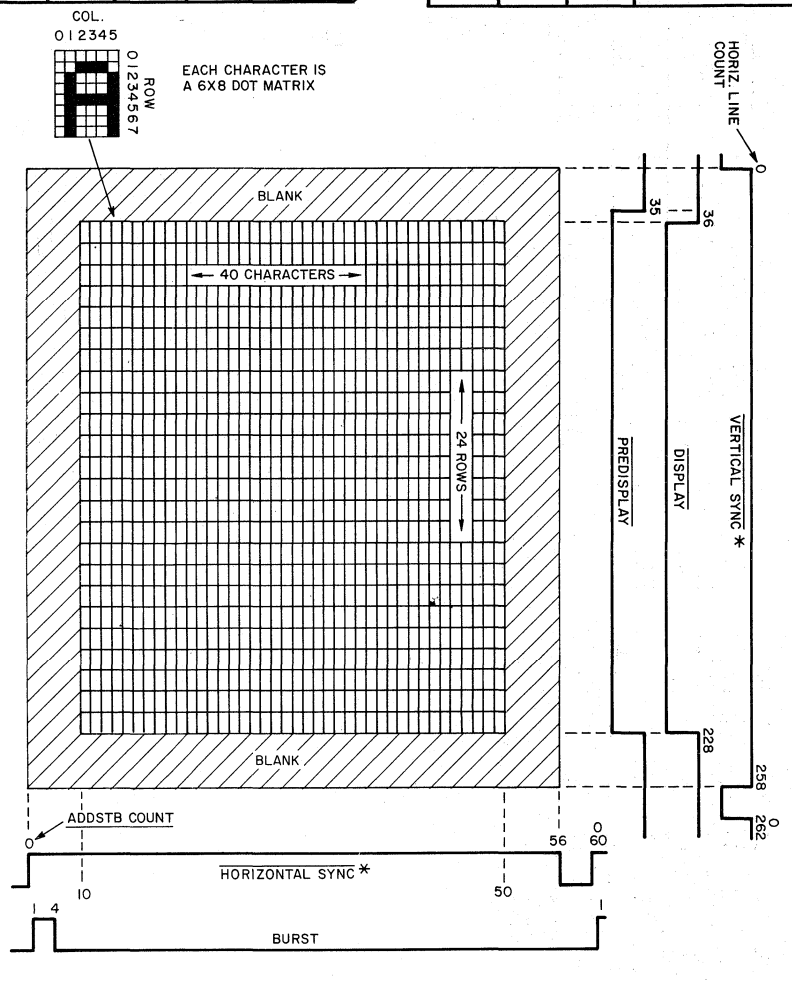
CDP1869C, CDP1870C Types

TABLE 1
TONE RANGE SELECT

TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	INPUT FREQUENCY (kHz)
0	0	0	5.5371094
0	0	1	11.074218
0	1	0	22.148437
0	1	1	44.296875
1	0	0	88.593750
1	0	1	177.18750
1	1	0	354.37500
1	1	1	708.75000

TABLE 2
WHITE NOISE RANGE SELECT

WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	TOP-OF-RANGE FREQUENCY (kHz)
0	0	0	.69213865
0	0	1	1.3842773
0	1	0	2.7685547
0	1	1	5.5371084
1	0	0	11.074218
1	0	1	22.148437
1	1	0	44.296875
1	1	1	88.598750



* HORIZONTAL AND VERTICAL SYNC ARE COMBINED TO FORM COMPSYNC

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Fig. 5 - 40 x 24 character display.

TABLE 3
CHARACTER COLOR CONTROL

COLB1	COLB0	RED	BLUE	GREEN
0	0	CCB0	CCB1	PCB
0	1	CCB0	PCB	CCB1
1	0	PCB	CCB0	CCB1
1	1	PCB	CCB0	CCB1

CDP1869C, CDP1870C Types

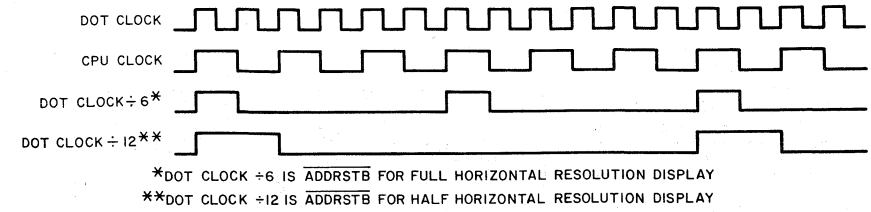

Fig. 6A - ADDSTB timing diagram.

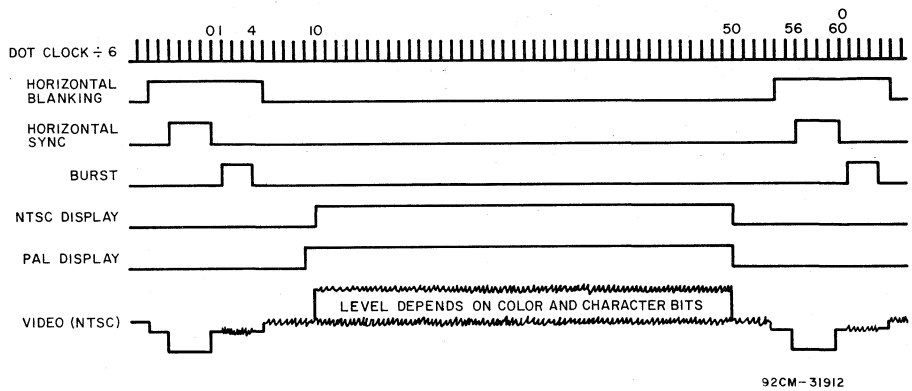

Fig. 6B - Horizontal timing diagram.

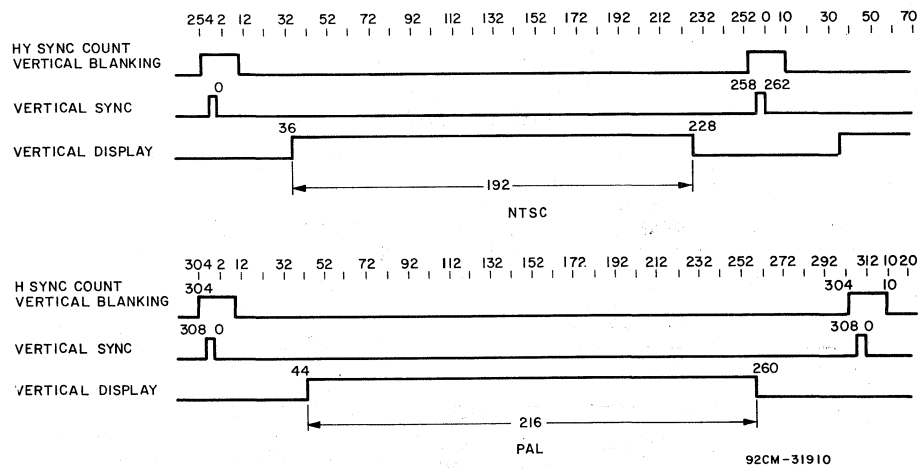

Fig. 6C - Vertical timing diagram.

TABLE 4
COLOR FORMAT CONTROL

CFC	BKG CHR	BKG LUM	DOT CHR	DOT LUM
0	BKG R,B,G	BKG R,B,G	CCB0/CCB1 PCB	CCB0/CCB1 PCB
1	BKG R,B,G	BKG R,B,G	BKG R,B,G	CCB0/CCB1 PCB

CDP1869C, CDP1870C Types

TABLE 5
COLOR SELECT

CHAR OR BKG COLOR DATA BITS			OUTPUT COLOR	% OF MAX LUMINANCE
RED	BLUE	GREEN		
0	0	0	BLACK	0
0	0	1	GREEN	59
0	1	0	BLUE	11
0	1	1	CYAN	70
1	0	0	RED	30
1	0	1	YELLOW	89
1	1	0	MAGENTA	41
1	1	1	WHITE	100

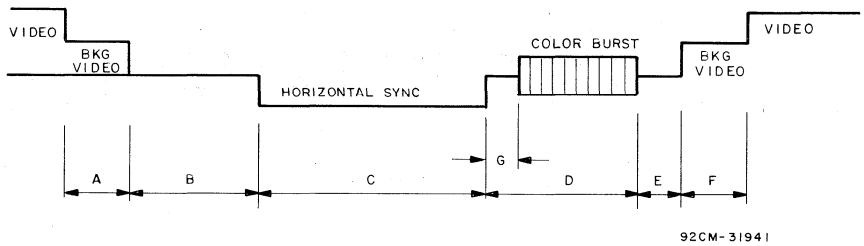

TABLE 7A
HORIZONTAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.67 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	3.7 μs	NA	4.8 μs
B	0.02H MIN 1.27 μs MIN	2.12 μs	1.55 μs	2.12 μs
C	0.07H-.08H 4.45-5.08 μs	4.23 μs	4.7 μs	4.27 μs
D	0.045H-0.55H 8-11 CYCLES 3.58 MHZ	3.174 μs 11 CYCLES 3.58 MHZ	11 CYCLES 4.433 MHZ	3.199 μs 14 CYCLES 4.433 MHZ
E	0.02H MIN 1.27 μs MIN	1.41 μs	2.07 μs	1.07 μs
F	NA	6 μs	NA	4.98 μs
G	0.006H 0.381 μs	0.352 μs	0.70 μs	.355 μs
HORIZONTAL FREQUENCY	15,734.264 HZ (COLOR) 15,750 HZ (B&W)	15,750 HZ	15,625 HZ	15,628 HZ

H = 63.5 μs NA = NOT APPLICABLE

CDP1869C, CDP1870C Types

TABLE 6
DISPLAY FORMAT COMBINATIONS (FULL COLOR SYSTEM)

CDP1870 FRES HORIZ	CDP1869 FRES VERT	CDP1869 DOUBLE PAGE	CDP1869 16-ROW HI-RES	CHAR DISPLAY MATRIX	CHAR/ LINE	CHAR LINES/ FRAME
0	0	0	0	6x8	20	12
0	0	0	1	6x16	20	6
0	0	1	0	6x8	20	12
0	0	1	1	—	—	—
0	1	0	0	6x8	20	24
0	1	0	1	6x16	20	12
0	1	1	0	6x8	20	24
0	1	1	1	—	—	—
1	0	0	0	6x8	40	12
1	0	0	1	6x16	40	6
1	0	1	0	6x8	40	12
1	0	1	1	—	—	—
1	1	0	0	6x8	40	24
1	1	0	1	6x16	40	12
1	1	1	0	6x8	40	24
1	1	1	1	—	—	—

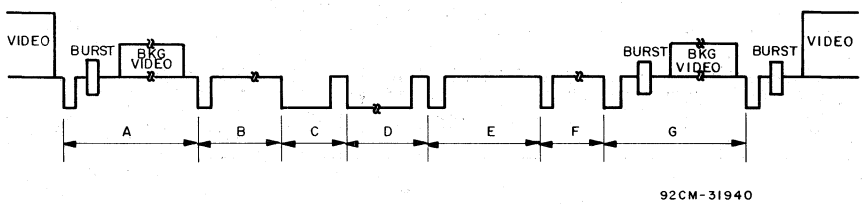

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TABLE 7B
VERTICAL TIMING STANDARDS

DIAGRAM	NTSC STANDARD	NTSC VIS 5.67 MHz XTAL	PAL STANDARD	PAL VIS 5.626 MHz XTAL
A	NA	26H	NA	44H
B*	3H	4H	2.5H	4H
C	1H	1H	1H	1H
D	2H	3H	1.5H	3H
E	1H	1H	1H	1H
F	2H	9H	19H	9H
G	9H-12H	26H	NA	34H
HORIZONTAL PERIOD (H)	63.5 μs	63.5 μs	64 ms	64 μs
VERTICAL FREQUENCY	59.94 HZ (COLOR) 60 HZ (B&W)	60.115 HZ	50 HZ	50.09 HZ

* = NO BKG VIDEO, NO BURST NA = NOT APPLICABLE

CDP1869C, CDP1870C Types

TABLE 6 (CONT'D)
DISPLAY FORMAT COMBINATIONS (FULL COLOR SYSTEM)

MAX. DISPLAY PAGE MEM. SIZE	MAX. DISPLAY CHAR. MEM. SIZE	CHAR SIZE #	COMMENTS
240x7	128x8x6	4	Repeats each row and col twice
240x7	128x16x6	8	Repeats each row and col twice, 16 different rows
1200x7	128x8x6	4	Repeats each row and col twice, hardware scroll
—	—	—	Invalid operation
960x7	128x8x6	2	Repeats each col twice
960x7	128x16x6	6	Repeats each col twice, 16 different rows
1920x7	128x8x6	2	Repeats each col twice, hardware scroll
—	—	—	Invalid operation
240x7	128x8x6	3	Repeats each row twice
240x7	128x16x6	7	Repeats each row twice, 16 different rows
1200x7	128x8x6	3	Repeats each row twice, hardware scroll
—	—	—	Invalid operation
960x7	128x8x6	1	Highest resolution
960x7	128x16x6	5	Highest resolution, 16 different rows
1920x7	128x8x6	1	Highest resolution, hardware scroll
—	—	—	Invalid operation

TABLE 8
CDP1870 COMMAND REGISTER CODE

CPU I/O INSTRUCTION	BUS 7	BUS 6	BUS 5	BUS 4	BUS 3	BUS 2	BUS 1	BUS 0
Out 63	FRES Horz	COLB1	COLB0	DISP OFF	CFC	BKG RED	BKG BLUE	BKG GREEN

TABLE 9
CDP1869 COMMAND REGISTER CODES

CPU I/O INSTRUCTION	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8
OUT 64	0*	TONE ÷ 2^6	TONE ÷ 2^5	TONE ÷ 2^4	TONE ÷ 2^3	TONE ÷ 2^2	TONE ÷ 2^1	TONE ÷ 2^0
OUT 65	WN OFF	WN FREQ SEL2	WN FREQ SEL1	WN FREQ SEL0	WN AMP 2^3	WN AMP 2^2	WN AMP 2^1	WN AMP 2^0
OUT 66	X	X	X	X	X	PMA10 REG	PMA9 REG	PMA8 REG
OUT 67	X	X	X	X	X	HMA10 REG	HMA9 REG	HMA8 REG

CPU I/O INSTRUCTION	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
OUT 64	TONE OFF	TONE FREQ SEL2	TONE FREQ SEL1	TONE FREQ SEL0	TONE AMP 2^3	TONE AMP 2^2	TONE AMP 2^1	TONE AMP 2^0
OUT 65	FRES VERT	DOUBLE PAGE	16-ROW HI-RES	X	NTSC	X	X	CMEN ACCESS MODE
OUT 66	PMA7 REG	PMA6 REG	PMA5 REG	PMA4 REG	PMA3 REG	PMA2 REG	PMA1 REG	PMA0 REG
OUT 67	HMA7 REG	HMA6 REG	HMA5 REG	HMA4 REG	HMA3 REG	HMA2 REG	X**	X**

X = DON'T CARE * = MUST BE LATCHED LOW ** = ALWAYS LATCHED LOW INTERNALLY

General-Purpose Memories

Technical Data

CD4036A, CD4039A Types

COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

ary Addressing CD4036AD, CD4036AK
Direct Word-Line CD4039AD, CD4039AK
Addressing

Special Features:

- *COS/MOS logic compatibility at all input and output terminals*
- *Memory bit expansion*
- *Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines*
- *Memory bypass capability for all bits*
- *Buffering on all outputs*
- *CD4036A—on-chip binary address decoding, separate READ INHIBIT and WRITE controls*
- *CD4039A—Direct word-line addressing*
- *Access Time—200 ns (typ.) at $V_{DD} = 10$ V*

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (see Fig. 19). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (see Fig. 4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

Applications:

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- *Channel Preset Memory in digital frequency-synthesizer circuits*
- *General-purpose and scratchpad memory in COS/MOS and other low-power systems.*

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-ORing multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig. 5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

CD4036A, CD4039A Types

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE ..... —65 to +150 °C
OPERATING-TEMPERATURE RANGE ..... −55 to +125 °C
DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$) ..... −0.5 to +15 V
DEVICE DISSIPATION (Per Package) ..... 200 mW
ALL INPUTS ..... $V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$) ..... 3 to 15 V
LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265 °C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK						UNITS
		V_O Volts	V_{DD} Volts	−55 °C		25 °C		125 °C		
				Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current, I_L			5	—	5	—	5	—	300	μA
			10	—	10	—	10	—	600	
Quiescent Device Dissipation/Package, P_D			5	—	25	—	25	—	1500	μW
			10	—	100	—	100	—	6000	
Output Voltage: Low-Level, V_{OL}			5	—	0.01	—	0.01	—	0.05	V
			10	—	0.01	—	0.01	—	0.05	
High-Level, V_{OH}			5	4.99	—	4.99	—	4.95	—	V
			10	9.99	—	9.99	—	9.95	—	
Threshold Voltage: N-Channel, V_{THN}	$I_D = 20\ \mu A$			1.7 typ.		1.5 typ.		1.3 typ.		V
P-Channel, V_{THP}	$I_D = -20\ \mu A$			−1.7 typ.		−1.5 typ.		−1.3 typ.		V
Noise Immunity, V_{NL} (All inputs except bit inputs when in memory bypass mode.) V_{NH}			5	1.5	—	1.5	—	1.4	—	V
			10	3	—	3	—	2.9	—	
			5	1.4	—	1.5	—	1.5	—	
			10	2.9	—	3	—	3	—	
Output Drive Current: N-Channel, I_{DN}	Normal Read Modes	0.5	5	0.12	—	0.10	—	0.07	—	mA
		0.5	10	0.30	—	0.25	—	0.17	—	
P-Channel, I_{DP}		4.5	5	−0.12	—	−0.10	—	−0.07	—	mA
		9.5	10	−0.30	—	−0.25	—	−0.17	—	
Output Drive Current: N-Channel, I_{DN}	Memory Bypass Mode +	0.5	5	0.04	—	0.03	—	0.02	—	mA
		0.5	10	0.09	—	0.075	—	0.05	—	
P-Channel, I_{DP}		4.5	5	−0.04	—	−0.03	—	−0.02	—	mA
		9.5	10	−0.09	—	−0.075	—	−0.05	—	
Input Current, I_I		—	—	—	—	10 typ.		—	—	pA

+ Bit inputs driven from low-impedance driver.

CD4036A, CD4039A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25\,°C$ and $C_L = 15$ pF
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTIC	TEST CONDITIONS		CD4036AD, CD4036AK CD4039AD, CD4039AK			UNITS
		V_{DD} Volts	Min.	Typ.	Max.	
Read Delay Time, t_{rd}: (Access time)	Output tied through 100 kΩ to V_{SS} for data output "high" and to V_{DD} for data output "low"	5	—	375	750	ns
Read Inhibit (RI)		10	—	150	300	Note 4
Chip Inhibit (CI)		5	—	500	1000	ns
		10	—	200	400	Note 4
Memory Bypass (MB)		5	—	375	750	ns
		10	—	150	300	
Address[1] (ADD)		5	—	500	1000	ns
		10	—	200	400	
Write Set-up Time[2], t_{WS}		5	250	125	—	μs
		10	100	50	—	
Write Removal Time[3], t_{WR}		5	0	0	—	ns
		10	0	0	—	
Write Pulse Duration, t_W		5	150	75	—	ns
		10	60	30	—	
Data Set-up Time[5], t_{DS}		5	—	0	0*	ns
		10	—	0	0*	
Data Overlap Time[6], t_{DO}		5	100•	50	—	ns
		10	40•	20	—	
Output Transition Time, t_{THL} / t_{TLH}		5	—	200	400	ns
		10	—	100	200	
Input Capacitance, C_I	Any Input		—	5	—	pF

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD and CD4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
   * Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.
6. The time that DATA signal must remain present after the WHITE pulse removal.
   • Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

HANDLING CONSIDERATIONS

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

OPERATING CONSIDERATIONS

1. Low impedance pulse generators or power supplies connected to the inputs of these devices must be disconnected before the dc power supply is turned off.
2. All unused input leads should be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved.

CD4036A, CD4039A Types

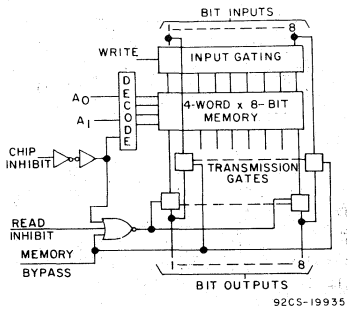


Fig. 1—CD4036A—logic block diagram.

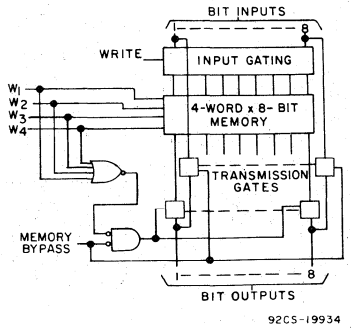


Fig. 2—CD4039A—logic block diagram.

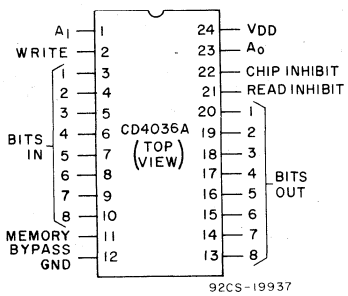
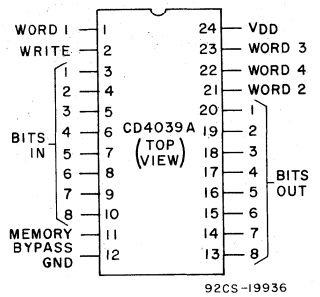


Fig. 3a)—CD4036AD and CD4036AK terminal assignments.



b)—CD4039AD and CD4039AK terminal assignments.

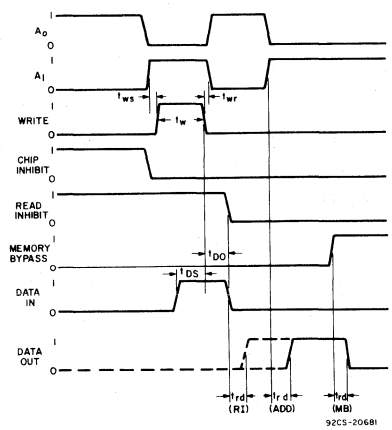


Fig. 4—CD4036A timing diagram.

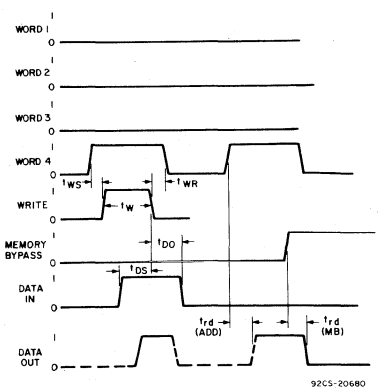


Fig. 5—CD4039A timing diagram.

CD4036A, CD4039A Types

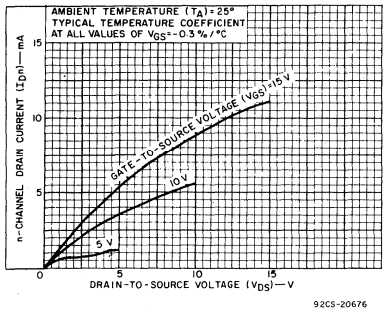


Fig. 6—Typical n-channel drain characteristics.

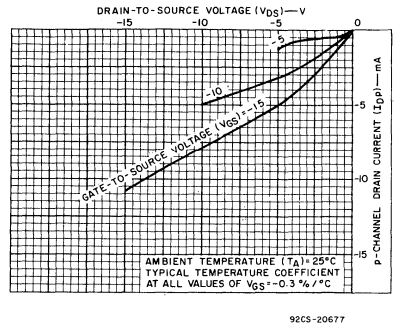


Fig. 7—Typical p-channel drain characteristics.

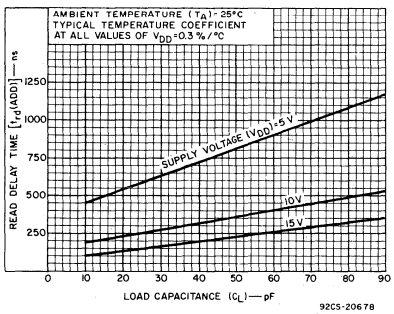


Fig. 8—Typical read delay time vs. C_L.

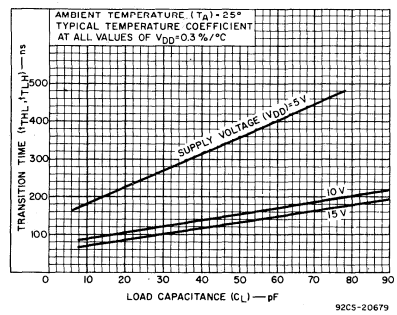


Fig. 9—Typical transition time vs. C_L.

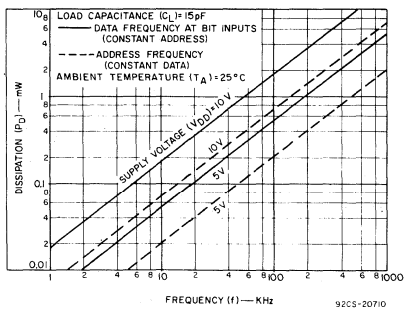


Fig. 10—Typical power dissipation vs. frequency.

CD4036A, CD4039A Types

TEST CIRCUITS

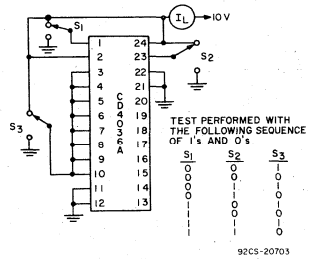


Fig. 11—Quiescent current (CD4036A).

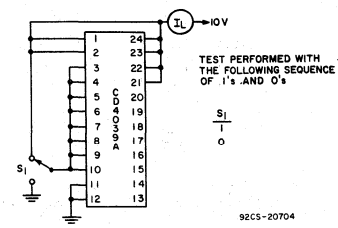


Fig. 12—Quiescent current (CD4039A).

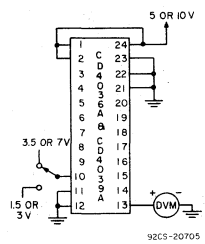


Fig. 13—Noise immunity.

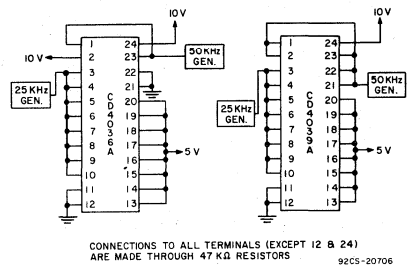


Fig. 14—Operating life.

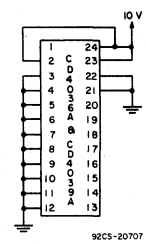


Fig. 15—Biased life.

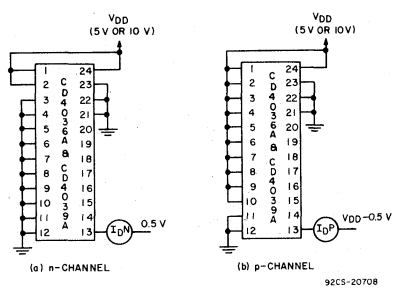


Fig. 16—Drive current.

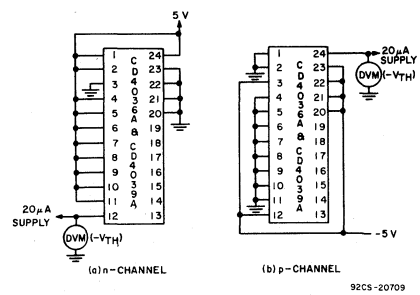


Fig. 17—Threshold voltage.

CD4036A, CD4039A Types

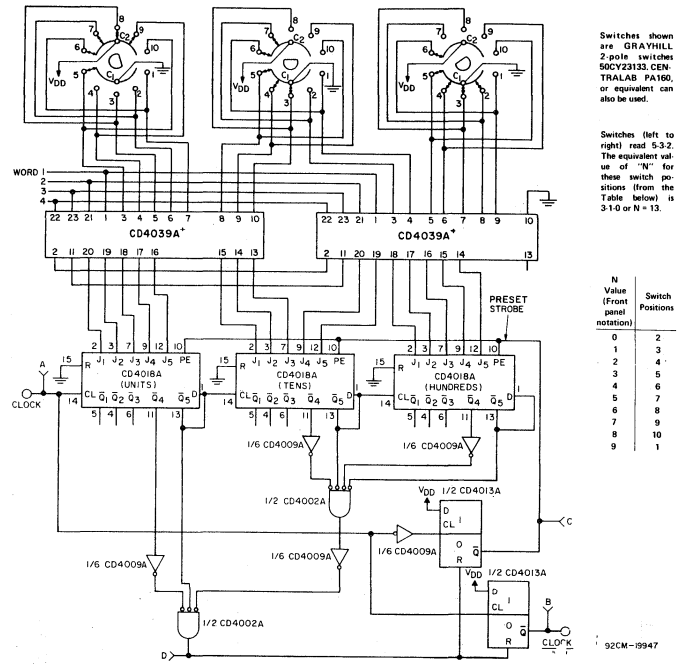


Fig. 18—Three-decade programmable ÷ N counter with 4-channel preset memory settings for frequency synthesizers.

The divide-by-N counter system shown in Fig. 18 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be read into each CD4018A by simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.

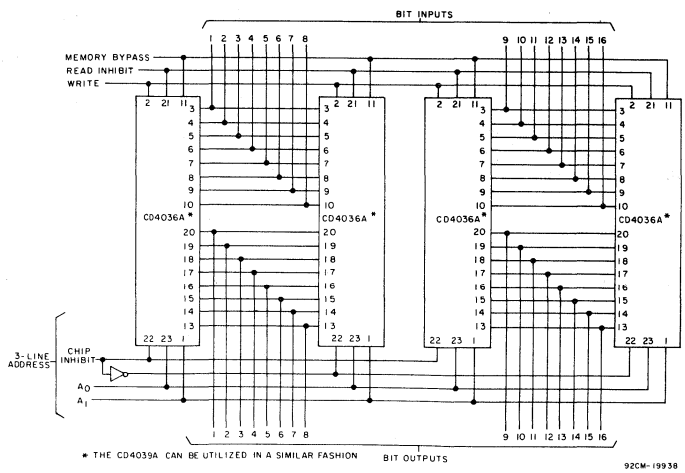


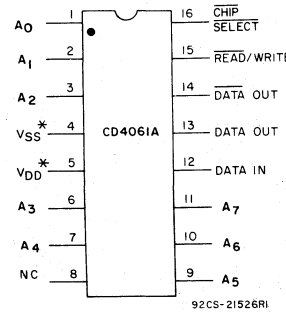
Fig. 19—General-purpose memory storage—8 words x 16 bits (RAM or ROM).

CD4061A Types

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

Features:

- **Low standby power: 10 nW/bit (typ.) @ V_{DD} = 10 V**
- **Access time: 380 ns (max.) @ V_{DD} = 10 V**
- **Single 3-to-15 V power supply**
- **COS/MOS input/output logic compatibility**
- **TTL output drive capability**
- **Three-state data outputs for bus-oriented systems**
- **1101-type pin designations***
- **Separate data output and data input lines**
- **Noise immunity: 45% of V_{DD} (typ.)**
- **Fully decoded addressing**
- **Single write/read control line**



The RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0-A_7) to select one of 256 storage locations. Additional connections are provided for a READ/WRITE command CHIP SELECT DATA IN, and DATA OUT and DATA OUT lines.

To perform READ and WRITE operations the CHIP-SELECT signal must be low. When the CHIP-SELECT signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-SELECT signal must be returned to a high level, regardless of the logic level of the READ/WRITE input. In a multiple package application, the CHIP-SELECT signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP SELECT and READ/WRITE signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE . . . . . –55 to +125°C

DC SUPPLY-VOLTAGE RANGE:
V_{DD}▲ . . . . . –0.5 to +15 V

DEVICE DISSIPATION (PER PACKAGE) . . . . . 200 mW

ALL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

RECOMMENDED DC SUPPLY VOLTAGE
(V_{DD}-V_{SS}) . . . . . 3 to 15 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

*The pin designations are compatible with other static 256-bit memories and are, therefore, not compatible with standard COS/MOS CD4000A-series devices; i.e., V_{DD} is pin 5 and V_{SS} is pin 4.

CD4061A Types

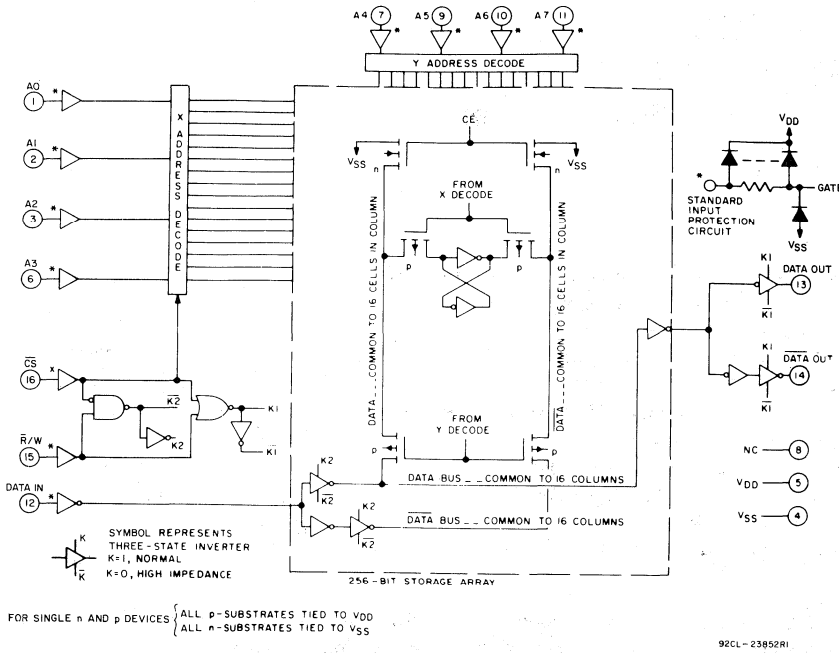


Fig. 1 – CD4061A logic diagram.

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	$\overline{\text{CHIP-SELECT}}$	$\overline{\text{READ/WRITE}}$	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read Modify Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

*For a READ MODIFY WRITE operation, $\overline{\text{CHIP SELECT}}$ may be held to logic 0 for the whole operation.

CD4061A Types

STATIC ELECTRICAL CHARACTERISTICS

(All inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . 3 to 15 V)

CHARACTERISTIC	TEST CONDITIONS		LIMITS							UNIT
			−55°C		25°C			125°C		
	V_O (V)	V_{DD} (V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current, I_L *See Fig. 14*		5	–	5	–	0.12	5	–	150	μA
		10	–	10	–	0.25	10	–	300	
Quiescent Device Dissipation/Package, P_D		5	–	–	–	0.6	25	–	750	μW
		10	–	–	–	2.5	100	–	3000	
Output Voltage Low-Level, V_{OL}		5	–	0.01	–	0	0.01	–	0.05	V
		10	–	0.01	–	0	0.01	–	0.05	
High-Level, V_{OH}		5	4.99	–	4.99	5	–	4.95	–	
		10	9.99	–	9.99	10	–	9.95	–	
Noise Immunity, (All Inputs) *See Fig. 17* V_{NL}	0.8	5	1.5	–	1.5	2.25	–	1.4	–	V
	1	10	3	–	3	4.5	–	2.9	–	
V_{NH}	4.2	5	1.4	–	1.5	2.25	–	1.5	–	
	9	10	2.9	–	3	4.5	–	3	–	
Output Drive Current: (Data Out, Data Out) N-Channel (Sink), I_DN *See Figs. 3, 4, 12*	0.4	4.5	2	–	1.6	2.5	–	1.1	–	mA
	0.5	10	4.3	–	3.5	5	–	2.4	–	
P-Channel (Source), I_DP *See Figs. 5, 6, 13*	2.5	5	−1.1	–	−0.9	−1.8	–	−0.65	–	
	4.6	5	−0.5	–	−0.4	−0.8	–	−0.3	–	
	9.5	10	−1.1	–	−0.9	−1.8	–	−0.65	–	
Output Off Resistance (High-Impedance State), R_o (Off)		5	10	–	10	–	–	10	–	MΩ
		10	10	–	10	–	–	10	–	

CD4061A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$, $V_{SS} = 0$ V, $C_L = 50$ pF, and t_r, $t_f = 20$ ns

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	MIN.*	TYP.	MAX.*	
READ CYCLE TIME						
Read Cycle	t_{RC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	ns
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	ns
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	ns
		10	200	–	–	
Read Access	t_{RA}	5	–	450	750	ns
		10	–	250	380	
Data Out Hold	t_{DOH}	5	110	170	230	ns
		10	130	160	190	
Data Out Active	t_{DOA}	5	80	120	160	ns
		10	40	70	100	
Output Transition	t_{TLH}	5	–	60	100	ns
		10	–	50	75	
	t_{THL}	5	–	35	60	
		10	–	25	40	
Chip-Select Input Rise and Fall Time,	t_{rCE}	5	–	–	15	μs
	t_{fCE}	10	–	–	5	
		15	–	–	1	
WRITE CYCLE TIME						
Write Cycle	t_{WC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	
		10	200	–	–	
Write Hold	t_{WRH}	5	150	100	–	
		10	100	70	–	
Write	t_{WRW}	5	150	100	–	
		10	100	70	–	
Data-In Setup	t_{DIS}	5	140	80	–	
		10	80	35	–	
Data-In Hold	t_{DIH}	5	25	10	–	
		10	20	10	–	

* See Symbols Definitions.

CD4061A Types

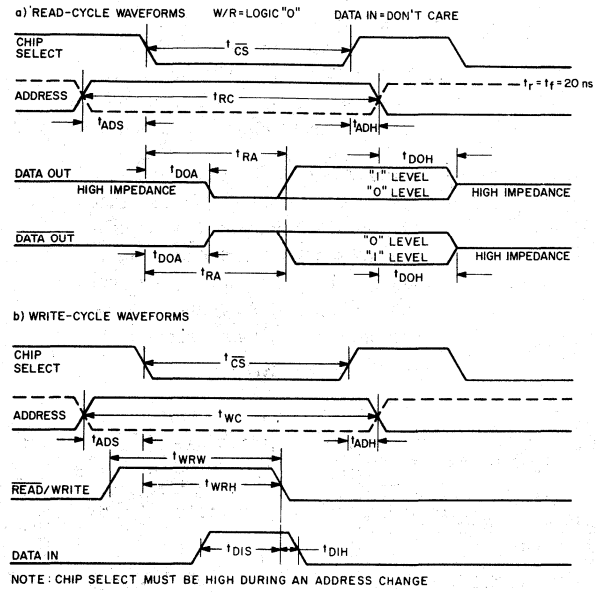


Fig. 2 – Typical write-read waveforms.

SYMBOL DEFINITIONS

t_{RC} – Read Cycle Time – Time required between address changes during a read cycle. Minimum read cycle time is equal to t_{ADS}(min) + $t_{\overline{CS}}$ (min) + t_{ADH}(min).

t_{ADS} – Address Setup Time – Time required before the Chip-Select voltage level can be lowered after the slowest address transition.

t_{ADH} – Address Hold Time – Time required before the earliest address transition can take place after Chip-Select voltage level has been increased. t_{ADH}(min) + t_{ADS}(min) is the minimum time required to discharge internal nodes and allow setting of address decoders during an address transition. Chip-Select level must be high during each address change, even if only read or write cycles are successively performed. However, if address is not changed, the Chip-Select may remain in its active (low) state during successive read and write cycles.

$t_{\overline{CS}}$ – Chip Select Time – Time required for the Chip Select to be active for a valid memory cycle.

t_{RA} – Read Access Time – Measured from Chip Select negative going transition to the valid output data.

t_{DOA} – Data-Out Active – Time required before the high-impedance state of Data Output is changed to a low-voltage state and Data output is changed to a high-voltage state. (If the read out data from a selected storage location is logic "1", then Data Output will rise and Data Output will fall. If the read out data is logic "0", both Data Output and Data Output will maintain their original states.

t_{DOH} – Data-Out Hold – Time required for the Data Output and Data Output to change from an active to a high-impedance state.

t_{WC} – Write Cycle Time – Time required between address changes during a write cycle. This time sets the maximum operating speed for the memory, with a minimum cycle time equal to t_{ADS}(min) + $t_{\overline{CS}}$ (min) + t_{ADH}(min).

t_{WRH} – Write Hold Time – Time required before the negative transition of R/W pulse with respect to the negative transition of the Chip-Select signal.

t_{DIS} – Data-In Setup Time – Time required for the data input to be valid before the negative transition of the R/W pulse.

CD4061A Types

t_{DIH} – Data-In Hold Time – Time required for the data input to be valid after R/W pulse is returned to a low level. The minimum data-in width is equal to $t_{DIS}(min) + t_{DIH}(min)$.

t_{WRW} – Write Width – Time required for the R/W pulse to be high. Note that the positive transition of this signal can be made after the Chip-Select signal is high. In addition, the high state of the R/W signal shall be within the Chip-Select active state by at least a t_{WRH} period.

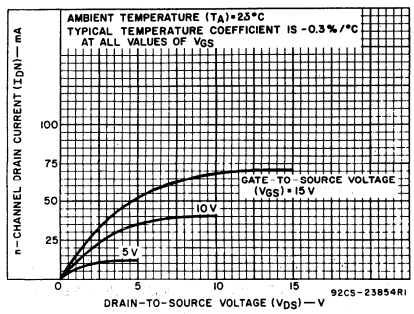


Fig. 3 – Typical n-channel drain characteristics.

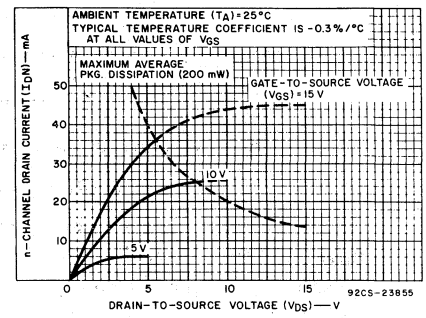


Fig. 4 – Minimum n-channel drain characteristics.

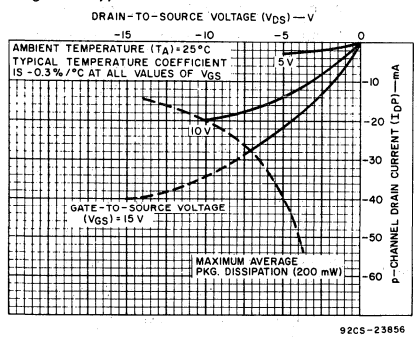


Fig. 5 – Typical p-channel drain characteristics.

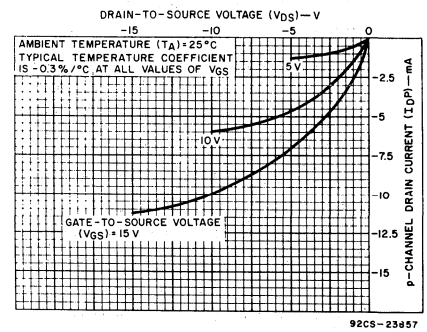


Fig. 6 – Minimum p-channel drain characteristics.

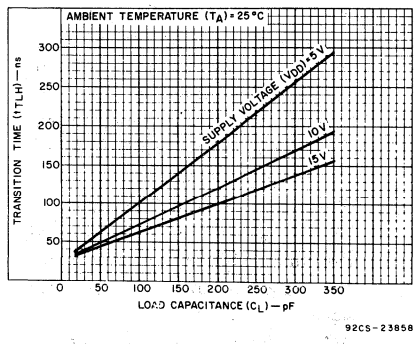


Fig. 7 – Typical low-to-high transition time (t_{TLH}) vs. C_L.

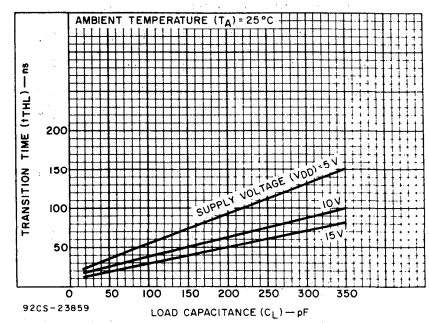


Fig. 8 – Typical high-to-low transition time (t_{THL}) vs. C_L.

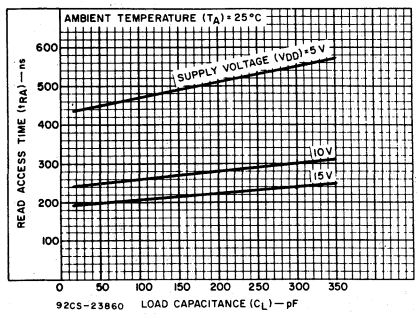


Fig. 9 – Typical read access time (t_{RA}) vs. C_L.

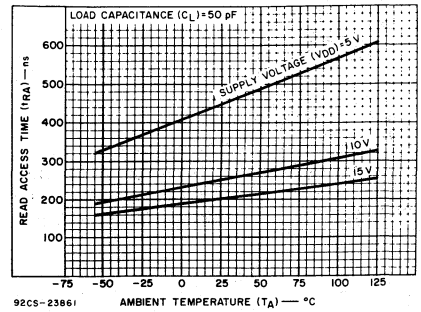


Fig. 10 – Typical read access time (t_{RA}) vs. temperature.

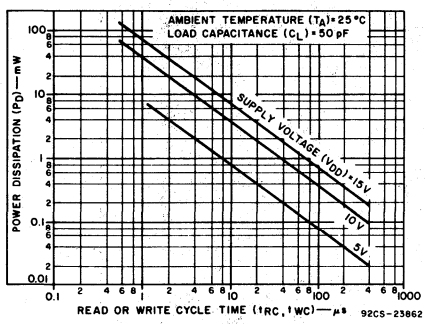
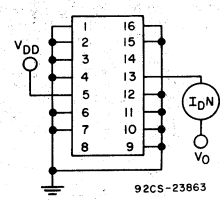


Fig. 11 – Typical power dissipation vs. cycle time.



Note: At address "0", "0" stored in memory.

Fig. 12 – N-channel drive current.

Note for Fig. 12 and Fig. 13:
Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of t_{CE} = 400 ns.

Note: At address 0, "1" stored in memory.

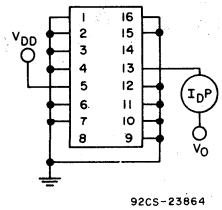


Fig. 13 – P-channel drive current.

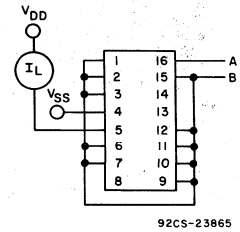


Fig. 14 – Quiescent device current.

Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

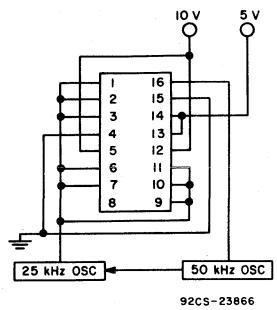
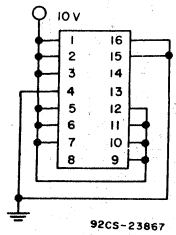


Fig. 15 – Operating life.

Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.

CD4061A Types



Description of Test:

Functional test run with random data input. All inputs toggle between 30% and 70% of V_{DD}.

Fig. 16 – Bias life.

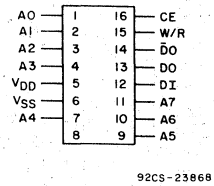
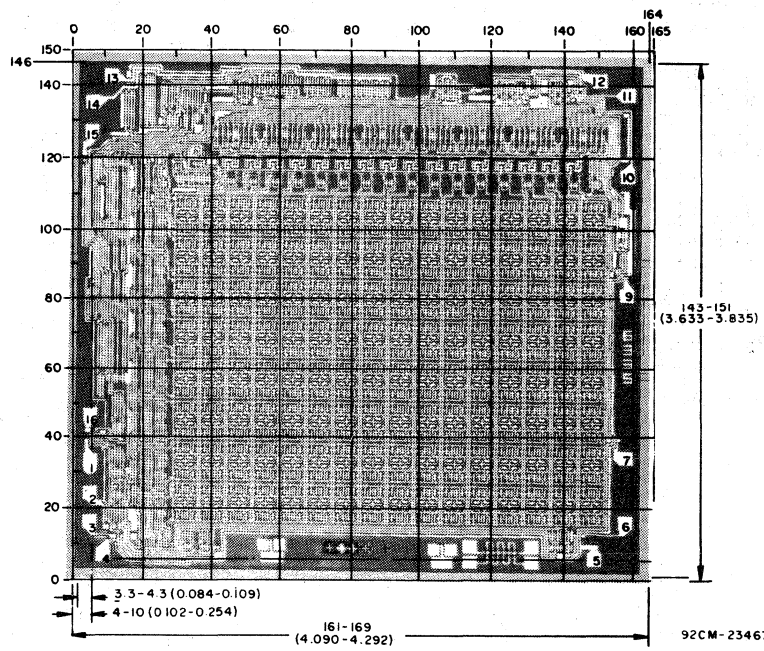


Fig. 17 – Noise immunity.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).

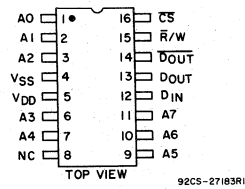
Dimensions and pad layout for CD4061A.

CD40061, CD40061A Types
Preliminary Data

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

Features:

- Organization — 256-words by 1-bit
- COS/MOS compatible inputs and outputs
- Low power dissipation (typ.) @ 700 nS cycle time:
  10 nW/Bit standby @ V_{DD} = 5 V
  0.1 mW/Bit operating @ V_{DD} = 5 V
  40 nW/Bit standby @ V_{DD} = 10 V
  0.4 mW/Bit operating @ V_{DD} = 10 V
- Access time (typ.):
  265 nS @ V_{DD} = 10 V; 700 nS @ V_{DD} = 5 V
- Noise immunity (typ.): 30% of V_{DD}
- TTL output drive capability
- 3-State complementary data outputs
- Separate data-in and data-out lines



TERMINAL ASSIGNMENT

The RCA-CD40061 and CD40061A are 256-word by 1-bit COS/MOS fully static random access memories. They are similar in terminal arrangement and function to the CD4061A, except that the requirement for the Chip-Select input to return to a high level between address changes in eliminated.

The CD40061AD and CD40061AE have maximum supply voltage ratings of 12 V; the CD40061E maximum rating is 7 V. These devices are fully decoded and utilize eight Address inputs (A_0-A_7) to select one of the 256 storage locations. Additional connections are provided for an active Low Chip-Select ($\overline{CS}$), a Read/Write command ($\overline{R}/W$), a Data input (DATA IN), an active High 3-State Output (DATA OUT), and an active Low 3-State Output ($\overline{DATA}$ OUT). DATA OUT is the same voltage state as DATA IN.

The Chip-Select input must be low to enable the Read or Write operations. A high level both inhibits these functions and causes the outputs to exhibit a high impedance. Output voltage levels appear at the output only when both $\overline{CS}$ and $\overline{R}/W$ inputs are at low levels. These outputs interface directly with TTL devices.

Both the CD40061E and CD40061AE are supplied in 16-lead dual-in-line plastic packages. The CD40061A is supplied in a hermetically sealed 16-lead dual-in-line ceramic side-brazed package. The CD40061 is also supplied in chip form (H suffix).

CD40061 and CD40061A OPERATIONAL MODES

MODE	$\overline{CHIP\text{-}SELECT}$	$\overline{READ/WRITE}$	DATA OUT	$\overline{DATA\ OUT}$
Write	0	1	High Impedance	High Impedance
Read	0	0	Storage State	Complement of Storage State
Unselected	1	X	High Impedance	High Impedance

1 = High Level 0 = Low Level X = Don't Care

CD40061, CD40061A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE RANGE ($V_{DD} - V_{SS}$):
- CD40061E . . . . . −0.5 to 7 V
- CD40061AD, CD40061AE . . . . . −0.5 to 12 V

RECOMMENDED DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$):
- CD40061E . . . . . 3 to 6 V
- CD40061AD, CD40061AE . . . . . 3 to 11 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT ANY ONE INPUT . . . . . ±10 mA
RECOMMENDED INPUT VOLTAGE SWING . . . . . V_{DD} to V_{SS}
DEVICE DISSIPATION (per package) . . . . . 200 mW
OPERATING-TEMPERATURE RANGE:
- CERAMIC-PACKAGE TYPE (CD40061AD) . . . . . −55 to +125°C
- PLASTIC-PACKAGE TYPES (CD40061E, CD40061AE) . . . . . −40 to +85°C

STORAGE-TEMPERATURE RANGE . . . . . −65 to +150°C
LEAD TEMPERATURE (During soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265°C

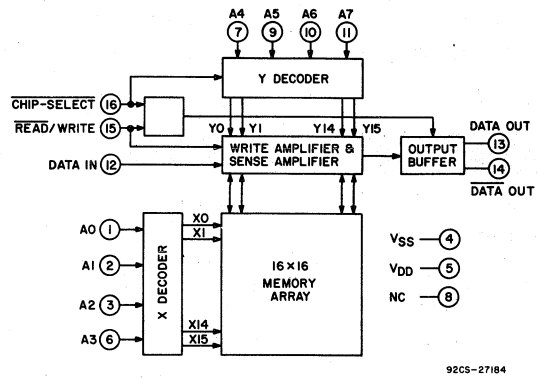


Fig. 1 – Functional block diagram for CD40061 and CD40061A.

STATIC ELECTRICAL CHARACTERISTICS

Values shown for V_{DD} = 5 V apply to all types, values shown for V_{DD} = 10 V apply to the CD40061AD and CD40061AE only.

CHARACTERISTIC	TEST CONDITIONS		LIMITS Full Temp. Range		TYPICAL VALUES	UNITS
	V_O(V)	V_{DD}(V)	Min.	Max.	at 25°C	
Quiescent Device Current, I_{DD}		5 10	– –	10 20	0.5 1	μA
Output Voltage, Low Level, V_{OL}		5 10	– –	0.05 0.05	0 0	V
Output Voltage, High Level, V_{OH}		5 10	4.95 9.95	– –	5 10	V
Output Current, Low Level, I_{OL}	0.4 0.5	5 10	0.85 2.1	– –	1.1 2.8	mA
Output Current, High Level, I_{OH}	4.5 9	5 10	–0.3 –0.6	– –	–0.4 –0.9	mA
Noise Immunity, All Inputs Low, V_{NL}	0.8 1	5 10	1 2	– –	1.5 3	V
Noise Immunity, All Inputs High, V_{NH}	4.2 9	5 10	1 2	– –	1.5 3	V
Output Resistance, Off State, R_O(off)		5 10	5 5	– –	10 10	MΩ

CD40061, CD40061A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at V_{DD} ± 5%, Input t_r, t_f = 20 ns, and C_l = 50 pF, see Note 2.

Values shown for V_{DD} = 5 V apply to all types; values shown for V_{DD} = 10 V apply to the CD40061AD and CD40061AE only.

READ CYCLE TIMES (For waveforms, see Figs. 2, 3, and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD}(V)	LIMITS● Full Temp. Range Min.	LIMITS● Full Temp. Range Max.	TYPICAL VALUES at 25°C	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5	880	–	720	ns
		10	380	–	290	
Address Setup, (Note 2)	t_{ADS}	5	40	–	20	ns
		10	20	–	10	
Address Hold,	t_{ADH}	5	0	–	–5	ns
		10	0	–	–5	
Read Setup,	t_{RDS}	5	0	–	–5	ns
		10	0	–	–5	
Read Hold,	t_{RDH}	5	0	–	–5	ns
		10	0	–	–5	
Data Out Hold,	t_{DOH}	5	–	65	40	ns
		10	–	40	20	
Data Out Active,	t_{DOA}	5	–	50	35	ns
		10	–	35	25	
Read Cycle, (Note 3)	t_{RC}	5	880	–	720	ns
		10	380	–	290	
Access,	t_{ACC}	5	–	850	700	ns
		10	–	345	265	

WRITE CYCLE TIMES (For waveforms, see Figs. 2,3, and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD}(V)	LIMITS● Full Temp. Range Min.	LIMITS● Full Temp. Range Max.	TYPICAL VALUES at 25°C	UNITS
Chip-Select,	$t_{\overline{CS}}$	5	420	–	350	ns
		10	200	–	150	
Address Setup, (Note 2)	t_{ADS}	5	40	–	20	ns
		10	20	–	10	
Address Hold,	t_{ADH}	5	0	–	–5	ns
		10	0	–	–5	
Write Setup,	t_{WRS}	5	330	–	270	ns
		10	190	–	140	
Write Width,	t_{WRW}	5	330	–	270	ns
		10	190	–	140	
Data In Setup,	t_{DIS}	5	0	–	–5	ns
		10	0	–	–5	
Data In Hold,	t_{DIH}	5	40	–	20	ns
		10	20	–	10	
Write Cycle, (Note 3)	t_{WC}	5	480	–	400	ns
		10	240	–	180	

For footnotes, see page 4.

CD40061, CD40061A Types

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

READ/MODIFY/WRITE TIMES (For waveforms, see Figs. 2, 3, and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD}(V)	LIMITS● Full Temp. Range Min.	Max.	TYPICAL VALUES at 25°C	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5	1190	–	980	ns
		10	545	–	410	
Address Setup, (Note 2)	t_{ADS}	5	40	–	20	ns
		10	20	–	10	
Address Hold,	t_{ADH}	5	0	–	–5	ns
		10	0	–	–5	
Read Setup,	t_{RDS}	5	0	–	–5	ns
		10	0	–	–5	
Data Out Active,	t_{DOA}	5	–	50	35	ns
		10	–	35	25	
Previous Data Hold,	t_{PDH}	5	–	65	50	ns
		10	–	40	25	
Access,	t_{ACC}	5	–	850	700	ns
		10	–	345	265	
Read Width Effective,	t_{RDW}	5	860	–	710	ns
		10	355	–	270	
Write Setup,	t_{WRS}	5	330	–	270	ns
		10	190	–	140	
Write Width,	t_{WRW}	5	330	–	270	ns
		10	190	–	140	
Data In Setup,	t_{DIS}	5	0	–	–5	ns
		10	0	–	–5	
Data In Hold,	t_{DIH}	5	40	–	20	ns
		10	20	–	10	
Read/Modify/Write Cycle, (Note 3)	t_{RWC}	5	1230	–	1000	ns
		10	570	–	430	

● The maximum and minimum limit values of the dynamic characteristics under worst operating conditions are based on the time durations expressed in Figs. 2, 3, and 4. The minimum limit indicates the shortest time generated at the output or required at the input. The maximum limit indicates the longest time generated at the output or required at the input. The typical values are for 25°C and nominal voltage. Timing measurements for the transition period are taken at either the 0.8 V_{DD} or 0.2 V_{DD} point.

Note 1 – The chip-select times specified provide an active output data time of 50 ns minimum.

Note 2 – Address rise and fall times must be equal to or less than 1 μs under all conditions and for all modes.

Note 3 – Cycle time defines the shortest time in which this memory will correctly perform its desired function.

CAPACITANCES (V_I = 0, f = 1 MHz)

CHARACTERISTICS	Min.	Typ.	Max.	UNITS
Address Input, C_A	–	9	–	pF
Chip-Select, C_{CS}	–	9	–	pF
Read/Write Input, C_{WE}	–	5	–	pF
Data Input, C_{DI}	–	5	–	pF
Data Output, C_{DO}	–	10	–	pF

CD40061, CD40061A Types

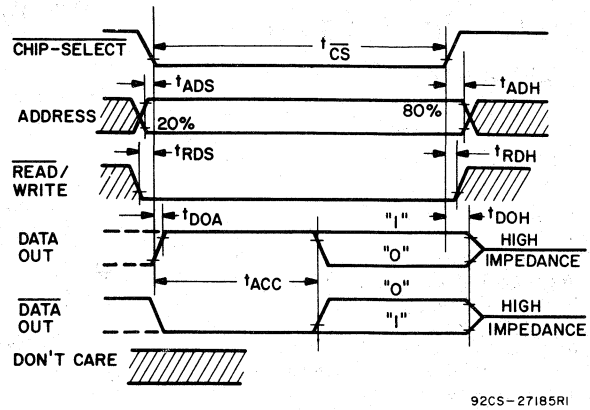


Fig.2 – Read cycle waveforms for CD40061, CD40061A.

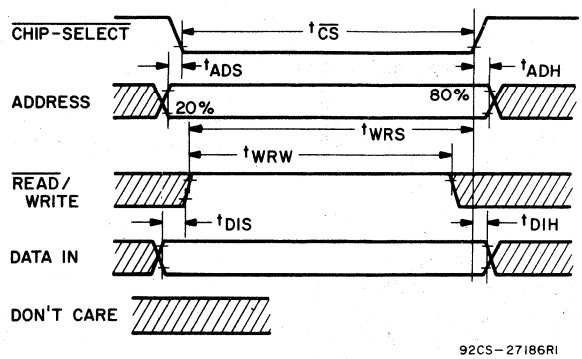


Fig.3 – Write cycle waveforms for CD40061, CD40061A.

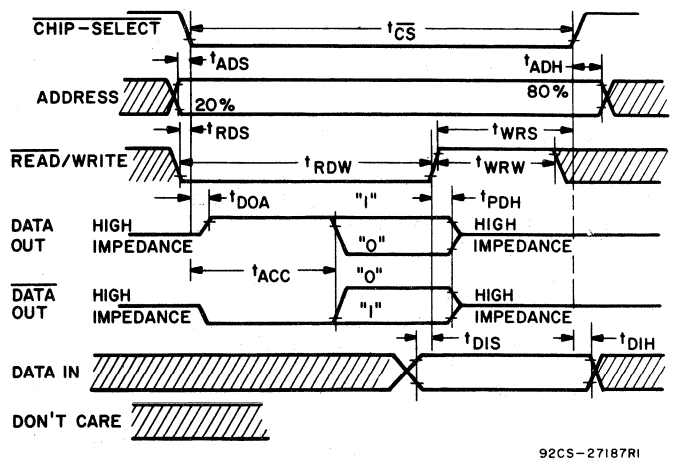


Fig.4 – Read/modify/write cycle waveforms for CD40061, CD40061A.

CD40114B Types

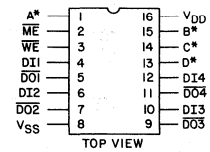
COS/MOS 64-Bit Random Access Memory

Preliminary Data

High-Voltage Types (20-Volt Rating)

Features:

- **Input address latch**
- **3-state outputs**
- **Low-power TTL compatible**
- **Equivalent to and pin-compatible with National 74C89**
- **Pin -compatible with 74S189**
- **Buffered inputs and outputs**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for description of "B" Series CMOS Devices"**



Terminal Assignment

The RCA-CD40114B is a 16-word x 4-bit random access memory (RAM) with four address inputs, four data inputs, a WRITE ENABLE (WE) input, a MEMORY ENABLE ($\overline{ME}$) input, and four 3-state data outputs. The four address inputs are decoded internally to select one of the 16 possible word locations. The address information is latched on the negative edge of the $\overline{ME}$ input by an internal address register. The selected output assumes a high-impedance condition when the device is writing or disabled. The $\overline{ME}$ input and the 3-state outputs allow memory expansion.

Applications:

- **Main frame memories**
- **Memory storage**
- **Scratch-pad memories**
- **Games**

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	3-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	3-STATE
H	H	Inhibit, Storage	3-STATE

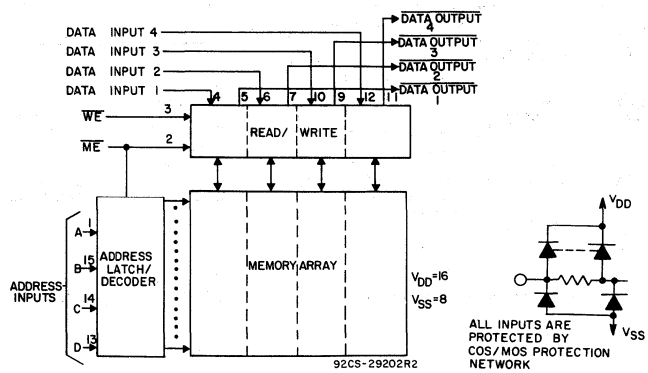


Fig. 1 — Functional Block Diagram

CD40114B Types

Address Operation

The high-to-low transition of $\overline{ME}$ enables the memory. Address inputs must be stable (either high or low) prior to and during this transition, but it is not necessary to hold them stable beyond it.

Write Operation

When $\overline{WE}$ and $\overline{ME}$ are low, information present at the data inputs is written into the memory at the selected address.

Read Operation

When $\overline{ME}$ is low and $\overline{WE}$ is high the complement of the memory contents at the selected address location are non-destructively read out at the four data outputs.

The CD40114B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead plastic packages (E suffix), and in chip form (H suffix).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

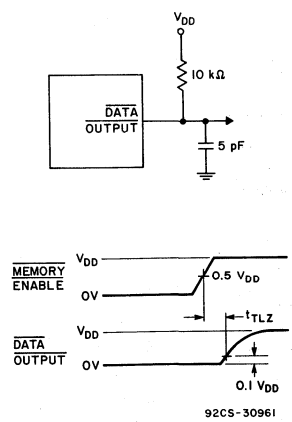


Fig. 2 — Output low to high-impedance transition time test circuit and waveforms.

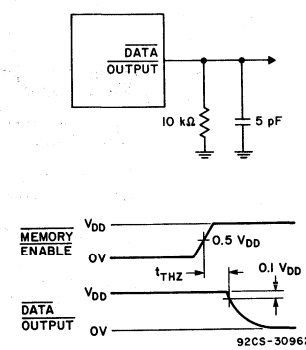


Fig. 3 — Output high to high-impedance transition time test circuit and waveforms.

CD40114B Types

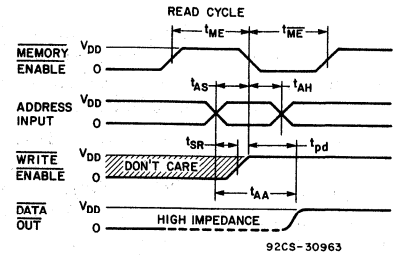


Fig. 4 – Read cycle waveforms.

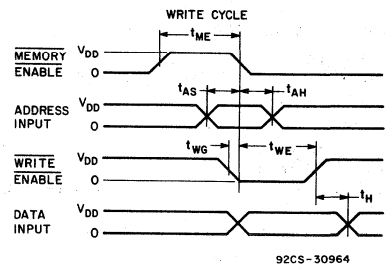


Fig. 5 – Write cycle waveforms

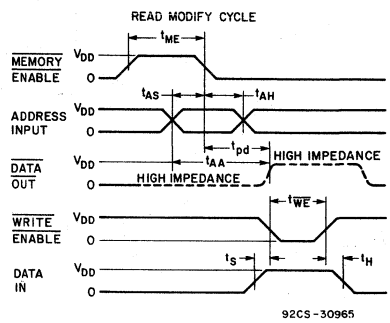


Fig. 6 – Read-modify-write cycle waveforms.

CD40114B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

CD40114B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r, t_f = 20 ns

Unless Otherwise Specified

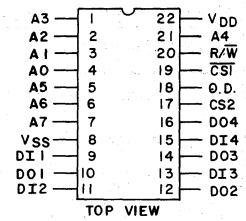
CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Access Time From Address Change, t_{AA}		5	325	650	ns
		10	140	280	
		15	120	240	
Min. Address Setup Time, t_{AS}		5	75	150	ns
		10	30	60	
		15	25	50	
Min. Address Hold Time, t_{AH}		5	30	60	ns
		10	20	40	
		15	15	30	
Min. $\overline{\text{Memory Enable}}$ Pulse Width, $t_{\overline{ME}}$, t_{ME}		5	200	400	ns
		10	75	150	
		15	60	120	
Min. $\overline{\text{Write Enable}}$ Setup Time For a Read, t_{SR}		5	–	0	ns
		10	–	0	
		15	–	0	
Min. $\overline{\text{Write Enable}}$ Setup Time for a Write, t_{WS}		5	–	t_{ME}	ns
		10	–	t_{ME}	
		15	–	t_{ME}	
Min. $\overline{\text{Write Enable}}$ Pulse Width, $t_{\overline{WE}}$		5	150	300	ns
		10	50	100	
		15	40	80	
Min. Data Input Hold Time, t_H		5	25	50	ns
		10	12	25	
		15	10	20	
Min. Data Input Setup Time, t_S		5	25	50	ns
		10	12	25	
		15	10	20	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from $\overline{\text{Memory Enable}}$	R_L = 10 kΩ, C_L = 5 pF	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time from Output-high or Output-low to High-Impedance State from $\overline{\text{Write Enable}}$	R_L = 10 kΩ, C_L = 5 pF	5	150	300	ns
		10	60	120	
		15	50	100	
Propagation Delay Time From $\overline{\text{Memory Enable}}$, t_{pd}		5	250	500	ns
		10	100	200	
		15	80	160	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Output Capacitance, C_{OUT}	Any Output		6.5	13	pF

MWS5101 Types

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- Industry standard pinout
- Very low operating current – 4 mA typ. at V_{DD} = 5 V and cycle time = 1 μs
- Two Chip-Select inputs – simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- Single-power-supply operation – 4 to 6.5 V
- High noise immunity–30% of V_{DD} over the range 5 to 6.5 V
- TTL compatible
  - Drives one TTL load
  - Accepts TTL level inputs using pull-up resistor
- Output-Disable for common I/O systems
- 3-State data output for bus-oriented systems
- Separate data inputs and outputs



TERMINAL ASSIGNMENT

The RCA-MWS5101 is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAM's to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, RCA-CDP1822, may be used.

The MWS5101 types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

RCA Type No.		Max. Access Time – ns	Max. Quiescent Current – μA
MWS5101DL1	V_{DD} = 5 V, T_A = 0-70°C	250	10
MWS5101EL1		250	10
MWS5101DL2		250	50
MWS5101EL2		250	50
MWS5101DL3		350	200
MWS5101EL3		350	200
MWS5101DL8		450	500
MWS5101EL8		450	500

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage values referenced to V_{SS} terminal) ..... –0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... –0.5 to V_{DD} +0.5 V
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) ..... –55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) ..... –40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... –65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

MWS5101 Types

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES		UNITS
	Min.	Max.	
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

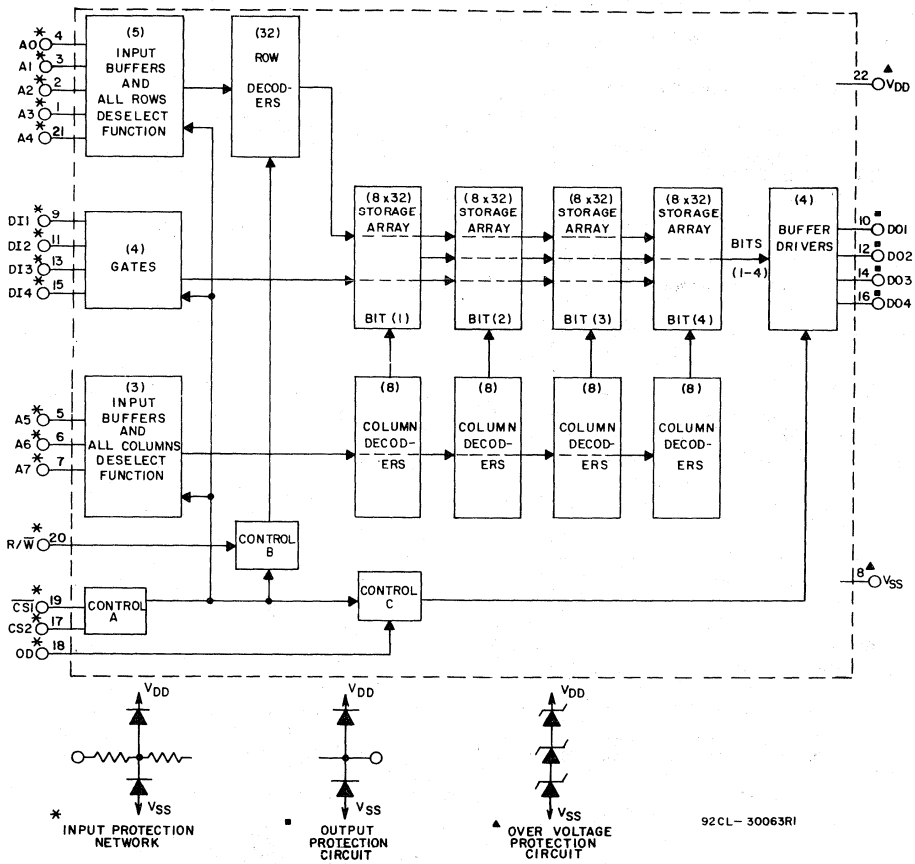


Fig. 1 – Functional block diagram for MWS5101.

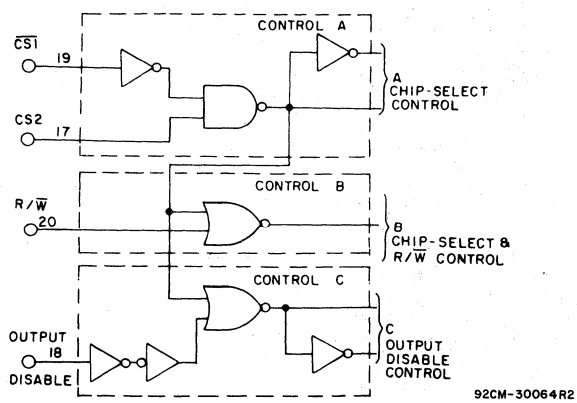


Fig. 2 – Logic diagram of controls for MWS5101.

MWS5101 Types

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{Chip Select 1}}$ $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	Read/$\overline{\text{Write}}$ R/$\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF and 1 TTL Load; See Figs. 4 and 5.

CHARACTERISTIC		LIMITS MWS5101D, MWS5101E									UNITS
		L1 Types L2 Types			L3 Types			L8 Types			
		Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Read Cycle Times											
Read Cycle	t_{RC}	250	–	–	350	–	–	450	–	–	ns
Access from Address	t_{ADA}	–	150	250	–	200	350	–	250	450	ns
Output Valid from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	–	150	250	–	200	350	–	250	450	ns
Output Valid from Chip-Select 2	t_{DOA2}	–	150	250	–	200	350	–	250	450	ns
Output Active from Output Disable	t_{DOA3}	–	–	110	–	–	150	–	–	200	ns
Output Hold from $\overline{\text{Chip-Select 1}}$	t_{DOH1}	20	–	–	20	–	–	20	–	–	ns
Output Hold from Chip-Select 2	t_{DOH2}	20	–	–	20	–	–	20	–	–	ns
Output Hold from Output Disable	t_{DOH3}	20	–	–	20	–	–	20	–	–	ns
Write Cycle Times											
Write Cycle	t_{WC}	300	–	–	400	–	–	500	–	–	ns
Address Setup	t_{AS}	110	–	–	150	–	–	200	–	–	ns
Write Recovery	t_{WR}	40	–	–	50	–	–	50	–	–	ns
Write Width	t_{WRW}	150	–	–	200	–	–	250	–	–	ns
Data In Width Effective	t_{DIW}	150	–	–	200	–	–	250	–	–	ns
Data In Hold	t_{DIH}	40	–	–	50	–	–	50	–	–	ns
$\overline{\text{Chip-Select 1}}$ Setup	$t_{\overline{CSS1}}$	260	–	–	350	–	–	450	–	–	ns
Chip-Select 2 Setup	t_{CSS2}	260	–	–	350	–	–	450	–	–	ns
Output Disable Setup	t_{ODS}	110	–	–	150	–	–	200	–	–	ns

† Time required by a limit device to allow for the indicated function.
● Typical values are for T_A = 25°C and nominal V_{DD}.

MWS5101 Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%.

CHARACTERISTIC		TEST CONDITIONS		LIMITS			UNITS
		V_O (V)	V_{IN} (V)	MWS5101D MWS5101E			
				Min.	Typ.●	Max.	
Quiescent Device Current, I_{DD}	L1 Types	–	0,5	–	–	10	µA
	L2 Types	–	0,5	–	–	50	
	L3 Types	–	0,5	–	–	200	
	L8 Types	–	0,5	–	–	500	
Output Voltage: Low-Level,	V_{OL}	–	0,5	–	0	0.1	V
High-Level,	V_{OH}	–	0,5	4.9	5	–	
Input Low Voltage,	V_{IL}	0.5,4.5	–	–	–	1.5	
Input High Voltage,	V_{IH}	0.5,4.5	–	3.5	–	–	
Output Low (Sink) Current,	I_{OL}	0.4	0,5	2	4	–	mA
Output High (Source) Current,	I_{OH}	4.6	0,5	–1	–2	–	
Input Current,	I_{IN}	–	0,5	–	–	±1	µA
3-State Output Leakage Current, I_{OUT}	L1 Types	0,5	0,5	–	–	±1	
	L2 Types	0,5	0,5	–	–	±1	
	L3 Types	0,5	0,5	–	–	±1	
	L8 Types	0,5	0,5	–	–	±2	
Operating Current,	I_{DD1}†	–	0,5	–	4	8	mA
Input Capacitance,	C_{IN}	–	–	–	5	7.5	pF
Output Capacitance,	C_{OUT}	–	–	–	5	7.5	

† Outputs open-circuited; cycle time = 1 µs.
● Typical values are for T_A = 25°C and nominal V_{DD}.

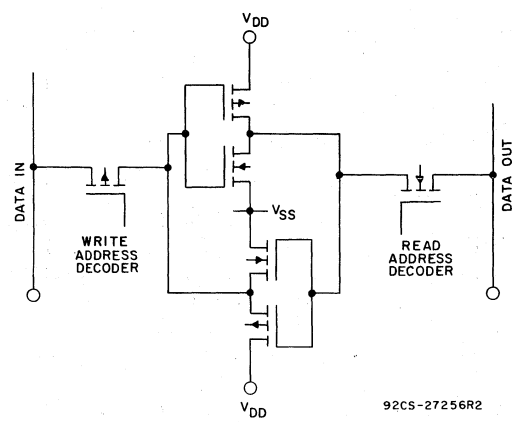


Fig. 3 – Memory cell configuration.

MWS5101 Types

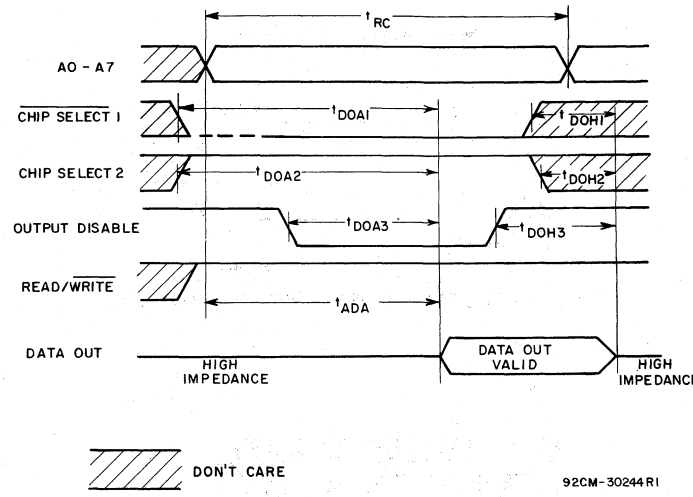
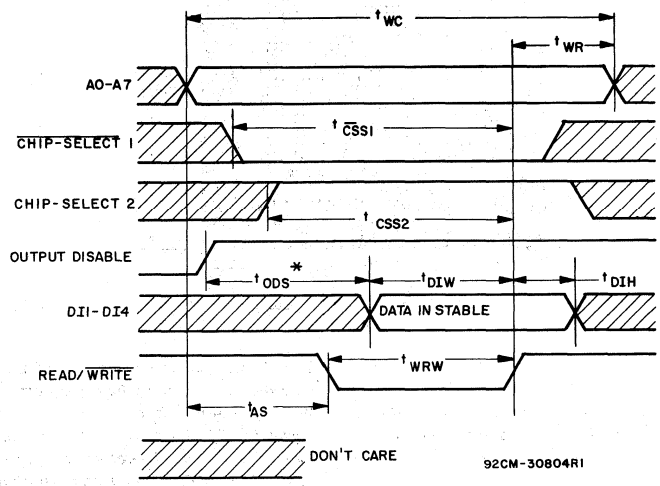


Fig. 4 — Read cycle waveforms and timing diagram.



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY; FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE.

Fig. 5 — Write cycle waveforms and timing diagram.

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70°C; See Fig. 6.

CHARACTERISTIC	TEST CONDITIONS		MWS5101D MWS5101E			UNITS
		V_{DD} (V)	Min.	Typ.●	Max.	
Minimum Data Retention Voltage, V_{DR}			–	1.5	2	V
Data Retention Quiescent Current, I_{DD} — L1 Types	V_{DR}=2 V		–	1	5	μA
Data Retention Quiescent Current, I_{DD} — L2 Types			–	2	15	μA
Data Retention Quiescent Current, I_{DD} — L3 Types			–	5	50	μA
Data Retention Quiescent Current, I_{DD} — L8 Types			–	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}		5	600	–	–	ns
Recovery to Normal Operation Time, t_{RC}		5	600	–	–	ns

● Typical values are for T_A = 25°C and nominal V_{DD}.

MWS5101 Types

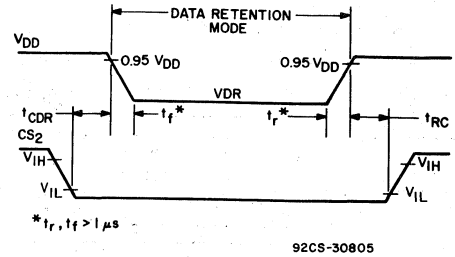
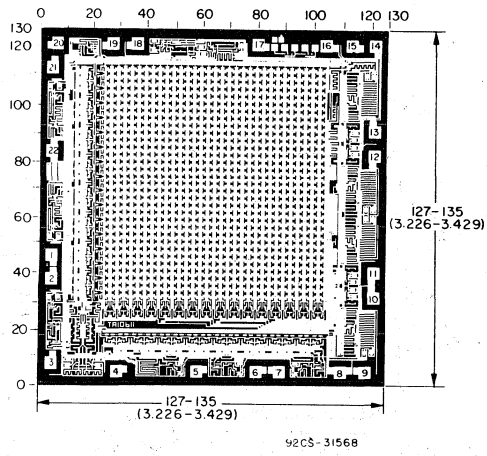


Fig. 6 – Low V_{DD} data retention waveforms and timing diagram.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

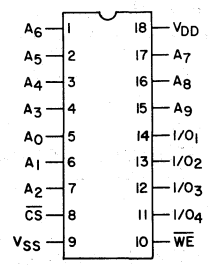
Dimensions and pad layout for MWS5101H.

MWS5114 Types

COS/MOS 1024-Word by 4-Bit LSI Static RAM

Features:

- **Fully static operation**
- **Low standby and operating power**
- **Industry standard 1024 x 4 pinout (same as pinouts for 6514, 2114, 9114, and 4045 types)**
- **Common data input and output**
- **Single power supply operation**
- **Memory retention for stand-by battery voltage as low as 2 V min.**
- **All inputs and outputs directly TTL compatible**
- **3-state outputs**



TERMINAL ASSIGNMENT

The RCA-MWS5114 is a 1024-word by 4-bit static random-access memory that uses the RCA ion-implanted silicon gate silicon-on-sapphire complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply fo 4.5 to 5.5 V.

The MWS5114 is supplied in 18-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal) . . . . . −0.5 to 7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) . . . . . −55 to +125°C
PLASTIC PACKAGES (E SUFFIX TYPES) . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

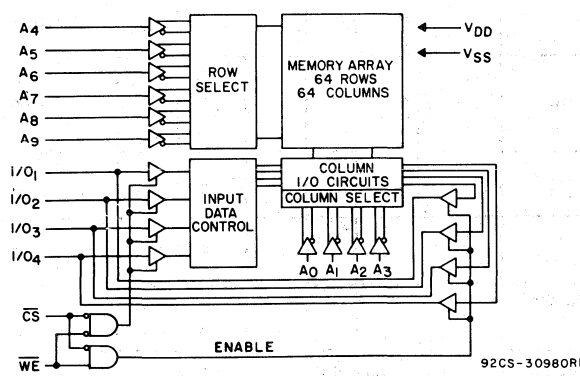


Fig. 1 — Functional block diagram for MWS5114.

MWS5114 Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C

For maximum reliability, operating conditions should be selected so that operation is always withing the following ranges:

CHARACTERISTIC	RANGE ALL TYPES	UNITS
DC Operating-Voltage	4 to 6	V
Input Voltage	V_{SS} to V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				MWS5114			MWS5114-5			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	–	20	50	–	–	100	µA
(V_{IN} = V_{DD} or V_{SS}, $\overline{CS}$ = High Level)	–	0,2	2	–	1	15	–	5	25	
Output Low Drive (Sink) Current, I_{OL} Min.	0.4	0,5	5	2	4	–	2	4	–	mA
Output High Drive (Source) Current, I_{OH} Min.	4.6	0,5	5	–0.4	–1	–	–0.4	–1	–	mA
Output Voltage Low-Level V_{OL} Max.	–	0,5	5	–	0	0.1	–	0	0.1	V
Output Voltage High Level, V_{OH} Min.	–	0,5	5	4.9	5	–	4.9	5	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	–	1.2	0.8	–	1.2	0.8	V
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	2.4	–	–	2.4	–	–	
Input Current, I_{IN} Max.	–	0,5	5	–	±0.1	±1	–	±0.1	±1	µA
3-State Output Leakage Current I_{OUT}	0,5	0,5	5	–	±0.5	±5	–	±0.5	±5	µA
Operating Current, I_{DD1}#	–	0,5	5	–	4	–	–	4	–	mA
Input Capacitance C_{IN}	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}	–	–	–	–	5	7.5	–	5	7.5	

*Typical values are for T_A = 25°C and nominal V_{DD}. #Outputs open circuited; cycle time = 1 µs.

MWS5114 Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70°C, V_{DD} = 5 V ±5%, t_r,t_f = 10 ns; C_L = 50 pF and 1 TTL Load

CHARACTERISTIC		LIMITS						UNITS
		MWS5114			MWS5114-5			
		Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Read Cycle Times See Fig. 2								
Read Cycle	t_{RC}	650	450	–	650	450	–	ns
Access	t_{AA}	–	450	650	–	450	650	
Chip Selection to Output Valid	t_{CO}	–	400	600	–	400	600	
Chip Selection to Output Active	t_{CX}	20	100	–	20	100	–	
Output 3-state from Deselection	t_{OTD}	–	125	175	–	125	175	
Output Hold from Address Change	t_{OHA}	50	150	–	50	150	–	

† Time required by a limit device to allow for the indicated function.
● Typical values are for T_A = 25°C and nominal V_{DD}.

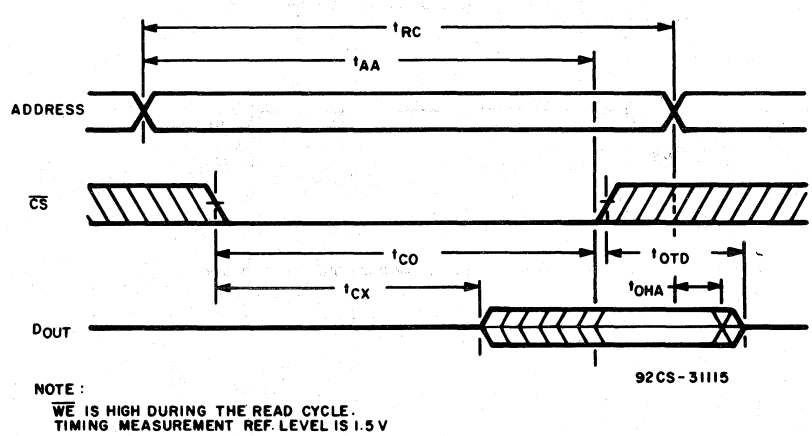


Fig. 2 – Read cycle waveforms.

MWS5114 Types

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70°C; See Fig. 4

CHARACTERISTIC		TEST CONDITIONS		MWS5114			UNITS
			V_{DD} (V)	Min.	Typ.●	Max.	
Data Retention Voltage,	V_{DR}			2	–	–	V
Data Retention Quiescent Current, I_{DD}	MWS5114	V_{DR} = 2 V		–	1	15	μA
	MWS5114-5			–	5	25	
Chip Deselect to Data Retention Time,	t_{CDR}		5	600	–	–	ns
Recovery to Normal Operation Time,	t_{RC}		5	600	–	–	

● Typical values are for T_A = 25°C and nominal V_{DD}.

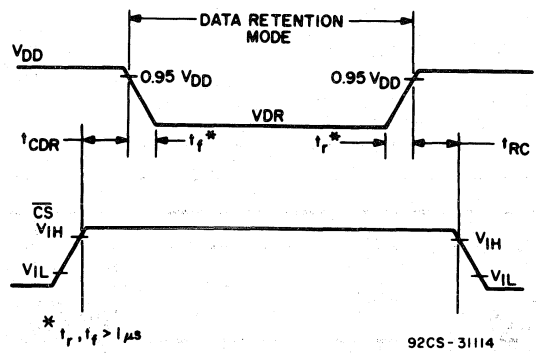


Fig. 4 – Low V_{DD} data retention waveforms and timing diagram.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA COS/MOS devices have a network for electrostatic protection during handling. Recommended handling practices for COS/MOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}–V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

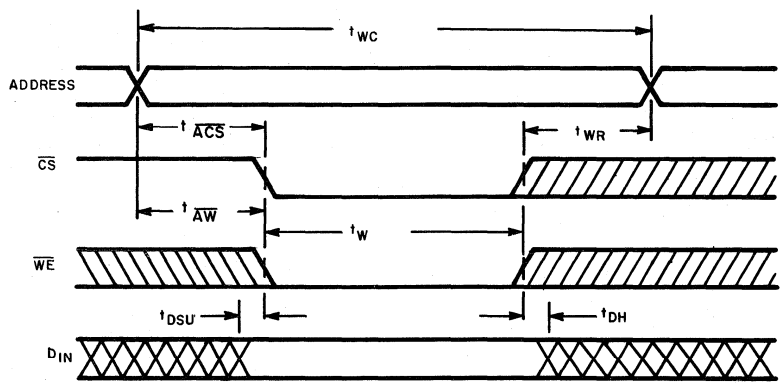
Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70°C, V_{DD} = 5 V ±5%, t_r,t_f = 10 ns; C_L = 50 pF and 1 TTL Load

CHARACTERISTIC		LIMITS						UNITS
		MWS5114			MWS5114-5			
		Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Write Cycle Times See Fig. 3								
Write Cycle	t_{WC}	500	400	–	500	400	–	ns
Write	t_W	450	350	–	450	350	–	
Write Release	t_{WR}	50	25	–	50	25	–	
Address to Chip Select Set-Up Time	$t_{\overline{ACS}}$	0	0	–	0	0	–	
Address to Write Set-Up Time	$t_{\overline{AW}}$	50	0	–	50	–	–	
Data to Write Set-Up Time	t_{DSU}	0	0	–	0	0	–	
Data Hold from Write	t_{DH}	30	10	–	30	10	–	

† Time required by a limit device to allow for the indicated function.
● Typical values are for T_A = 25°C and nominal V_{DD}.



NOTE: $\overline{WE}$ IS LOW DURING THE WRITE CYCLE
TIMING MEASUREMENT REF. LEVEL IS 1.5 V

Fig. 3 – Write cycle waveforms.

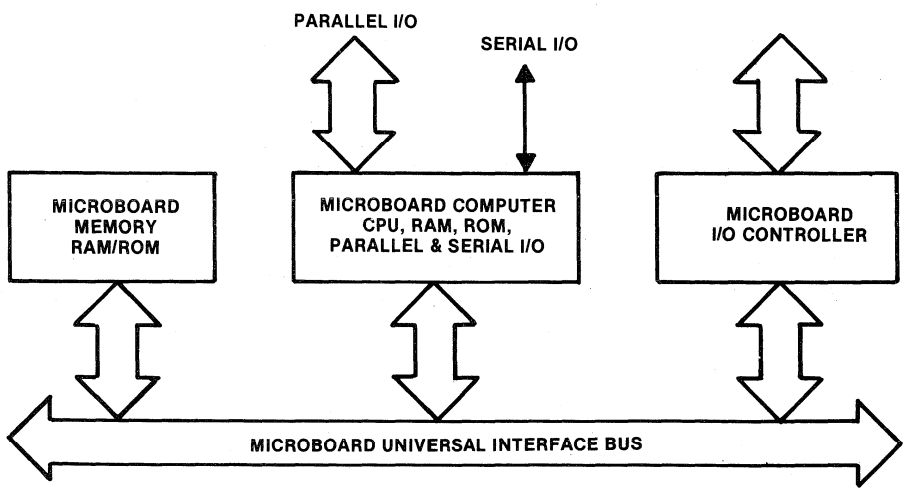
COSMAC Microboard Computer Systems (CMOS Single-Board Computers and Associated Microboard Products)

Technical Data

Features and Functional Classifications

The RCA CDP18S600 Series offers a line of single-board computers plus a variety of expansion memory and I/O boards and accessory hardware. These boards may be combined to provide customized microcomputer systems for specific applications. RCA offers designers low-power CMOS computer boards engineered and tested to reduce the time required for the user to develop the over-all system. These ready-to-use microboard modules provide the following significant advantages.

- **Simple to Use**—Simply select the 4.5 x 7.5-inch Microboard modules your system needs, plug them on to the Microboard 5- or 25-card chassis with COSMAC Microboard Universal Backplane, and add a milliwatt power supply. You are ready to begin the development of the software for your application. No hand-wired breadboards, no hardware headaches, no design delays.
- **Low-Power Operation**—Utilizing all CMOS components, your RCA COSMAC Microboard system can be powered from a small supply, a wall supply, or even a battery. The integral battery option of the Microboard 8K RAM can be used to power the entire system.
- **Low-Cost Power Supply**—The low power requirements of the Microboard modules coupled with their wide operating-range capabilities allow use of low-cost power supplies having extended regulation limits. No longer does the power supply have to be bigger, bulkier, and heavier than the entire system. And you eliminate cooling fans along with associated reliability hazards.
- **Easy to Modify**—With the COSMAC Microboard Universal Backplane, any Microboard module works in any location. Use the broad selection of readily interchangeable Microboard modules. Simply exchange or add modules to match your changing design requirements. Lots of flexibility without hardware design headaches.
- **Excellent Noise Immunity**—CMOS technology provides reliable operation in high-noise process-control, automotive, and production-monitoring environments. No ground plane or extra decoupling capacitors needed.
- **Development System Compatibility**—All Microboard modules are designed to plug directly into the COSMAC Development Systems to facilitate rapid hardware and software development. The RCA COSMAC DOS Development System provides Editor, Assembler (Level I, II, and MACRO), Disk Operating System, Utility, and many other useful programs for the neophyte-to-expert software designer. And RCA provides ample technical literature and field engineering support.



Block diagram illustrating interconnection of Microboard modules.

Features and Functional Classifications

COSMAC Microboard Selection Guide

Single Board Computers

	Clock Freq.	RAM	ROM/ EPROM (Sockets)	Serial I/O Lines	Parallel I/O Lines
CDP18S601	2 MHz	4K	4K/8K	1	25
CDP18S602	2 MHz	2K	2K/4K/8K	1 (UART)	21
CDP18S603	2 MHZ	1K	4K/8K	1	25

Memory-I/O Expansion Boards

	RAM (Bytes)	ROM/ EPROM (Sockets)	Serial I/O Lines	Parallel I/O Lines	Other
CDP18S620	4K	—	—	—	—
CDP18S621	16K	—	—	—	—
CDP18S621V1	16K	—	—	—	—
CDP18S622	8K	—	—	—	Battery Back-Up
CDP18S623	8K	—	—	—	—
CDP18S625	—	8K/16K	—	—	—
CDP18S640,V1	256	4K/8K	—	—	Control Switches 6 Digit Hex Display
CDP18S641	—	—	1 (UART)	—	—
CDP18S642	—	—	—	—	D/A Converter
CDP18S643	—	—	—	—	A/D Converter
CDP18S660	2K	4K/8K	—	40	—

Microboard Prototyping Systems

CDP18S691 — Prototyping System (Includes CDP18S601, CDP18S640, CDP18S659, Monitor Firmware, 5 Card Encased Chassis, Cables, Documentation)
CDP18S692 — Prototyping System (Same as CDP18S691 Except Contains CDP18S602 Computer Board)

Microboard System Development Aids

CDP18S023,V3— 5 Volt Power Supply
CDP18S659 — Blank Breadboard
CDP18S670 — 25 Card Chassis with Power Supply
CDP18S675 — 5 Card Chassis
CDP18S676 — 5 Card Encased Chassis
CDP18S480 — PROM Programmer
CDP18S502 — Extender Card

CDP18S601

RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S601 is a versatile computer system on a single 4.5×7.5 inch card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S601 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application. The CDP18S601 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007 facilitating prototype design and the debugging of both hardware and software.

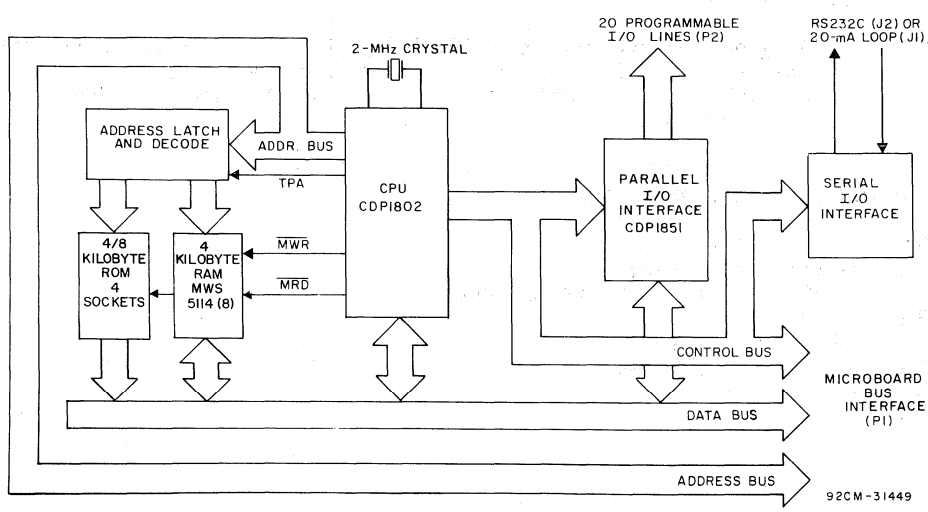
Component Features

Central Processing Unit. The central processor for the CDP18S601 Microboard Computer is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Inter-

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required—10 mA (typ.)†
- High noise immunity
- 2-MHz crystal clock
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 4 kilobytes of read/write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 20 programmable parallel I/O lines
- 4 flag inputs
- Q serial data output
- RS232C or 20-mA serial I/O
- 65,536-byte memory space
- 44-pin system interface
- Temperature range −0 °C to 70 °C
- Small board size—4.5×7.5 inches

†With CMOS ROM and RS232C serial interface.



Block diagram of RCA COSMAC Microboard Computer CDP18S601.

rupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of eight MWS5114 RAM's, the CDP18S601 provides 4 kilobytes of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S601 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

Application

The COSMAC Microboard Computer CDP18S601 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may also be operated in conjunction with other Microboard System components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S601 Microboard Computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC CDOS Development System CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Specifications

Memory Capacity

On-board RAM: 4 kilobytes

On-board ROM/EPROM: 4 sockets for up to 16 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Any even 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Operating Temperature Range

0 °C to 70 °C.

Dimensions

4.5 inches × 7.5 inches (114.3 × 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

With CMOS ROM's, with RS232C: +5 V at 10 mA, typical operating

With CMOS ROM's and 20-mA loop: +5 V at 30 mA, typical operating

Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

CDP18S601

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the COSMAC Microboard Computer CDP18S601 and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

DB7 through DB0—Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2—Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{MRD}$ line. When high, $\overline{MRD}$ indicates data transfer from I/O to memory; when low, from memory to I/O.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$—Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. The CDP18S601 uses EF1 and EF2, conditioned by the secondary I/O address, to test the READY state of I/O ports A and B. The serial data interface input is presented directly on EF4 or EF3 chosen by link LK36. I/O devices using the INT line may make use of the EF lines to identify the device. They may also be used to indicate priority or status.

INT—Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as program counter.

$\overline{DMAI}$, $\overline{DMAO}$—Taken directly to the CPU pins and not utilized by the CDP18S601, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and/or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0—State code outputs from the CPU which identify the type of machine cycle in progress.

	State Code Lines	
State Type	**SC1**	**SC0**
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB—Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

A7 through A0—Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDP18S601 buffers, latches, and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

$\overline{\text{MWR}}$—A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

$\overline{\text{MRD}}$—A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless MRD is properly used to condition data output.

Q—A single-bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions. The CDP18S601 may use Q as a serial data output to the RS232C and 20-mA data terminal drivers. It is also available for other uses through the Microboard Bus (P1) and Parallel I/O (P2) connectors. Q may also be tested with a branch instruction and thereby operates as a program switch.

CLOCK OUT—A 2-MHz square-wave clock provided for general use. It is derived from the crystal-controlled oscillator in the CPU.

$\overline{\text{WAIT}}$, $\overline{\text{CLEAR}}$—Two control inputs to the CPU which determine the mode of operation.

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

Load Mode. Holds the CPU in the IDLE state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that termination of the DMA-IN operation does not force execution of the next instruction. DMA IN requests then load memory starting from location zero for as many bytes as there are DMA IN requests.

Reset Mode. Registers I, N, and Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, and registers X, P, and R0 are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2, but never an S3. Power-up reset is obtained by a Schmitt-trigger buffered RC network connected to $\overline{\text{CLEAR}}$.

Pause Mode. Stops the internal CPU timing generator on the first high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run Mode. May be initiated from the Pause or Reset Mode functions. If initiated from Pause, the CPU resumes operation on the first high-to-low transition of the input clock. If initiated from Reset, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU—Run Utility Software. A signal supplied to the CDP18S601 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S601 is 4 kilobytes of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy any even 4-kilobyte block in the memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

CDP18S601

Table I—4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK10, LK11, or LK22 Pin Connections
0000 - 0FFF	1:16, 5:12
1000 - 1FFF	1:16, 6:11
2000 - 2FFF	1:16, 7:10
3000 - 3FFF	1:16, 8:9
4000 - 4FFF	2:15, 5:12
5000 - 5FFF	2:15, 6:11
6000 - 6FFF	2:15, 7:10
7000 - 7FFF	2:15, 8:9
8000 - 8FFF	3:14, 5:12
9000 - 9FFF	3:14, 6:11
A000 - AFFF	3:14, 7:10
B000 - BFFF	3:14, 8:9
C000 - CFFF	4:13, 5:12
D000 - DFFF	4:13, 6:11
E000 - EFFF	4:13, 7:10
F000 - FFFF	4:13, 8:9

LINK 11 is associated with the 4-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

Two types of links are provided and must be made up by the user to suit the particular ROM configuration selected. The first link type is for accommodating the type of ROM selected (CDP1834, 2708, 2758, or 2716. The second link type is for selecting the memory address space to be occupied by the ROM.

Link LK4 is an 18-pin dual-in-line arrangement with preprinted links to accommodate the CDP1834 or 2708 ROM's. Table II gives the connections required for each ROM type.

Links LK10 and LK22 are 16-pin dual-in-line arrangements with no preprinted links. A DIP switch may be installed if frequent address changes are expected. Link LK10 provides the high-order four address bits decoded so that two links or jumpers place sockets XU24 and XU25 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK22 does the same for sockets XU26 and XU27. See Table I for address map and link connections.

To avoid having floating inputs to the gates, both links LK10 and LK22 should always have two jumpers. For example, if sockets XU26 and XU27 are unused, LK22 may be jumpered the same as LK10. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK10 and LK22 should be jumpered identically in accordance with Table II. Then, the ROM's should be installed in sockets XU25, XU27, XU24, and XU26, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK10 and LK22 should be jumpered independently in accordance with Table II for the required two 4-kilobyte blocks. Then, socket XU25 is the low 2 kilobytes and socket XU24 is the high 2 kilobytes of the 4-kilobyte block as set in LK10. Similarly, socket XU27 is the low 2 kilobytes and socket XU26 is the high 2 kilobytes of the 4-kilobyte block set in LK22.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with two-kilobyte ROM's type 2716. If all links are set up for the 2-kilobyte ROM's as shown in Table II for LK4, and LK10 and LK22 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU25 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU24, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU24 or socket XU25 while the other is occupied by a 1-kilobyte ROM. Socket XU27 (low 2 kilobytes) and socket XU26 (high 2 kilobytes) may be used in the same manner.

Table II - ROM Type Selection Links

Link LK4 Pins	ROM Type CDP1834*	2708*	2758	2716
1:18	X	OPEN	SHORTED	SHORTED
2:17	X	SHORTED	OPEN	OPEN
3:16	SHORTED	SHORTED	SHORTED	OPEN
4:15	OPEN	OPEN	OPEN	SHORTED
5:14	OPEN	OPEN	OPEN	SHORTED
6:13	SHORTED	SHORTED	SHORTED	OPEN
7:12	X	SHORTED	OPEN	OPEN
8:11	X	OPEN	OPEN	SHORTED
9:10	X	OPEN	SHORTED	OPEN

*X = don't care; Link LK4 is prewired to accept CDP1834 or 2708.

I/O Operation

Serial I/O Interface. Serial data output is generated by the Q line from the CPU. Thus, software using the SET Q and RESET Q instructions generates data rate and format. Serial data input is presented to either EF3 or EF4, selectable by links as shown in Table III. The software uses the test branch instructions to decode incoming data.

Table III—Link Table for Serial Data In

Link LK36	Function
7:10	Data to EF3
8:9	Data to EF4

Electrical interfaces for either the 20-mA loop or RS232C data terminals are provided on connectors J1 and J2 respectively. Output drivers are separate but the input receiver is shared. The only modification required for RS232C interface is the installation of a jumper wire in the C5 holes.

Two-Level I/O Addressing Conventions. During an I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

- The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard in the system having an I/O function.
- The group number is divided into two parts, the lower four bits being a one-of-four encoding and the high four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the 6 commands left after reserving the 61 and 69. The total number of useful I/O addresses is 114.
- The 69 input instruction is reserved for reading the latched output of the 61 instruction. The CDP18S601 does not provide this feature, but it may be added where desired.

The use of the two halves of the group number must be independent and exclusive. That is, the high-order bits must be zero when any low-order bit is used, and the low-order bits must be zero when the high-order bits are used. Once a group number is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by devices assigned to that group number.

The CDP18S601 uses bit three as the group select; that is, the group number $(08)_{16}$ or $(0000\ 1000)_2$ is transmitted by the 61 output instruction to select the programmable I/O on board.

Parallel I/O Interface. The parallel I/O interface consists of 20 lines provided on connector P2. These 20 lines are generated by the CDP1851 Programmable I/O Interface and may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides the Q line, EF1 through EF4, CLEAR, three different voltages, and a logic ground.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device.

The CDP1851 is assigned to I/O group eight. Therefore, in order to enable access, a 61 output instruction with data = 08 is required before read, write, or control I/O may be performed.

Signal ARDY conditioned by the group select generates EF1; BRDY and group select generates EF2. Link LK41, pins A and B may be jumpered if interrupt-driven software is to be used. Then, INTA or INTB generates INT unconditionally.

Once the group select is accomplished, N1 and N2 are used to address the CDP1851. The following read and write instructions are used to access data, status, and command registers.

62—Write to control register

64—Write to Port A data register (if A is an output)

66—Write to Port B data register (if B is an output)

6A—Read status register

6C—Read Port A data register (if A is an input)

6E—Read Port B data register (if B is an input)

Using the READY Lines for Data Synchronization. The Port A and Port B RDY lines are presented to the CPU EF1 and EF2 lines when the group select is set.

CDP18S601

Note that there is a logic reversal: when RDY is true, the EF is false. A test for ARDY true might use the B1 instruction (34) which would take the branch if ARDY were false. Even through these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU.

When a port designated as an **output** port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true), and load the next output byte. When a port is designated as an **input** port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and then reads the input byte. **In this case, a dummy read after reset is necessary to raise the first RDY.**

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

Using the INTERRUPT Line for Data Synchronization. If link LK41, A:B is jumpered, INTA or INTB generates INT to the CPU. INT is not conditioned by the group select.INT is set by the remote device sending STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table IV summarizes the actions of READY and INT for input and output modes.

The software can find the source of the interrupt by setting the group select 08, and then, either testing the RDY lines or reading the status byte. The low-order two bits of the status byte are: bit 0 = INTB; bit 1 = INTA.

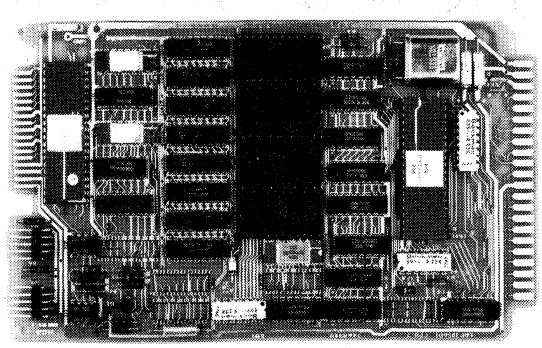
Bidirectional Mode. Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, ARDY and ASTB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and BSTB becomes A OUTPUT STB. Each of the eight lines AD0—AD7 may transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that output data is gated into AD0—AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Bit-Programmable Mode. Both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Table IV—READY and INTERRUPT Actions for Input and Output Modes.

		Output Port	Input Port
READY	Set By	Loading Data	Reading Data
	Reset by	STB leading edge	STB leading edge
INTERRUPT	Set by	STB trailing edge	STB trailing edge
	Reset by	Loading Data	Reading Data



Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development System CDP18S005

Replacement of the CDS II CPU Module CDP18S102 with the RCA COSMAC Microboard Computer CDP18S601 requires some link changes on the CDP18S601. These changes are:

LK 43—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS II backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

LK 36 —Serial Data In to external flag lines. Connect pins 7:10 for EF3 or pins 8:9 for EF4. If the CDS Terminal Interface Module CDP18S507 in location 14 is to be retained, do not use EF4 on this board. Otherwise, a conflict on EF4 is created.

LK 36—RNU to start ROM's at address 8000. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS II backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed.

Microboard Computer Bus Interface (P1)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMAI-N
B	TPB-P	2	DMAO-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	−5V/−15V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12V/+15V
Y	+5V	21	+5V
Z	GND	22	GND

Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+5V
31	EF2-N	32	−5V/−15V
33	EF1-N	34	+12V/+15V

CDP18S601

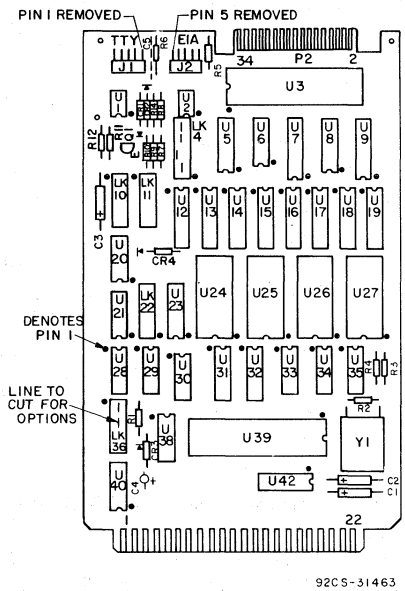
LK 10, 11, and 22—Set up as previously described for the memory address desired, taking care that the CDS II memories are not assigned to overlap the assignment of the CDP18S601 Microboard Computer.

Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND



Layout diagram of RCA COSMAC Microboard Computer CDP18S601.

Parts List

C1, C2, C3=15μF, 20 V
C4=1.5 μF, 35 V

CR1, CR2, CR3, CR4=1N270

J1, J2=connector, right angle (mates with connector comprised of housing - AMP 1-86148-2, contact - AMP 86016-1, keying plug - AMP 87077-1, or equivalent)

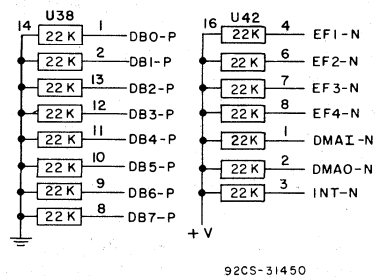
Q1=2N5139

R1=100 kΩ, ¼ W, 5%
R2=22 MΩ, ¼ W, 5%
R3, R4,=22 kΩ, ¼ W, 5%
R5=3 kΩ, ¼ W, 5%
R6, R14=1 kΩ, ¼ W, 5%
R7=11 kΩ, ¼ W, 5%
R8=4.3 kΩ, ¼ W 5%
R9=130 Ω, ¼ W, 5%
R10=10 kΩ, ¼ W, 5%
R11=2.7 kΩ, ¼ W, 5%
R12=220 Ω, ¼ W, 5%

U1=CA3160
U2=CA3140
U3=CDP1851CE
U5, U8=CDP1856CE
U6=CD4069BE
U7=CDP1867CE
U9=CDP1866CE
U12-U19=MWS5114E-5
U20, U38=resistor module, 22 kΩ, 14 pin
U21=CD4001BE
U23=CDP1858CE
U28, U29=CD4012BE
U30=CD4016BE
U31, U32=CD4050BE
U33=CD4025BE
U34=CD4013BE
U35=CD4023BE
U39=CDP1802CE
U40=CD4093BE
U42=resistor module, 22 kΩ, 16 pin

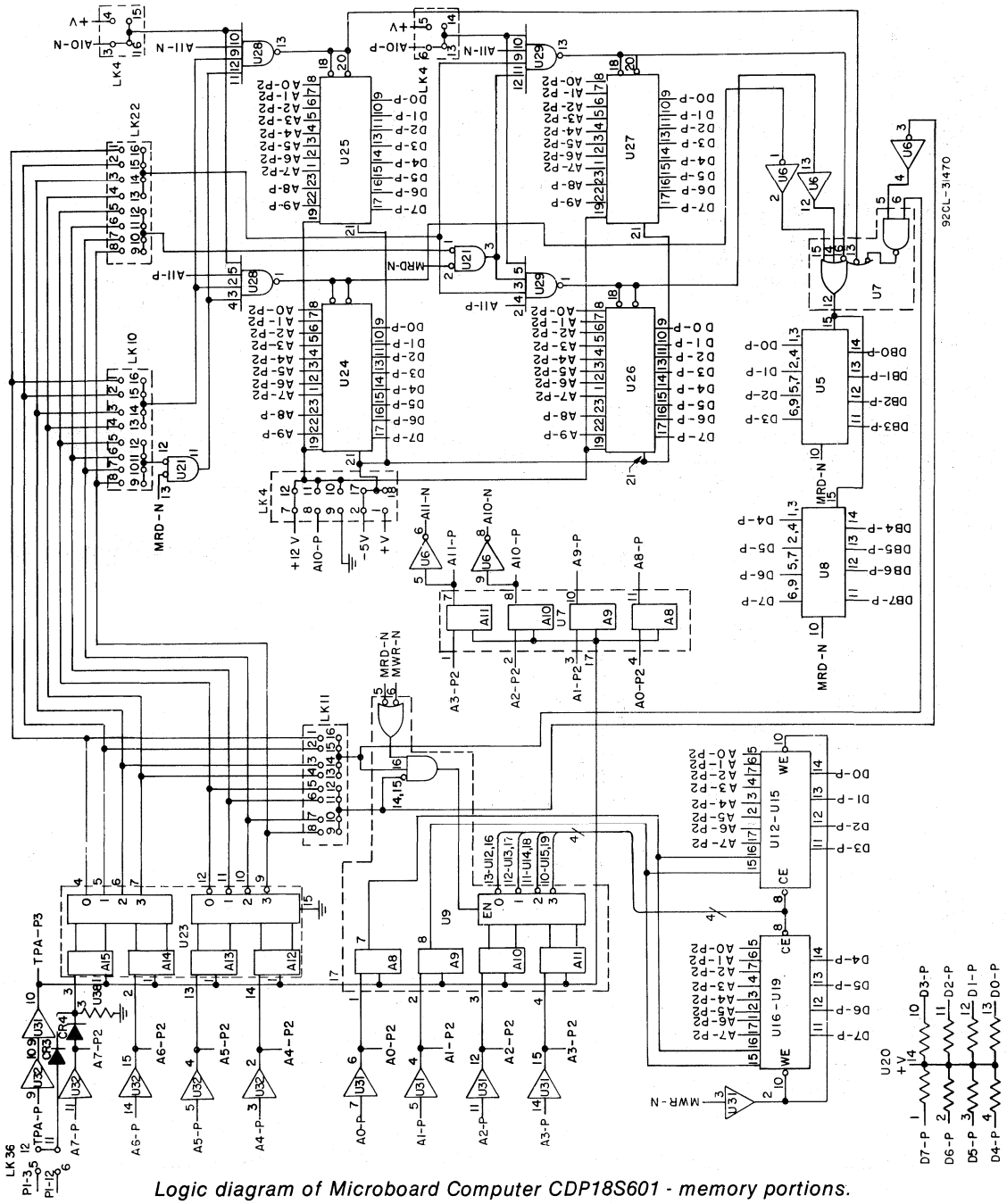
XU24-XU27=24-pin socket
XU39=40-pin socket

Y1=2.00-MHz crystal



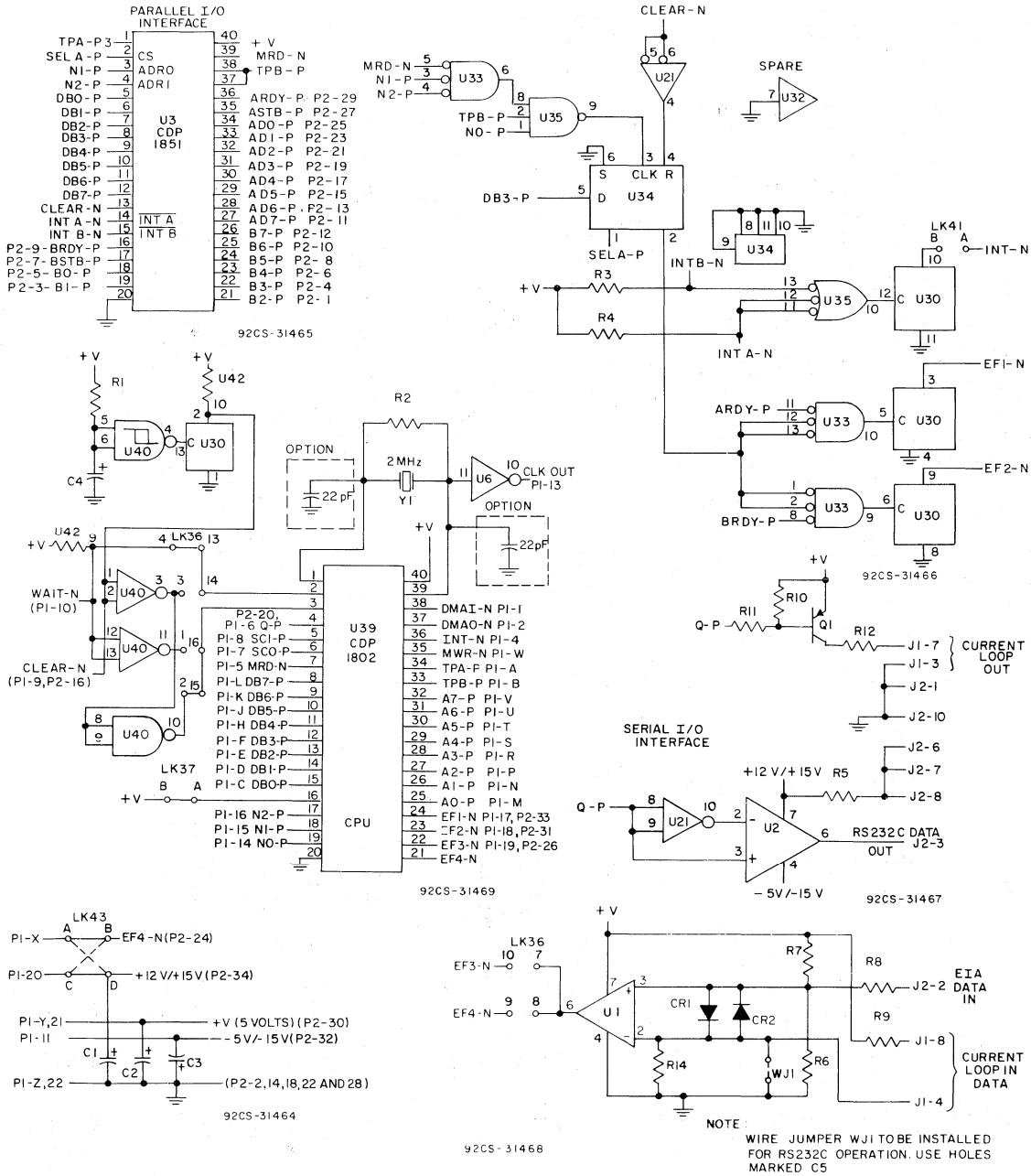
Pull-down and pull-up resistors.

CDP18S601



Logic diagram of Microboard Computer CDP18S601 - memory portions.

CDP18S601



Logic diagram of Microboard Computer CDP18S601 - CPU and interface portions.

CDP18S602

RCA COSMAC Microboard Computer

Advance Data

The RCA COSMAC Microboard Computer CDP18S602 is a versatile computer system on a single 4.5 x 7.5 inch printed-circuit card, The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a UART serial communications interface, power-on reset, and expansion interface. Two on-board sockets are provided for read-only memory enabling the user to select 1, 2, 4, or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The CDP18S602 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and the special requirements of his specific application. The CDP18S602 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007, facilitating prototype design and the debugging of both hardware and software.

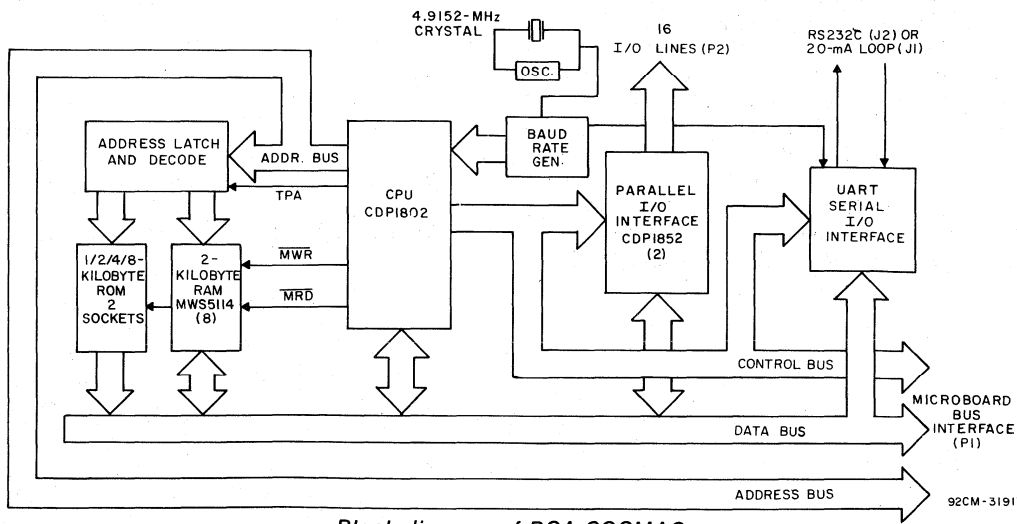
Component Features

Central Processing Unit. The central processor for the CDP18S602 Microboard Computer is the 8-bit

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required: 9 to 29 mA (typ.)*
- High noise immunity
- Selectable clock frequency
- UART with selectable baud rate
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 2 kilobytes of read/write memory
- Sockets for 1/2/4/8 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 16 parallel I/O lines
- 4 flag inputs; Q serial data output
- RS232C or 20-mA serial I/O
- 65,536 byte memory space
- 44-pin system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Powered through either expansion or I/O connector
- Temperature range: 0 °C to 70 °C
- Small board size: 4.5 x 7.5 inches

*Depending whether 20-mA serial interface is used.



Block diagram of RCA COSMAC Microboard Computer CDP18S602.

CDP18S602

silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of four MWS5114 RAM's, the CDP18S602 provides 2 kilobytes of CMOS read-write memory. In addition, two sockets are provided for one, two, four, or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2758, 2716, or 2732 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of two 8-Bit Byte I/O Ports, type CDP1852, the CDP18S602 provides eight input and eight output I/O lines. A UART-driven serial communications interface, having both 20-milliampere loop and EIA RS232C capability, is provided and has 14 switch-selectable baud rates from 50 to 9600 baud. Edge connectors are provided for the I/O lines and the Microboard bus interface. Right angle header connections are provided for the serial communications interfaces.

Application

The COSMAC Microboard Computer CDP18S602 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector, through the I/O connector, or wired directly to the board. It may also be operated in conjunction with other Microboard System Components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

Specifications

Memory Capacity
- On-board RAM: 2 kilobytes
- On-board ROM/EPROM: 2 sockets for up to 8 kilobytes
- Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM

Memory Address Map
- On-board RAM: Any four-kilobyte block
- On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1, 2, 4, or 8-kilobyte block

I/O Capacity
- Parallel: 8 input; 8 output; 4 flag input; 1 Q output
- Serial: UART, 14 selectable baud rates from 50 to 9600 baud

Operating Temperature Range
- 0 °C to 70 °C

Dimensions
- 4.5 inches x 7.5 inches (114.3 x 190.5 mm)
- Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
- With CMOS ROM's and RS232C: +5 V at 9 mA, typical operating
- With CMOS ROM's and 20-mA loop: +5 V at 28 mA, typical operating
- Optional voltages used only for RS232C interface:
  - +12 to +15 V at 8 mA, typical
  - −5 to −15 V at 8 mA, typical

Connectors
- System Interface: Edge fingers, 44 pins on 0.156-inch centers
- Parallel I/O: Edge fingers, 34 pins on 0.100 inch centers
- Serial I/O: Right-angle header, 10 pin

Clock
- Selectable, crystal controlled; 2.4576, 1.2288, 0.6144, or 0.3072 MHz

CDP18S603

RCA COSMAC Microboard Computer

The RCA COSMAC Microboard Computer CDP18S603 is a versatile computer system on a single 4.5 × 7.5 inch card. The card contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power-on reset, and expansion interface. Four on-board sockets are provided for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. The CDP18S603 Microboard Computer is designed to provide the key hardware for various microcomputer applications allowing the designer to concentrate on the software and special requirements of his specific application. The CDP18S603 is plug-in compatible with the RCA COSMAC Development System II CDP18S005 and the RCA COSMAC CDOS Development System CDP18S007 facilitating prototype design and the debugging of both hardware and software.

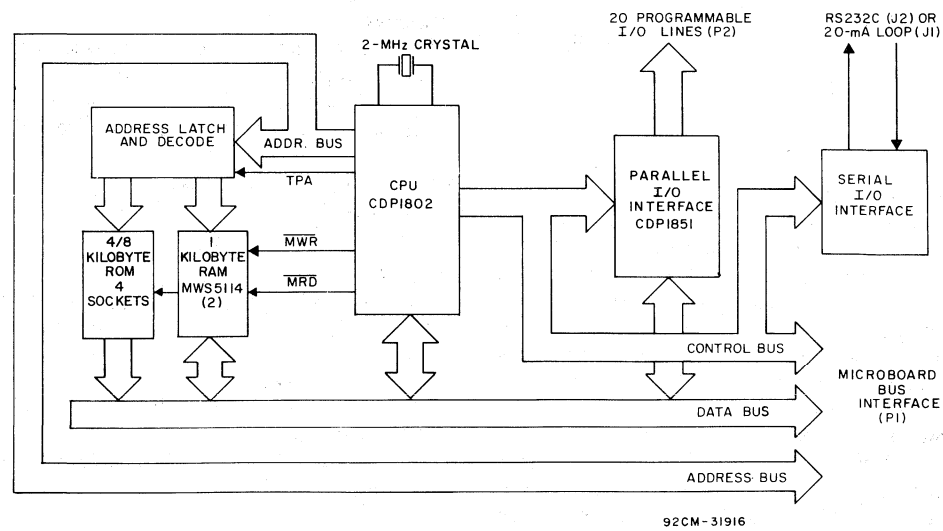
Component Features

Central Processing Unit. The central processor for the CDP18S603 Microboard Computer is the 8-bit

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Current required—7 to 27 mA (typ.)†
- High noise immunity
- 2-MHz crystal clock
- Compatible with COSMAC Development Systems
- Stand-alone capability
- 1 kilobyte of read/write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- Power-on reset
- COSMAC Microprocessor architecture
- Flexible memory and I/O expansion
- 20 programmable parallel I/O lines
- 4 flag inputs
- Q serial data output
- RS232C or 20-mA serial I/O
- 65,536-byte memory space
- 44-pin system interface
- Temperature range −0 °C to 70 °C
- Small board size—4.5 × 7.5 inches

†Depending whether 20-mA serial interface is used.



Block diagram of RCA COSMAC Microboard Computer CDP18S603.

CDP18S603

silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter thereby giving the system multiple program states. Each register may also be used for data storage and as memory pointers for subroutines, I/O, stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

Memory. By means of two MWS5114 RAM's, the CDP18S603 provides 1 kilobyte of CMOS read-write memory. Four sockets are provided for four or eight kilobytes of non-volatile read-only memory. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one-kilobyte boundaries.

I/O. By means of the CMOS programmable I/O Interface CDP1851, the CDP18S603 provides twenty programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique "handshaking" signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard bus interface. Right-angle header connections are provided for the serial communications interfaces.

The CDP18S603 is the same as the CDP18S601 except that the CDP18S601 has 4 kilobytes of read/write memory.

Application

The COSMAC Microboard Computer CDP18S603 may stand alone and be operated as a complete system. Power may be supplied through the Microboard Bus Interface connector or the parallel I/O connector or wired directly to the board. It may also be operated in conjunction with other Microboard System components installed in any location in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670).

The low current requirements of the Microboard Computer and other Microboard Systems components permit operation from a simple, compact wall-type supply such as the CDP18S023. No cooling fans or heat sinks are required.

The CDP18S603 Microboard Computer may be installed in the card nest of the COSMAC Development System II CDP18S005 or the COSMAC CDOS Development System CDP18S007 in place of the CPU Module to facilitate software and hardware development. This feature substantially expands the designer's debugging capabilities by making it possible to debug the software of a specific application concurrently with the use and testing of the hardware on the CDS. Other development systems allow only software debugging, leaving it to the user to transport the software to the hardware under test. With the final Microboard hardware configuration imbedded in the COSMAC Development System, the application software and hardware may be operated together in the optimum situation for analysis and improvement. For example, RAM may easily be allocated in place of ROM, thereby saving much time that might have been used in programming PROM's or EPROM's.

Specifications

Memory Capacity

On-board RAM: 1 kilobyte

On-board ROM/EPROM: 4 sockets for up to 16 kilobytes.

Off-board Expansion: Up to 65,536 bytes in any user-specified combination of RAM, ROM, and EPROM.

Memory Address Map

On-board RAM: Low 1-kilobyte block in any 4-kilobyte block.

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block.

I/O Capacity

Parallel: 20 lines each programmable as input, output, or bidirectional.

Serial: One input, one output, choice of 20-mA loop or RS232C. User-programmed baud rate and format.

Operating Temperature Range

0 °C to 70 °C.

Dimensions

4.5 inches × 7.5 inches (114.3 × 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements

With CMOS ROM's, with RS232C: +5 V at 7 mA, typical operating

With CMOS ROM's and 20-mA loop: +5 V at 27 mA, typical operating

Optional voltages used only for RS232C interface:
+12 to +15 V at 8 mA, typical
−5 to −15 V at 8 mA, typical

Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers.

Parallel I/O: Edge fingers, 34 pins on 0.100-inch centers.

Serial I/O: Two right-angle headers, 10 pin.

Clock

CPU and Interface: 2-MHz crystal-controlled oscillator on CPU.

Microboard Bus Interface Signals (Connector P1)

The bus interface signals for the CDP18S603 are identical to those of the CDP18S601. Refer to pages 258 and 259 for details.

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. Links (wire jumpers) are to be installed as described below. As an alternative, DIP switches may be readily installed in place of the links because the links are arranged in standard 16-pin DIP dimensions.

RAM Address. The RAM on the CDP18S603 is 1 kilobyte of contiguous memory. The high-order four bits of memory address are latched and decoded, and a set of eight links is provided so that any value of the four high-order bits may be selected as the address of this RAM. Thus, the RAM may occupy 1 kilobyte starting at any even 4-kilobyte block in the memory space.

To set up the RAM address, install two jumpers in link LK11, according to Table I. Alternatively, a DIP switch may be installed if frequent changes are anticipated.

Table I—4-Kilobyte Link Connections

4-Kilobyte Address Space	LINK LK10, LK11, or LK22 Pin Connections
0000 - 0FFF	1:16, 5:12
1000 - 1FFF	1:16, 6:11
2000 - 2FFF	1:16, 7:10
3000 - 3FFF	1:16, 8:9
4000 - 4FFF	2:15, 5:12
5000 - 5FFF	2:15, 6:11
6000 - 6FFF	2:15, 7:10
7000 - 7FFF	2:15, 8:9
8000 - 8FFF	3:14, 5:12
9000 - 9FFF	3:14, 6:11
A000 - AFFF	3:14, 7:10
B000 - BFFF	3:14, 8:9
C000 - CFFF	4:13, 5:12
D000 - DFFF	4:13, 6:11
E000 - EFFF	4:13, 7:10
F000 - FFFF	4:13, 8:9

LINK 11 is associated with the 1-kilobyte RAM.
LINK 10 is associated with the ROM sockets 25 and 24.
LINK 22 is associated with the ROM sockets 27 and 26.

ROM Address. Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). The CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM chips may be used.

ROM addressing in the CDP18S603 is accomplished exactly the same as in the CDP18S601. Refer to page 260 for details.

I/O Operation

I/O operation in the CDP18S603 is the same as in the CDP18S601. Refer to pages 261 and 262 for details.

Power-On Reset

An RC integrator (R1 and C4 in the control circuit logic diagram) and a Schmitt-trigger circuit (U30) provide a long-time-constant (approximately 150 milliseconds) signal when the +5-volt supply is turned on. This signal appears in the CLEAR-N input to the CPU, the parallel I/O interface, and the I/O group-select latch. After the CLEAR signal, the I/O group select is reset, the parallel I/O interface Ports A and B are set to be input ports, the mask register is reset (monitors all bits), and the status register is reset. The CPU initializes and starts processing at location 0000 (provided the WAIT line is not asserted).

The power-on reset is generated through a transmission gate. External circuits, therefore, may generate CLEAR on P1-9 or P2-16 using transmission gates, three-state, or open-collector devices.

If power-on reset is **not** desired, the removal of C4 will disable it and an external CLEAR must be provided.

Installation in the COSMAC Development System CDP18S005

Replacement of the CDS II CPU Module CDP18S102 with the RCA COSMAC Microboard Computer CDP18S603 requires some link changes on the CDP18S603. These changes are:

LK 43—Cut A:B and C:D and install A:D and B:C. If +12-volt supply is not needed (it is required only for the RS232C data terminal transmitter and 2708 EPROM's), do not install A:D.

If the +12-volt supply is needed, wire it to location 12, pin X in the CDS II backplane from location 13, pin 20. Then, on the CDP18S102 module previously removed, cut Link LK1 so that when it is re-installed, no conflict results between the +5-volt supply and the +12-volt supply. The wiring need not be removed when the CPU Module CDP18S102 is re-installed.

CDP18S603

Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMAI-N
B	TPB-P	2	DMAO-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	−5V/−15V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12V/+15V
Y	+5V	21	+5V
Z	GND	22	GND

Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+5V
31	EF2-N	32	−5V/−15V
33	EF1-N	34	+12V/+15V

LK 36,—Serial Data In to external flag lines. Connect pins 7:10 for EF3 or pins 8:9 for EF4. If the CDS Terminal Interface Module CDP18S507 in location 14 is to be retained, do not use EF4 on this board. Otherwise, a conflict on EF4 is created.

LK 36—RNU to start ROM's at address 8000. If the RAM or ROM occupies memory address 0000 or if the ROM occupies memory address 8000 and is the monitor or utility program, install pins 6:11. Then, add a wire to the CDS II backplane from location 12 pin 12 to location 10 pin D. This connection provides for a memory starting address of 8000 after RESET, RUNU switches are pressed. This wire should be removed when the CPU Module CDP18S102 is re-installed.

LK 10, 11, and 22—Set up as previously described for the memory address desired, taking care that the CDS II memories are not assigned to overlap the assignment of the CDP18S603 Microboard Computer.

Parts List

C1, C2, C3=15μF, 20 V
C4=1.5 μF, 35 V

CR1, CR2, CR3, CR4=1N270

J1, J2=connector, right angle (mates with connector comprised of housing - AMP 1-86148-2, contact - AMP 86016-1, keying plug - AMP 87077-1, or equivalent)

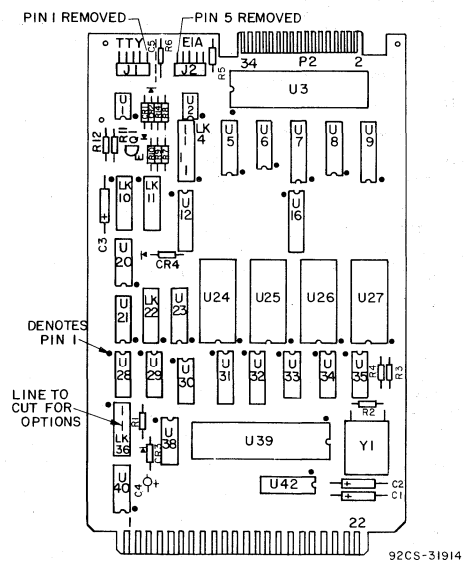
Q1=2N5139

R1=100 kΩ, ¼ W, 5%
R2=22 MΩ, ¼ W, 5%
R3, R4,=22 kΩ, ¼ W, 5%
R5=3 kΩ, ¼ W, 5%
R6, R14=1 kΩ, ¼ W, 5%
R7=11 kΩ, ¼ W, 5%
R8=4.3 kΩ, ¼ W 5%
R9=130 Ω, ¼ W, 5%
R10=10 kΩ, ¼ W, 5%
R11=2.7 kΩ, ¼ W, 5%
R12=220 Ω, ¼ W, 5%

U1=CA3160
U2=CA3140
U3=CDP1851CE
U5, U8=CDP1856CE
U6=CD4069BE
U7=CDP1867CE
U9=CDP1866CE
U12,U16=MWS5114E-5
U20, U38=resistor module, 22 kΩ, 14 pin
U21=CD4001BE
U23=CDP1858CE
U28, U29=CD4012BE
U30=CD4016BE
U31, U32=CD4050BE
U33=CD4025BE
U34=CD4013BE
U35=CD4023BE
U39=CDP1802CE
U40=CD4093BE
U42=resistor module, 22 kΩ, 16 pin

XU24-XU27=24-pin socket
XU39=40-pin socket

Y1=2.00-MHz crystal



Layout diagram of RCA COSMAC Microboard Computer CDP18S603.

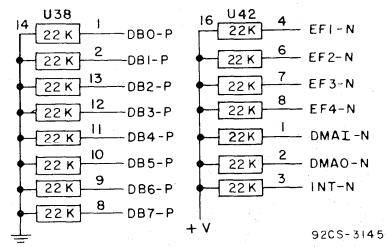
CDP18S603

Microboard Computer 20-mA Serial Interface (J1)

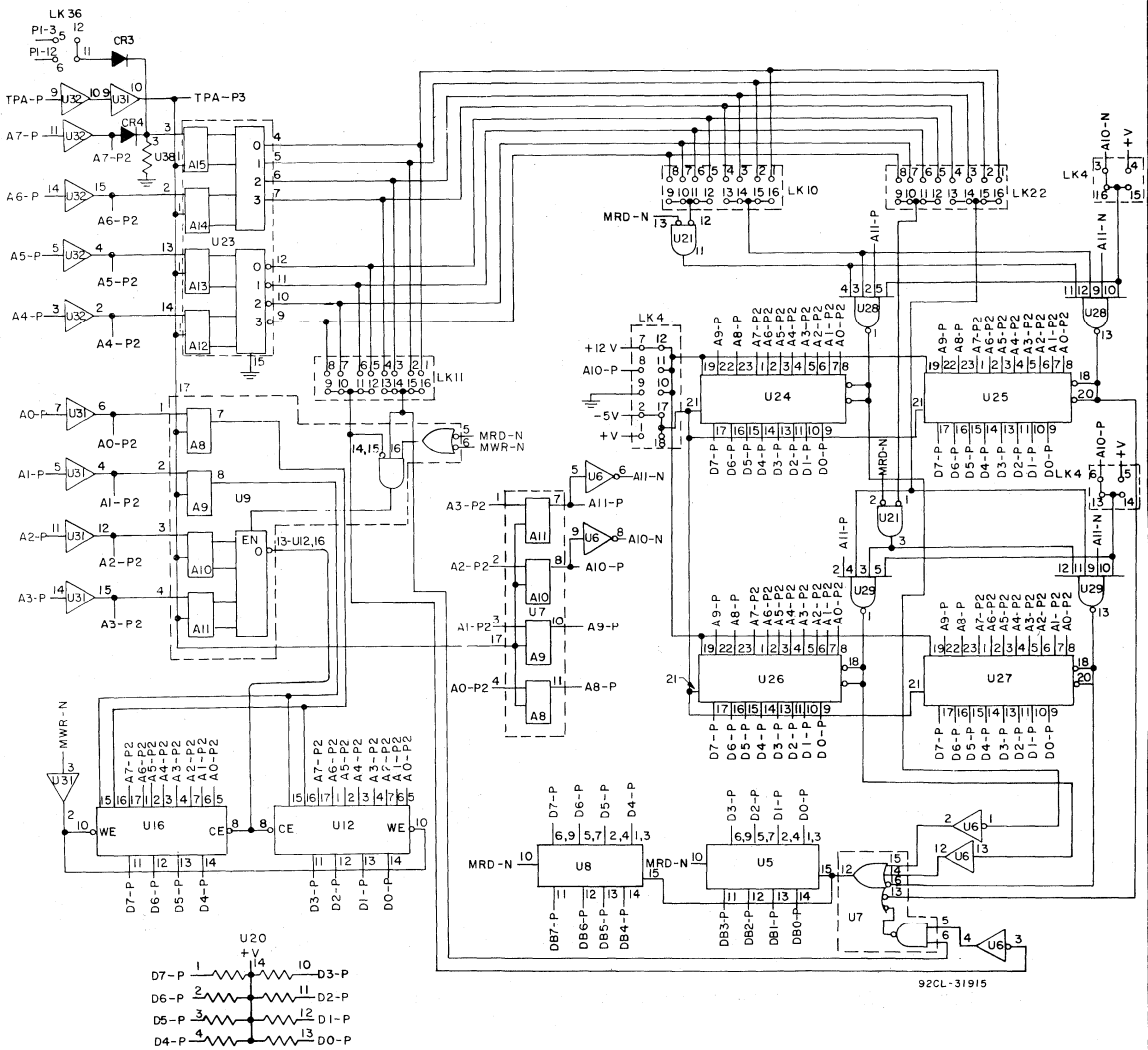
Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

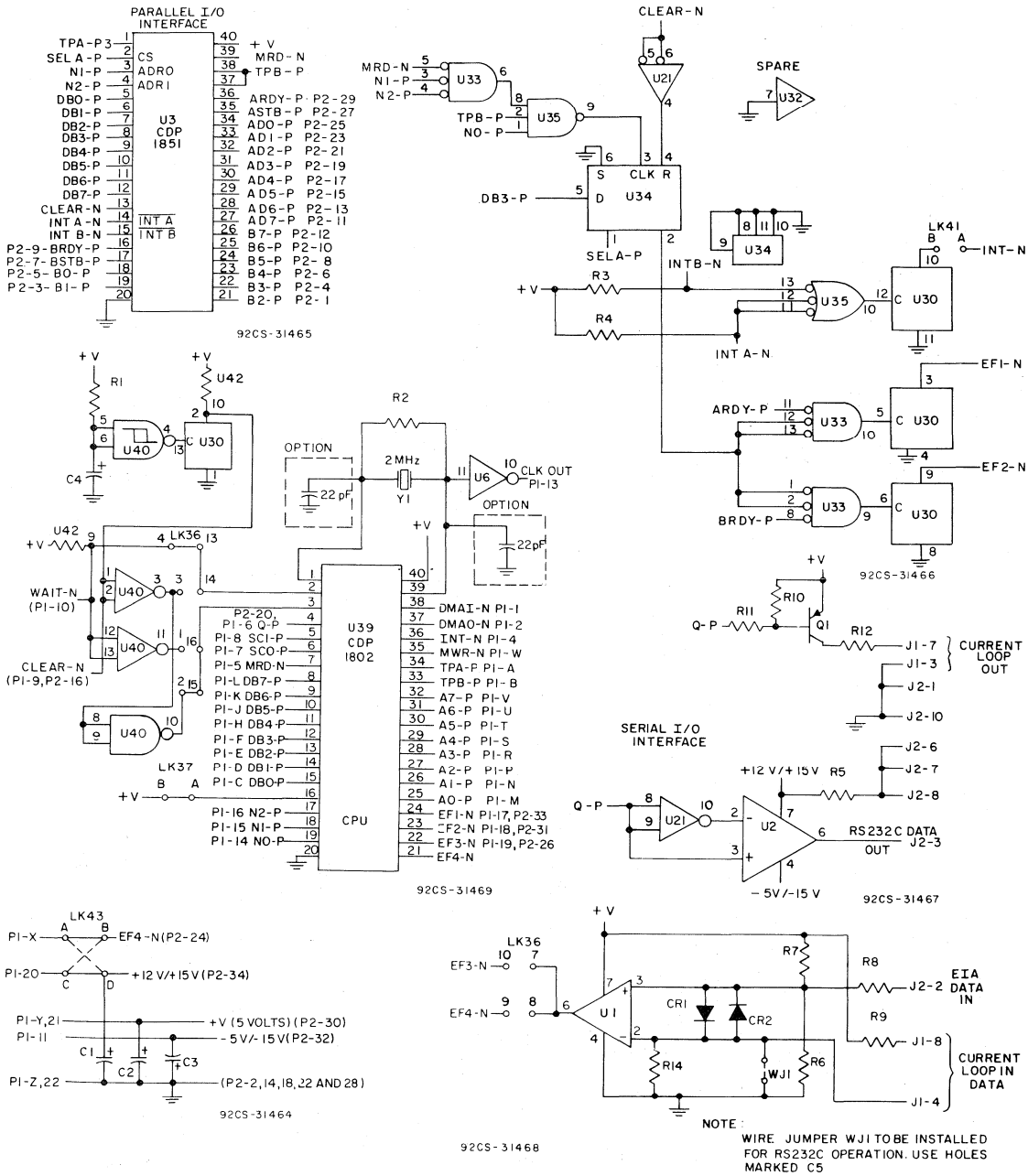


Pull-down and pull-up resistors.



Logic diagram of Microboard Computer CDP18S603—memory portions.

CDP18S603



Logic diagram of Microboard Computer CDP18S603—CPU and interface portions.

CDP18S620

RCA COSMAC Microboard 4-Kilobyte RAM

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 4-kilobyte block in the 64-kilobyte memory space. A four-rocker DIP switch is provided to set the binary value of the specific 4-kilobyte block to be occupied.

Specifications

Memory Capacity
4096 bytes (32 CMOS static RAM's 256 x 4).

Memory Addressing
Occupies any contiguous 4-kilobyte block on any 4-kilobyte boundary within the 64-kilobyte address space.
Switch-selectable block address.

Operating Temperature Range
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm).
Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
+5 volts at 4 milliamperes typical operating.

Connector
System interface: Edge fingers, 44 pins on 0.156-inch centers.

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- High noise immunity
- Flexible address assignment
- Fully buffered
- Simple system interface
- Temperature range - 0 °C to 70 °C
- Expandable by use of COSMAC Microboard Universal Backplane

Bus Interface Signals (Connector P1)

The RCA Microboard 4-Kilobyte RAM makes use of the following Microboard bus interface signals.

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

Bits 3 through 0 are latched in a CDP1858 4-bit Latch with Decode at TPA trailing edge. Bits 0 and 1 are decoded into four chip-enable lines called CE0-P through CE3-P. Bits 2 and 3 are decoded into four chip-enable lines called RE0-N

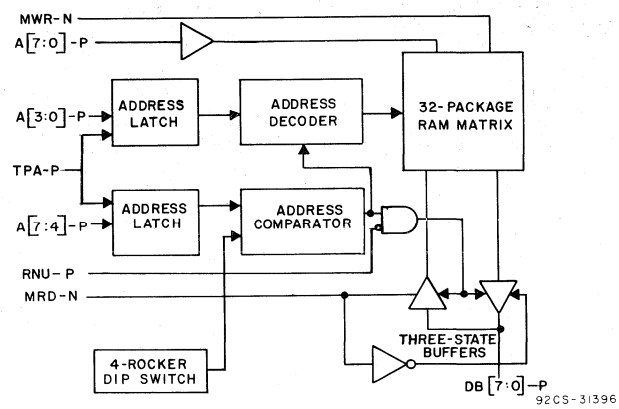


Fig. 1 - Block diagram of RCA COSMAC Microboard 4-Kilobyte RAM.

CDP18S620

through RE3-N. These eight lines are wired to CE2 and CE1, respectively, on the RAM chips in a matrix form, and any combination of bits 3 through 0 will uniquely select the proper two RAM chips.

Bits 7 through 4 are latched into a CDP1867 4-bit Latch on the TPA trailing edge. These bits are compared with the setting of the four DIP switch rockers. When they are equal, an enable is generated which enables the CDP1858 decoder for bits 3 through 0 mentioned above and the data bus three-state buffers.

DB7 through DB0 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the four high-address bits and the four DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted **to** the Microboard interface bus; when MRD is false, data bits are transmitted **from** the Microboard interface bus.

MRD - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the output control on each RAM chip.

MWR - Memory Write. This signal is buffered and wired to each RAM chip. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1858 and CDP1867 latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2, inhibits the board ENABLE signal, thereby eliminating memory access. The link need not be installed if not required. Its purpose is to inhibit the board when its address is **0000** (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal
A	TPA-P	*	1	DMAI-N
B	TPB-P		2	DMAO-N
C	DB0-P	*	3	RNU-P *
D	DB1-P	*	4	INT-N
E	DB2-P	*	5	MRD-N *
F	DB3-P	*	6	Q-P
H	DB4-P	*	7	SC0-P
J	DB5-P	*	8	SC1-P
K	DB6-P	*	9	CLEAR-N
L	DB7-P	*	10	WAIT-N
M	A0-P	*	11	−5 V/−15 V
N	A1-P	*	12	SPARE
P	A2-P	*	13	CLOCK OUT
R	A3-P	*	14	N0-P
S	A4-P	*	15	N1-P
T	A5-P	*	16	N2-P
U	A6-P	*	17	EF1-N
V	A7-P	*	18	EF2-N
W	MWR-N*		19	EF3-N
X	EF4-N		20	+12 V/+15 V
Y	+5 V	*	21	+5 V *
Z	GND	*	22	GND *

*Signals used on RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Installation in a Microboard System

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required unless the system has a RUN UTILITY switch and the DIP switch rockers are all open, in which case link LK2 pins A and B should be shorted.

The desired high-order four address bits should be set in the four-rocker DIP switch (UA9). The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

Installation in the COSMAC Development System CDP18S005

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in the CDS II in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the desired 4-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect A and B of link LK1.

For the RNU signal, connect A and B of link LK2, if the board is to reside at address 0000. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 4-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Link LK1 must be arranged as follows:

A to B - SHORTED
C to D - OPEN (Cut preprinted LINK)
E to F - SHORTED

When the CDP18S620 is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be inactive only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 4-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Physical Address Map

The physical address map given in Table II may be used to identify the board location of a memory device as a function of its address. Because the device organization is 256 x 4, two devices are involved with any byte of data. Table II provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte.

Table II - Physical Address Map of 32-Package RAM Matrix

Hex Address	Memory Location: High Half-Byte	Memory Location: Low Half-Byte
X0XX	UD1	UE1
X1XX	UD2	UE2
X2XX	UD3	UE3
X3XX	UD4	UE4
X4XX	UD5	UE5
X5XX	UD6	UE6
X6XX	UD7	UE7
X7XX	UD8	UE8
X8XX	UB1	UC1
X9XX	UB2	UC2
XAXX	UB3	UC3
XBXX	UB4	UC4
XCXX	UB5	UC5
XDXX	UB6	UC6
XEXX	UB7	UC7
XFXX	UB8	UC8

X = DON'T CARE, except that the most significant hex digit matches the DIP switch setting. If it does not, the board is not being addressed.

CDP18S620

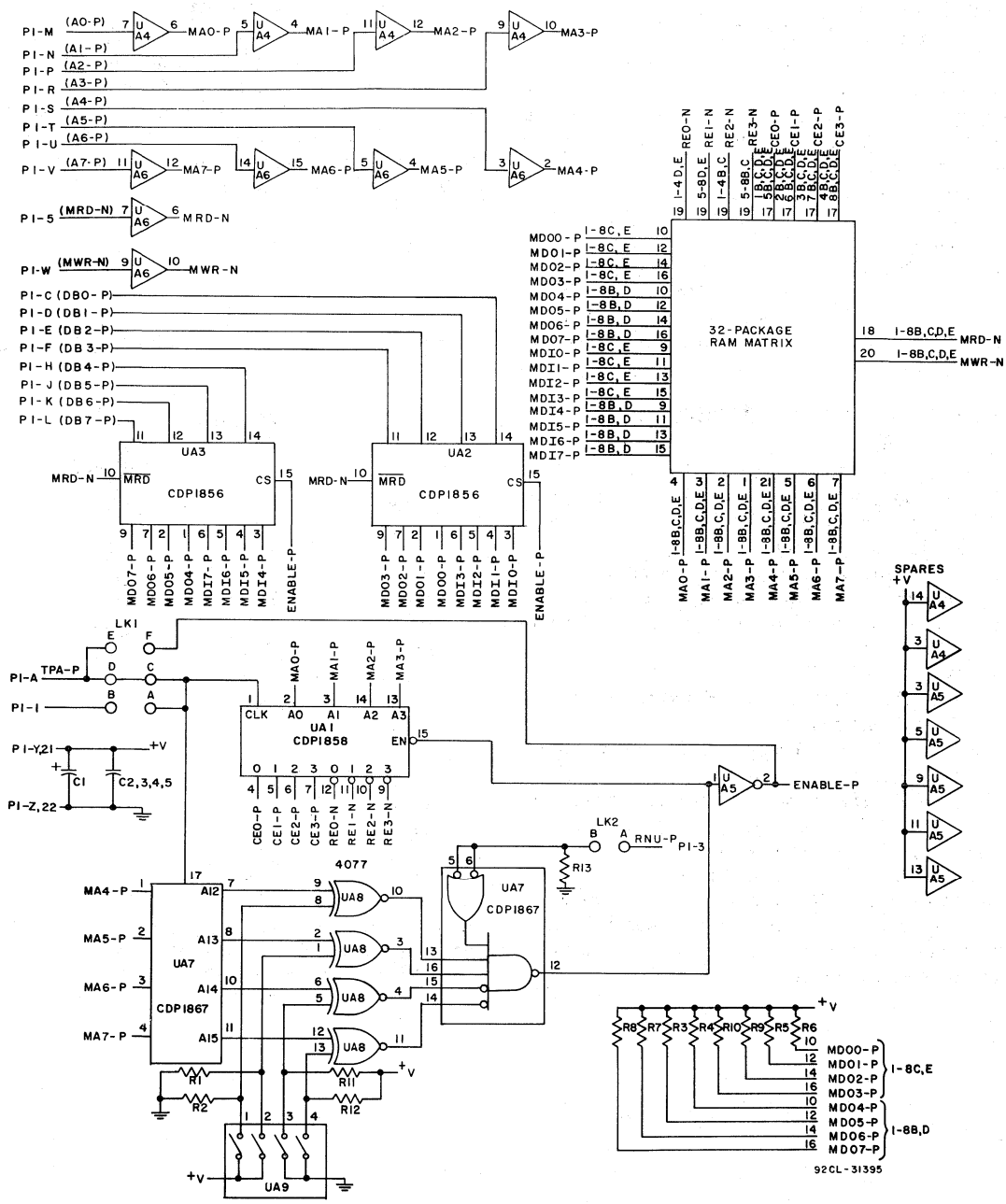


Fig. 2 - Logic diagram for RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

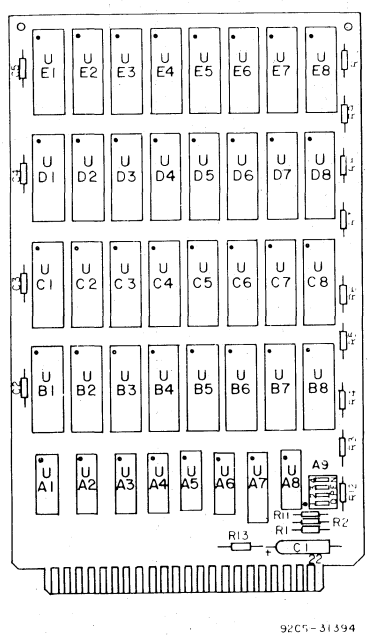
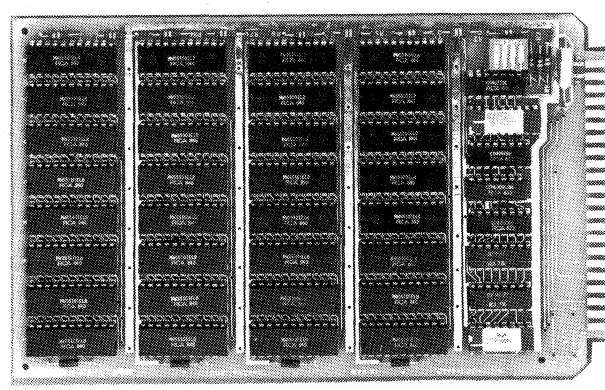


Fig. 3 - Layout diagram of RCA COSMAC Microboard 4-Kilobyte RAM CDP18S620.

Parts List

C1 = 15 μF, 20 V
C2 – C5 = 0.1 μF, 50 V
R1 – R13 = 22 kilohms, 0.25 W
UA1 = CDP1858CE
UA2, UA3 = CDP1856CE
UA4, UA6 = CD4050BE
UA5 = CD4069BE
UA7 = CDP1867CE
UA8 = CD4077BE
UA9 = 4-rocker DIP switch
UB1-UB8, UC1-UC8, UD1-UD8, UE1-UE8 } CDP1822E or MWS5101EL-3



CDP18S621
RCA COSMAC Microboard 16-Kilobyte RAM

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 16-kilobyte block in the 64-kilobyte memory space. A two-rocker DIP switch is provided to set the binary value of the specific 16-kilobyte block to be occupied.

Specifications

Memory Capacity
16192 bytes (32 CMOS static RAM's 1048 x 4; MWS5114)

Memory Addressing
Occupies any contiguous 16-kilobyte block on any 16-kilobyte boundary within the 64-kilobyte address space.
Switch-selectable block address.

Operating Temperature Range
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm).
Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
+5 volts at 6 milliamperes typical, operating at 2-MHz system clock.

Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- Fully buffered
- High noise immunity
- Flexible address assignment
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range - 0 °C to 70 °C

Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 16-Kilobyte RAM makes use of the following Microboard bus interface signals.

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

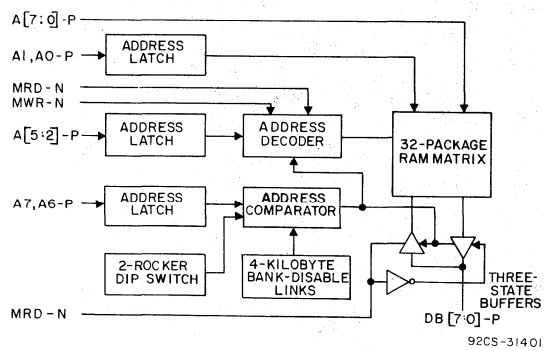


Fig. 1 - Block diagram of RCA COSMAC Microboard 16-Kilobyte RAM.

Bits 1 and 0 are latched in a CDP1866 (U1B) latch-decoder at TPA trailing edge. The output of these latches are wired to each memory chip, providing A9 and A8 for on-chip decoding.

Bits 3 and 2 are latched into four CDP1866 latch-decoders (U1B, U2B, U6B, U7B) in parallel, forming A11 and A10, and decoded into four sets of four chip-enable lines. These lines are wired to four 4-kilobyte blocks of memory chips as chip-enables.

Bits 5 and 4 are latched into a CDP1866 (U2B), forming A13 and A12, and are used to condition the four decoders so that only one 4-kilobyte block is addressed at any time.

Bits 7 and 6 are latched into a CDP1866 (U6B) forming A15 and A14. These bits are compared with the setting of the 2 DIP switch rockers. When there is a match, the four decoders and the data buffers are enabled.

DB7 through DB0 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the two high-address bits and the two DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted **to** the Microboard interface bus; when MRD is false, data bits are transmitted **from** the Microboard interface bus.

$\overline{\text{MRD}}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

$\overline{\text{MWR}}$ - Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866 latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2A, pins 4 and 13, inhibits the board ENABLE signal, thereby eliminating memory access. The link may be cut if not required. Its purpose is to inhibit the board when its address is 0000 (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal
A	TPA-P	*	1	DMAI-N
B	TPB-P		2	DMAO-N
C	DB0-P	*	3	RNU-P *
D	DB1-P	*	4	INT-N
E	DB2-P	*	5	MRD-N *
F	DB3-P	*	6	Q-P
H	DB4-P	*	7	SC0-P
J	DB5-P	*	8	SC1-P
K	DB6-P	*	9	CLEAR-N
L	DB7-P	*	10	WAIT-N
M	A0-P	*	11	−5 V/−15 V
N	A1-P	*	12	SPARE
P	A2-P	*	13	CLOCK OUT
R	A3-P	*	14	N0-P
S	A4-P	*	15	N1-P
T	A5-P	*	16	N2-P
U	A6-P	*	17	EF1-N
V	A7-P	*	18	EF2-N
W	MWR-N*		19	EF3-N
X	EF4-N		20	+12 V/+15 V
Y	+5 V	*	21	+5 V *
Z	GND	*	22	GND *

*Signals used on RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.

Installation in a Microboard System

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required.

The desired high-order two address bits should be set in the two-rocker DIP switch S1. The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

CDP18S621

Installation in the COSMAC Development System CDP18S005

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in the CDS II in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the 16-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect pins 1 and 16 of link LK2A.

For the RNU signal, a connection is preprinted between pins 3 and 13 of link LK2A. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 16-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Connect link LK2A as follows:

1 to 16 - SHORTED
2 to 15 - OPEN (Cut preprinted link)
3 to 14 - SHORTED

When the CDP18S621 is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 16-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Installation as a 4-, 8-, or 12-Kilobyte RAM

When required, the CDP18S621 may be configured as a 4-, 8-, or 12-kilobyte RAM. This expedient might be required when ROM is substituted for RAM in a developmental cycle. Any 4-kilobyte block may be disabled by the cutting of one link.

The disabling links for each 4-kilobyte block of memory, as defined in the physical address map given in Table II, are as follows

Memory Block To Be Disabled	Pins of Link LK2A To Be Cut
First 4 kilobytes	5 to 12
Second 4 kilobytes	6 to 11
Third 4 kilobytes	7 to 10
Fourth 4 kilobytes	8 to 9

The result of cutting one or more of these links is the creation of 4-kilobyte holes in the 16-kilobyte space normally occupied by the board. Other memories may then occupy these holes without conflict.

Physical Address Map

The physical address map given in Table II may be used to identify the board location of a memory device as a function of its address. Because the device organization is 1024 x 4, two devices are involved with any byte of data. Table II provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte.

Table II - Physical Address Map of 32-Package RAM Matrix

Binary Value of High Address Byte		Memory Location High Half-Byte	Memory Location Low Half-Byte
XX00	00XX	U2E	U2C
XX00	01XX	U2F	U2D
XX00	10XX	U1E	U1C
XX00	11XX	U1F	U1D
XX01	00XX	U4E	U4C
XX01	01XX	U4F	U4D
XX01	10XX	U3E	U3C
XX01	11XX	U3F	U3D
XX10	00XX	U6E	U6C
XX10	01XX	U6F	U6D
XX10	10XX	U5E	U5C
XX10	11XX	U5F	U5D
XX11	00XX	U8E	U8C
XX11	01XX	U8F	U8D
XX11	10XX	U7E	U7C
XX11	11XX	U7F	U7D

X = DON'T CARE, except that the two most significant bits match the DIP switch setting. If they do not, the board is not being addressed.

CDP18S621

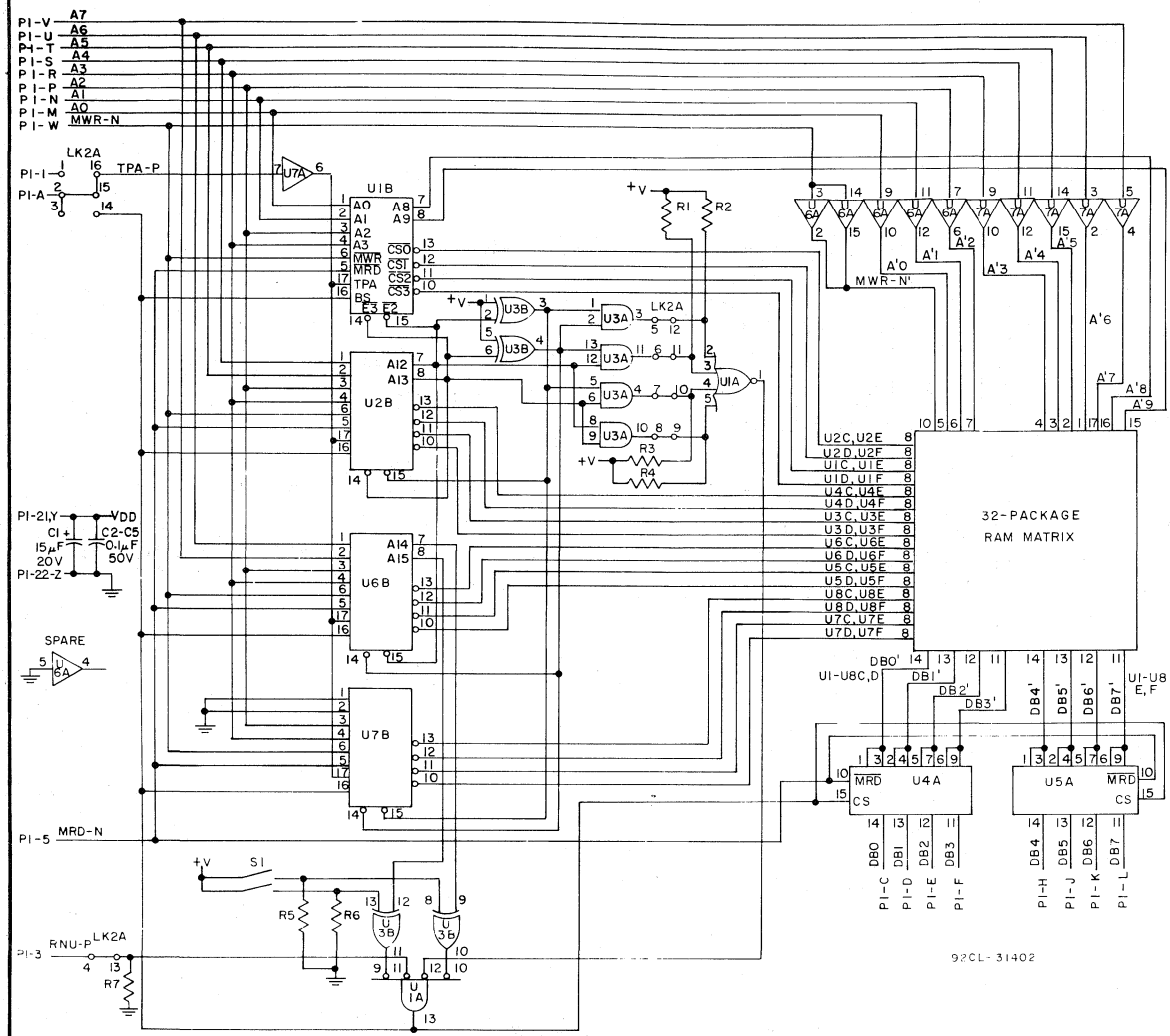
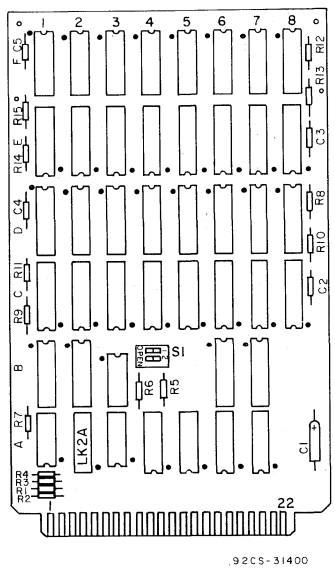


Fig. 2 - Logic diagram for RCA COSMAC Microboard 16-kilobyte RAM CDP18S621.

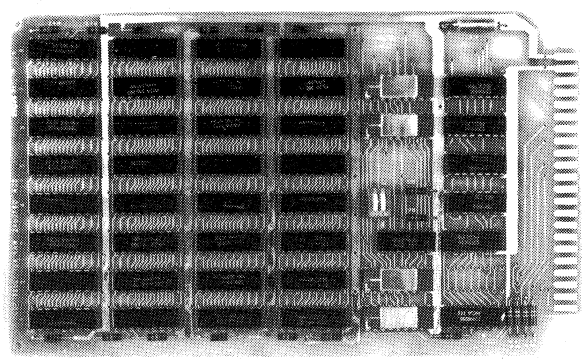
CDP18S621



Parts List

C1 = 15 μF, 20 V
C2 – C5 = 0.1 μF, 50 V
R1 – R15 = 22 kilohms, ¼ W
S1 = 2-rocker DIP switch
U1A = CD4002BE
U3A = CD4081BE
U4A, U5A = CDP1856CE
U6A, U7A = CD4050BE
U1B, U2B, U6B, U7B = CDP1866CE
U3B = CD4070BE
U1C – U8C, U1D – U8D, U1E – U8E, U1F – U8F = MWS5114E-5

Fig. 3 - Layout diagram of RCA COSMAC Microboard 16-Kilobyte RAM CDP18S621.



CDP18S622

Advance Data

RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 is a static read-write memory module with on-board address latches and decoders. The address and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any two even 4-kilobyte blocks within the 64-kilobyte memory space. Two sets of links (LK19 and LK20) are provided for address assignment of both 4-kilobyte blocks. Three 180-mAh nickel-cadmium batteries provide backup power for data retention when system power is down. The board is also prewired for use with an optional regulated power supply.

Specifications

Memory Capacity
8192 bytes (16 CMOS MWS5114 static RAM's 1024 x 4)

Memory Addressing
Occupies any two 4-kilobyte blocks on 4-kilobyte boundaries within the 64-kilobyte address space. Link-programmable block addressing.

Operating-Temperature Range
0°C to 70°C

Power Requirements - Standby

Without batteries:	+5 V at 600 μA, typ.
With batteries 10% charged:	+5 V at 145 mA, typ.
With batteries 90% charged:	+5 V at 4.5 mA, typ.
With optional 4th battery:	+6.5 V dc ± 5% at 500 mA, max.

(powers complete Microboard computer system)

Optional Power Supply - Regulated
Input: 8 to 20 V dc or 12.6 V ac at 1.5 A, max. (diode bridge installed)
Output: Regulated - 4.92 to 5.62 V dc at 500 mA

Battery Supply
3 batteries: 3.6 to 4.35 V at 90 mAh
4 batteries: 4.8 to 5.8 V at 90 mAh

Connector
System interface: Edge fingers, 44 pins on 0.156-inch centers

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Data Retention
With 3 batteries, fully charged: 96 hours, min.

Features:

- Low-power static CMOS (600 μA typ. battery drain)
- Small board size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Fits Micromonitor (CDP18S030) memory expansion connector
- High noise immunity (1.5 V typ.)
- Flexible address assignment
- Fully buffered
- Power supply option for ac operation
- Battery-backup memory (96-hr. data retention)
- 0 to 70°C operating-temperature range
- 44-pin system interface
- Integral battery option can power entire computer system
- Expandable by use of COSMAC Microboard Universal Backplane

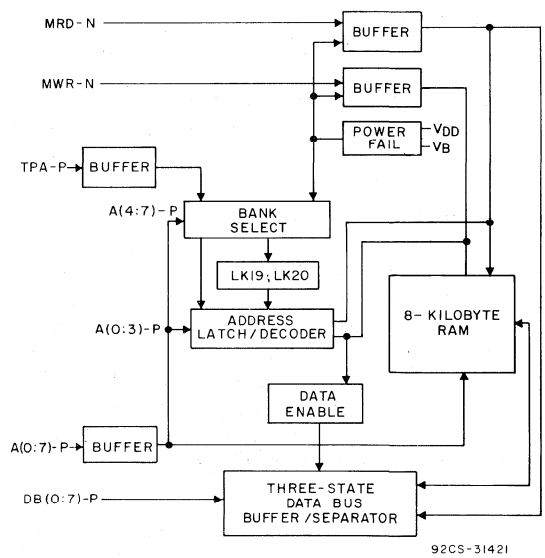


Fig. 1 - RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 block diagram.

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Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM makes use of the following Microboard bus interface signals.

A0 through A7 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM and address decoder. The address decoders latch the high-address byte on the trailing edge of TPA. The low-address byte becomes stable after TPA.
Address Bits A0 and A1 are latched into a CDP1866 (U23) at the trail-edge of TPA and generate output Address Bits A8 and A9.
Address Bits A2 and A3 are latched into two CDP1866's (U23 and U21). Each of these latches generate four chip-enable lines designated CS1-N through CS4-N for the lower 4-kilobyte RAM block and CS5-N through CS8-N for the upper 4-kilobyte RAM block, respectively. Each enable line is then wired to the appropriate MWS5114 RAM (1024 x 4). The selection of which set of enable signals is active is accomplished by Address Bits A4 through A7.
Address Bits A4 through A7 are latched into a CDP1858 (U18) latch at TPA trailing edge. Bits A4 and A5 are decoded into four active high signals. Bits A6 and A7 are decoded into four active low signals. These eight lines are wired to links LK19 and LK20 that control the location in memory space of each 4-kilobyte block of RAM. Links LK19 and LK20 are prewired so that the board occupies 8 kilobytes at address locations 1000_{16} through $2FFF_{16}$.

DB0 through DB7 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators (U26 and U27). These devices are in a high-impedance state in both directions until an enable is generated by an OR function of CS1-N through CS8-N. The direction is determined by the READ-N signal. When READ-N is true, data bits are transmitted to the Microboard interface bus; when READ-N is false, data bits are transmitted from the Microboard bus.

$\overline{\text{MRD}}$ - **Memory Read.** When true, MRD indicates that data will be read from memory. This signal is buffered and gated with PE-N (Power Enable) generating a signal READ-N. READ-N conditions the data bus interface buffers, the chip-enable (CS1-N through CS8-N) decoders, and the output control on each RAM.

$\overline{\text{MWR}}$ - **Memory Write**. When true, MWR dictates a write command. This signal is buffered and gated with PE-N (Power Enable) generating a signal WE-N. This signal enables the chip-enable decoders and conditions all the RAM's into the WRITE mode.

TPA - **Timing Pulse A**. This signal is buffered and used to latch the high-order address bits into the CDP1858 and CDP1866 latches. Latching takes place at the TPA trailing edge.
- **Power Enable**. The signal PE-N is generated by the CA3078 Micropower Operational Amplifier. The supply voltage for the amplifier is obtained directly from the battery supply, thus enabling proper operation without the application of external power. The battery voltage V_B and the external supply voltage V_{DD} are both sampled through a voltage divider network to the inputs of the CA3078. If a power failure is sensed, the PE-N signal is generated into the off state (high), thus isolating the data bus, chip select, memory write, and memory read functions from the Microboard interface bus.
Power-On Reset. The signal POR is available, if required by the user, through link LK3 A and B to pin 17 on the Microboard Interface Connector (P1). After power up (V_{DD} on), the signal will momentarily remain high and then stabilize to a low state. The RC integrator (R1 and C4) and the Schmitt trigger (U3) provide the signal approximately 150 milliseconds after power turn on. Systems using the data retention feature must use a POR to avoid random-memory access at power-on time. Microboard computer modules also provide a POR, generating CLEAR-N at P1-9. Link LK3 A and B should not be used in a Microboard system, only in other applications.

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RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Microboard Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622.

Table I - Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal
A	TPA-P	*	1	DMAI-N
B	TPB-P		2	DMAO-N
C	DB0-P	*	3	RNU-P *
D	DB1-P	*	4	INT-N
E	DB2-P	*	5	MRD-N *
F	DB3-P	*	6	Q-P
H	DB4-P	*	7	SC0-P
J	DB5-P	*	8	SC1-P
K	DB6-P	*	9	CLEAR-N
L	DB7-P	*	10	WAIT-N
M	A0-P	*	11	−5 V/−15 V
N	A1-P	*	12	SPARE
P	A2-P	*	13	CLOCK OUT
R	A3-P	*	14	N0-P
S	A4-P	*	15	N1-P
T	A5-P	*	16	N2-P
U	A6-P	*	17	EF1-N†
V	A7-P	*	18	EF2-N
W	MWR-N	*	19	EF3-N
X	EF4-N		20	+12 V/+15 V
Y	+5 V	*	21	+5 V *
Z	GND	*	22	GND *

*Signals used on RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622.
†Power reset option.

Installation in a Microboard System

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required unless the user wishes to change the location of the 8 kilobytes of RAM in memory space. The board is prewired for address locations 1000_{16} to $2FFF_{16}$. Table II gives the link modifications for different memory space allocations for each 4-kilobyte block of RAM.

Table II - Link Connections for 4-Kilobyte Blocks of RAM

4-Kilobyte Block Address (hex)	Link Connections LK19 (Lower 4 Kilobytes)	LK20 (Higher 4 Kilobytes)
0000 - 0FFF	1 to 16 and 5 to 12	1 to 16 and 5 to 12
1000 - 1FFF	2 to 15 and 5 to 12	2 to 15 and 5 to 12
2000 - 2FFF	3 to 14 and 5 to 12	3 to 14 and 5 to 12
3000 - 3FFF	4 to 13 and 5 to 12	4 to 13 and 5 to 12
4000 - 4FFF	1 to 16 and 6 to 11	1 to 16 and 6 to 11
5000 - 5FFF	2 to 15 and 6 to 11	2 to 15 and 6 to 11
6000 - 6FFF	3 to 14 and 6 to 11	3 to 14 and 6 to 11
7000 - 7FFF	4 to 13 and 6 to 11	4 to 13 and 6 to 11
8000 - 8FFF	1 to 16 and 7 to 10	1 to 16 and 7 to 10
9000 - 9FFF	2 to 15 and 7 to 10	2 to 15 and 7 to 10
A000 - AFFF	3 to 14 and 7 to 10	3 to 14 and 7 to 10
B000 - BFFF	4 to 13 and 7 to 10	4 to 13 and 7 to 10
C000 - CFFF	1 to 16 and 8 to 9	1 to 16 and 8 to 9
D000 - DFFF	2 to 15 and 8 to 9	2 to 15 and 8 to 9
E000 - EFFF	3 to 14 and 8 to 9	3 to 14 and 8 to 9
F000 - FFFF	4 to 13 and 8 to 9	4 to 13 and 8 to 9

Installation in the COSMAC Development System CDP18S005 (CDS II)

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in the CDS II in any memory slot 1 through 8. Bank Select wiring is not required on the backplane. If the address location of the two 4-kilobyte blocks of RAM is to be changed, refer to Table II for the link connections. Additional changes are required for the TPA, RNU, and POR (clear) signals to assure proper operation of the CDS II.

For the TPA signal, on LK4 of the CDP18S622 disconnect B and C, and connect A and B.

For the RNU signal, if the CDP18S622 is to reside at address 0000_{16}, pin 3 of any memory slot 1 through 9 of the CDS II should be wired to pin D of slot location 10 of the CDS II. This signal, RNU-P, starts utility software at location 8000_{16}. Its function on the CDP18S622 is to inhibit response while the utility program is being initiated.

For the POR signal, add a jumper between A and B of LK3 on the CDP18S622. This connection will provide the necessary clear signal to the CPU after power is applied to the CDS II. This signal must be provided so

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that the CPU will not inadvertently power up in the write mode and cause invalid data to be written to a programmed CDP18S622.

Installation in the Micromonitor CDP18S030

The RCA COSMAC 8-Kilobyte Battery-Backup RAM CDP18S622 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. For proper operation, LK4 must be modified to provide an "External Memory Deselect-N" signal for the Micromonitor. To make this modification, disconnect B and C on LK4 and connect C to D and A to B.

The memory address of the CDP18S622 can be located in any two 4-kilobyte blocks in the 64-kilobyte memory space other than the two standard locations (1000_{16} to $1FFF_{16}$ and 2000_{16} to $2FFF_{16}$).

The memory-disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set by links LK19 and LK20, even though the EXM bit is true. This arrangement allows for the substitution of two 4-kilobyte blocks of user memory within the 64-kilobyte memory space and enables the remainder of user memory space to operate normally.

Optional Power Supply

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 can be operated from a 12.6-volt ac power source by means of the regulated power supply option. The CDP18S622 printed-circuit board is prewired to accept the optional power-supply components listed in Table III. The power supply, a full-wave bridge rectifier with capacitive input filtering, delivers 17.8 volts dc at no load into a three-terminal positive-voltage regulator. The 5.26-volt dc output from the regulator (V_{REG}) is connected to link LK2.

To install the components listed in Table III, the user should refer to the Microboard layout diagram and the logic diagrams. The 12.6 volts (1 ampere) ac is applied to J1 and J2. The connections for link LK2 are given in Table IV for the four power-supply options.

Battery-Backup Memory Function

The RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 is supplied with three 180-mAh nickel-cadmium batteries capable of providing power to the control logic and RAM's during system power failures or other normal power-down situations. For operation of the CDP18S622 under battery power, the batteries must be charged for a period of 24 hours prior to use. With fully charged batteries, the data-retention capability is 96 hours under battery power. To disable the battery-backup feature of the CDP18S622, set switch S1 to the off position. This switch disconnects the battery voltage ground connection.

Optional Four-Battery Configuration

As shown in the layout diagram, the CDP18S622 provides for the addition of a fourth battery. With the additional battery, backup and operating power is available for the complete Microboard system. This feature

Table III - Components Required for Optional Regulated Power Supply

Component	Type	Quantity	Location	Suggested Supplier and Part No.
Capacitor	220 μF, 20 V dc	2	C2, C3	Sprague 137D227C7020F2
Diode	1N4001	4	CR6, CR7 CR8, CR9	RCA D1201F
Diode	1N270	1	CR5	—
Regulator	5 V, 3 pin	1	VR1	Fairchild 7805
Heat sink	—	1	H1	Aavid Eng. 5063B or Thermalloy 6070B
Heat sink compound	as required			
Hardware	screw #6-32, lock washer #6, hex nut #6-32			

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RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

Table IV - Connections for Link LK2

Function	Link Connections	
	Remove	Add
A. Power Microboard RAM CDP18S622 only from regulated supply - battery backup for Microboard RAM only	V_{DD} to V_{CC}	V_{REG} to V_{CC}
B. Power entire Microboard system from regulated supply - battery backup for entire system	V_{DD} to V_{CC}	V_{REG} to V_{CC} and V_{DD} to V_B
C. Power entire Microboard system from regulated supply - battery backup for Microboard RAM only	none	V_{REG} to V_{CC}
D. Power Microboard RAM from system V_{DD} - battery backup for entire system	V_{DD} to V_{CC}	V_{DD} to V_B

assures proper Microboard system operation during power supply failures.

To operate a Microboard Computer System with the battery-backup feature, the following steps must be taken. First, check that all devices in the system can be operated at 6.1 volts dc, the normal operating voltage for the system. Then,

1. Remove link V_{DD} to V_{CC} from LK2.
2. Remove link A to B on LK1.
3. Remove system V_{DD} from Microboard Chassis backplane. (V_{DD} will not be used).
4. Install link from V_{DD} to V_B on LK2.
5. Install link from B to C on LK1.
6. Install 180-mAh AAA nickel-cadmium battery in location B4 (Caution: Be sure to observe correct polarity).
7. Connect an external 6.5-volt dc supply to V_{CC} on LK2. (Provides system V_{DD}.)

Physical Address Map (Unmodified Board)

The physical address map given in Table V may be used to identify the location of any memory. Note that the map is valid only if LK19 and LK20 are not changed by the user from the original configuration.

Table V - Physical Address Map for Unmodified RCA COSMAC Microboard RAM CDP18S622

	Memory Location (Lower 4-kilobyte block - LK19)	
Hex Address	High Half-Byte	Low Half-Byte
1000 - 13FF	U16	U8
1400 - 17FF	U15	U7
1800 - 1BFF	U14	U6
1C00 - 1FFF	U13	U5
	Memory Location (Higher 4-kilobyte block - LK20)	
Hex Address	**High Half-Byte**	**Low Half-Byte**
2000 - 23FF	U12	U4
2400 - 27FF	U11	U3
2800 - 2BFF	U10	U2
2C00 - 2FFF	U9	U1

CDP18S622 Physical Address Map (LK19 and LK20 Modified)

Link LK19 controls the lower 4-kilobyte block of memory. The address map for LK19, regardless of which 4-kilobyte block is occupied, is given in Table VI.

Link LK20 controls the higher 4-kilobyte block of memory. The address map for LK20, regardless of which 4-kilobyte block is occupied, is given in Table VII.

Applications

The type of application for the CDP18S622 in which the battery-backup feature is used to advantage includes the transfer of software from the RCA COSMAC Development System CDP18S005 (CDS II) to a Microboard Computer System. In such an application, no additional hardware or software is required. The step-by-step procedure follows.

1. Remove any CDS II Memory Modules located in memory space 0000_{16} to $1FFF_{16}$ Bank 0 and 1).
2. Install the Microboard 8-Kilobyte Battery-Backup RAM CDP18S622 into any CDS II memory slot. Note that the CDP18S622 must be configured to occupy memory space 0000_{16} to $1FFF_{16}$ (see Table II) and S1 must be in the ON position.
3. Add a jumper to the CDS II backplane from pin 1 to pin A of the slot occupied by the CDP18S622.
4. Load the CDS II memory in its normal manner (i.e., from disk or magnetic tape).
5. Turn the power to the CDS II off.
6. Remove the CDP18S622 Microboard RAM from the CDS II and install it into the chassis of the Microboard Computer System.
7. Turn on the power of the Microboard Computer System and use it in its normal manner.

A second typical application of the CDP18S622 makes use of its data-retention capability. This capability is particularly useful for storing software in RAM over a week-end period so that a programming session can be continued without requiring a memory reload. This application requires only that the batteries have an adequate charge, as discussed earlier, and that Switch S1 be placed in the on position.

Table VI - Physical Address Map for LK19 as Modified

	Memory Location (Lower 4-kilobyte block - LK19)	
Hex Address*	**High Half-Byte**	**Low Half-Byte**
X000 - X3FF	U16	U8
X400 - X7FF	U15	U7
X800 - XBFF	U14	U6
XC00 - XFFF	U13	U5

*X denotes any one 4-kilobyte block ($X = 0_{16}$ to F_{16})

Table VII - Physical Address Map for LK20 as Modified

	Memory Location (Higher 4-kilobyte block - LK20)	
Hex Address*	**High Half-Byte**	**Low Half-Byte**
X000 - X3FF	U12	U4
X400 - X7FF	U11	U3
X800 - XBFF	U10	U2
XC00 - XFFF	U9	U1

*X denotes any one 4-kilobyte block ($X = 0_{16}$ to F_{16})

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RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

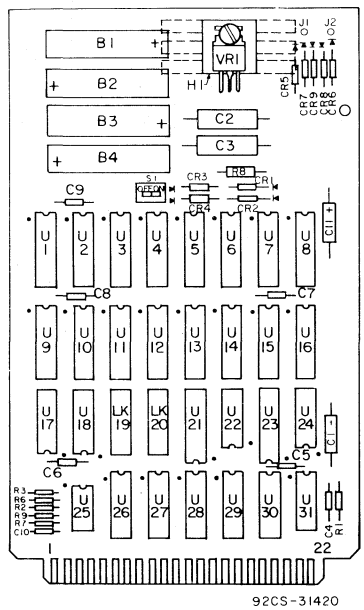
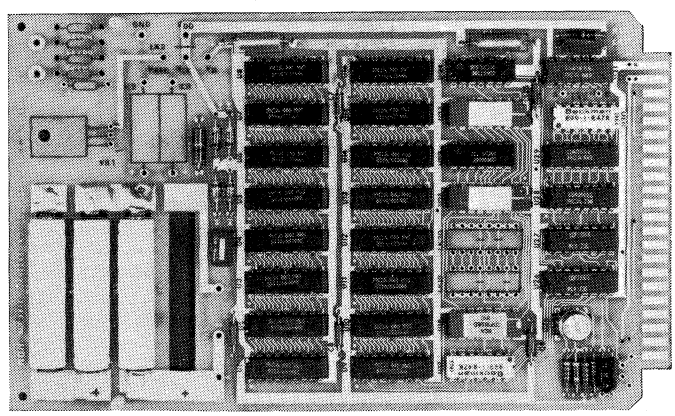


Fig. 2 - Layout diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622. B4, VR1, CR5 - CR9, C2 and C3 are optional items not installed on board.

Parts List

B1 – B3 = nickel-cadmium, 180 mAh, AAA
*B4 = nickel-cadmium, 180 mAh, AAA (Panasonic NR-AAA-U)
C1, C11 = 15 μF, 50 V
*C2, C3 = 220 μF, 20 V (Sprague 137D227C7020F2)
C4 = 0.33 μF, 50 V
C5 – C9 = 0.1 μF, 50 V
C10 = 22 pF
CR1 – CR4 = 1N270
*CR5 = 1N270
*CR6 – CR9 = 1N4001 (RCA D1201F)
*H1 = Heat sink (Thermalloy 6070B)
J1, J2 = terminal, optional 12.6 V ac
R1 = 100 kΩ, ¼ W, 5%
R2, R3 = 47 kΩ, ¼ W, 5%
R6 = 5.1 MΩ, ¼ W, 5%
R7 = 1.1 MΩ, ¼ W, 5%
R8 = 15 Ω, ½ W
R9 = 10.0 MΩ, ¼ W, 5%
S1 = 1-position DIP
U1 – U16 = CDP1825CE
U17, U30 = resistor module 22 kΩ, 16 pin
U18 = CDP1858CE
U21, U23 = CDP1866CE
U22 = CD4068BE
U24 = CD4071BE
U25 = CA3078S
U26, U27 = CDP1856CE
U28, U29 = CD4050BE
U31 = CD4093BE
*VR1 = 5-V voltage regulator (Fairchild 7805)

*User-supplied components for optional power supply.



CDP18S622

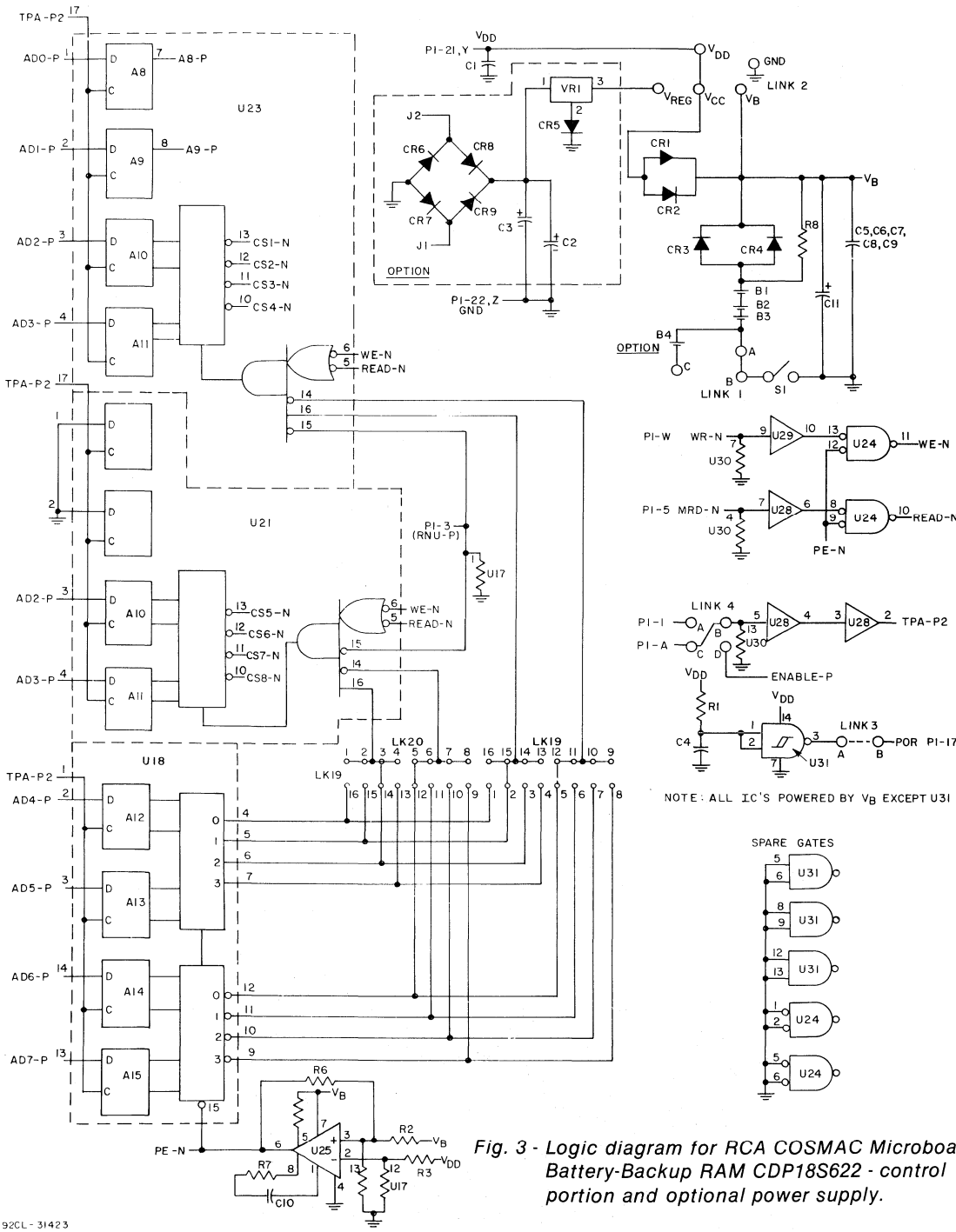


Fig. 3 - Logic diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622 - control portion and optional power supply.

92CL-31423

CDP18S622

RCA COSMAC Microboard 8-Kilobyte Battery-Backup RAM

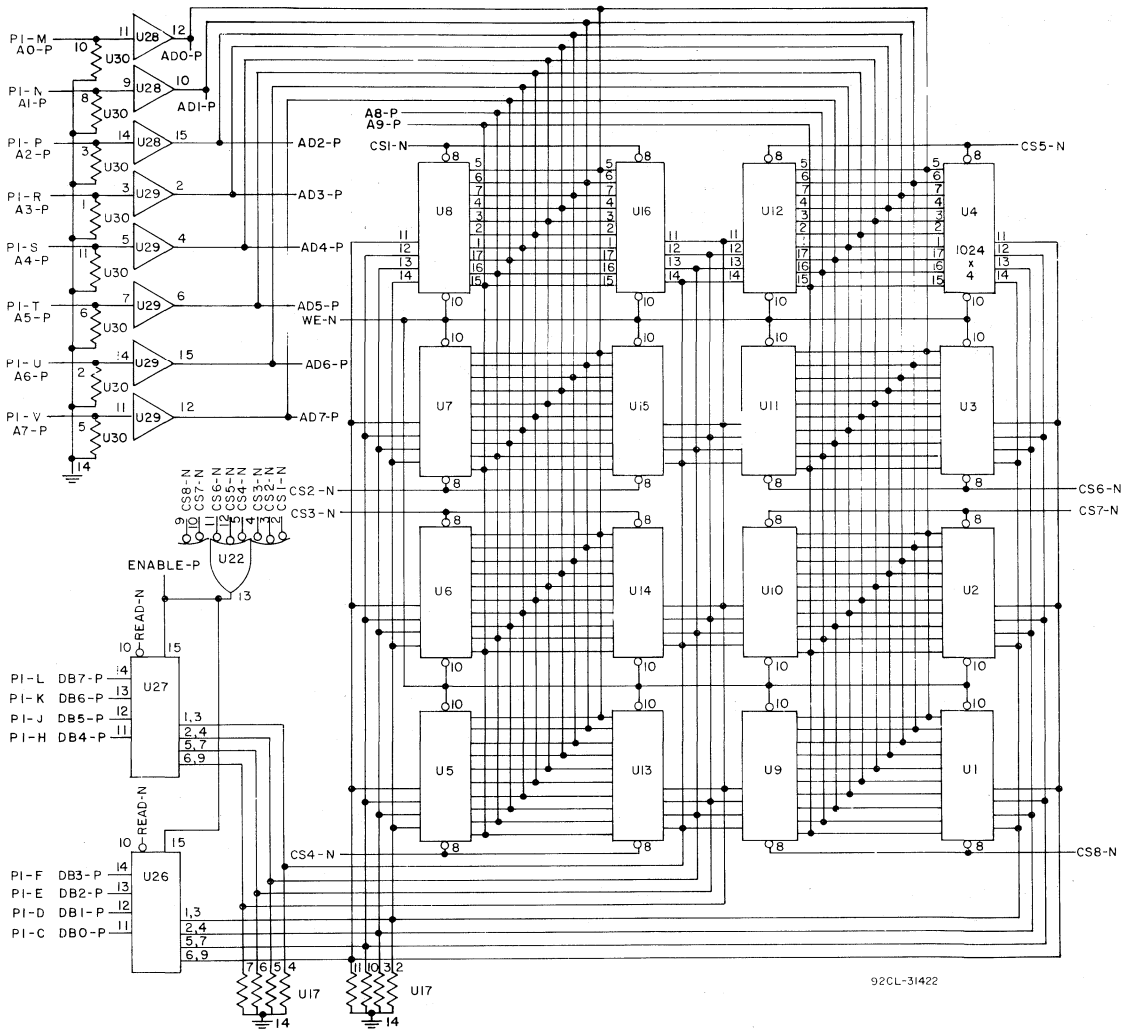


Fig. 4 - Logic diagram for RCA COSMAC Microboard Battery-Backup RAM CDP18S622 - memory and buffer portion.

CDP18S623
RCA COSMAC Microboard 8-Kilobyte RAM

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623 is a static read-write memory module having on-board address latches and decoders. Address lines and data lines are buffered to minimize loading of the Microboard bus interface. The memory occupies any even 8-kilobyte block in the 64-kilobyte memory space. A 3-rocker DIP switch is provided to set the binary value of the specific 8-kilobyte block to be occupied.

Specifications

Memory Capacity
8192 bytes (32 CMOS static RAM's 512 x 4)

Memory Addressing
Occupies any contiguous 8-kilobyte block on any 8-kilobyte boundary within the 64-kilobyte address space.
Switch-selectable block address.

Operating Temperature Range
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm).
Board pitch 0.5 inch (12.7 mm) minimum.

Power Requirements
+5 volts at 6 milliamperes typical, operating at 2-MHz system clock.

Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- Compatible with Micromonitor CDP18S030 expansion connector
- Fully buffered
- High noise immunity
- Flexible address assignment
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range - 0° C to 70° C

Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard 8-Kilobyte RAM makes use of the following Microboard bus interface signals.

A7 through A0 - Memory address bus on which the high- and low-address bytes are multiplexed. These signals are buffered and then wired to each RAM chip for the low-address byte, which becomes stable after TPA.

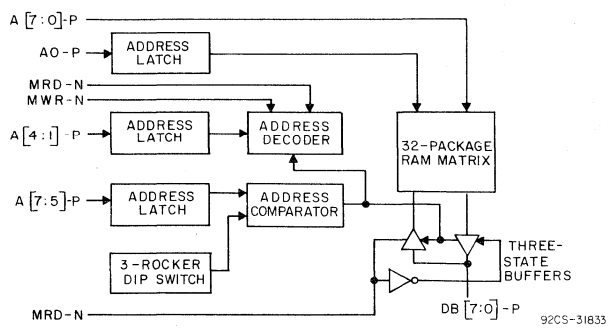


Fig. 1 - Block diagram of RCA COSMAC Microboard 8-Kilobyte RAM.

Bit D is latched in a CDP1866 (U1B) latch-decoder at TPA trailing edge. The output of this latch is wired to each memory chip, providing A8 for on-chip decoding.

Bits 1 and 2 are latched into four CDP1866 latch-decoders (U1B, U2B, U6B, U7B) in parallel, forming A9 and A10, and decoded into four sets of four chip-enable lines. These lines are wired to four 2-kilobyte blocks of memory chips as chip-enables.

Bits 3 and 4 are latched into a CDP1866 (U2B), forming A11 and A12, and are used to condition the four decoders so that only one 2-kilobyte block is addressed at any time.

Bits 5, 6, and 7 are latched into a CDP1866 (U6B; U1B) forming A13, A14, and A15. These bits are compared with the setting of the 3 DIP switch rockers. When there is a match, the four decoders and the data buffers are enabled.

DB7 through DB0 - These **Data Bus** lines are bidirectional and are interfaced through two CDP1856 4-bit Bus Buffer/Separators. These devices are in a high-impedance state in both directions until an enable is generated by a match between the 3 high-address bits and the 3 DIP switch rockers. The direction is determined by the MRD signal. When MRD is true, data bits are transmitted **to** the Microboard interface bus; when MRD is false, data bits are transmitted **from** the Microboard interface bus.

$\overline{\text{MRD}}$ - Memory Read. When true, MRD indicates that data will be read from memory. This signal is buffered. It conditions the data bus interface buffers and the chip-select decoders.

$\overline{\text{MWR}}$ - Memory Write. This signal is buffered. It conditions each RAM chip and the chip-select decoders. It is the write command.

TPA - Timing Pulse A. This signal is used to latch the high-order address bits into the CDP1866 latches. Latching takes place at the TPA trailing edge.

RNU - Run Utility. This signal, through link LK2A, pins 4 and 13, inhibits the board ENABLE signal, thereby eliminating memory access. The link may be cut if not required. Its purpose is to inhibit the board when its address is 0000 (DIP switches open) and a RUN UTILITY switch is causing the system to start at address 8000 instead of 0000.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623.

Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal
A	TPA-P	*	1	DMAI-N
B	TPB-P		2	DMAO-N
C	DB0-P	*	3	RNU-P *
D	DB1-P	*	4	INT-N
E	DB2-P	*	5	MRD-N *
F	DB3-P	*	6	Q-P
H	DB4-P	*	7	SC0-P
J	DB5-P	*	8	SC1-P
K	DB6-P	*	9	CLEAR-N
L	DB7-P	*	10	WAIT-N
M	A0-P	*	11	−5 V/−15 V
N	A1-P	*	12	SPARE
P	A2-P	*	13	CLOCK OUT
R	A3-P	*	14	N0-P
S	A4-P	*	15	N1-P
T	A5-P	*	16	N2-P
U	A6-P	*	17	EF1-N
V	A7-P	*	18	EF2-N
W	MWR-N*		19	EF3-N
X	EF4-N		20	+12 V/+15 V
Y	+5 V	*	21	+5 V *
Z	GND	*	22	GND *

*Signals used on RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623.

Installation in a Microboard System

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623 may be installed in any position in the five-card Microboard Chassis (CDP18S675) or in the 25-card Microboard Chassis (CDP18S670). No link changes are required.

The desired high-order two address bits should be set in the 3-rocker DIP switch S1. The least significant bit is rocker 1. The open position of the rocker generates a 0; the closed position generates a 1.

CDP18S623

Installation in the COSMAC Development System CDP18S005

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623 may be installed in the CDS II in any memory slot 1 through 8. No Bank Select wiring is required on the backplane. The binary address of the 8-kilobyte block should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1).

For the TPA signal, connect pins 1 and 16 of link LK2A.

For the RNU signal, a connection is preprinted between pins 3 and 13 of link LK2A. On the CDS II backplane, pin 3 of any memory slot 1 through 8 should be wired to pin D of slot location 10, which provides the RNU signal.

Installation in the Micromonitor CDP18S030

The RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623 may be installed in the external memory interface connector (P1) of the RCA COSMAC Micromonitor CDP18S030. The binary number of the desired 8-kilobyte block address should be set into the DIP switch (rocker 1 is the least significant bit; rocker open = 0; rocker closed = 1). Connect link LK2A as follows:

1 to 16 - SHORTED
2 to 15 - OPEN (Cut preprinted link)
3 to 14 - SHORTED

When the CDP18S623 is used in this manner, it will respond only to the block address set into the DIP switch rockers. The memory disable output from the Micromonitor CDP18S030 will be active only when the system under test generates a memory address that agrees with the value set into the DIP switch rockers even though the EXM bit is true. This arrangement allows for the substitution of a given 8-kilobyte block of user memory and enables the remainder of user memory space to operate normally.

Physical Address Map

The physical address map given in Table II may be used to identify the board location of a memory device as a function of its address. Because the device organization is 512 x 4, two devices are involved with any byte of data. Table II provides the two device locations for each address, one containing the high-order half byte and the other the low-order half byte. For example, if the hex address 8240 contains an error in the 2^2 bit, then the second line indicates that the device in question is in location U2D.

Table II - Physical Address Map of 32-Package RAM Matrix

	Memory Location	
Hex Address	High Half-Byte	Low Half-Byte
(0,2,4,6,8,A,C,E)(0-1)XX	U2E	U2C
(0,2,4,6,8,A,C,E)(2-3)XX	U2F	U2D
(0,2,4,6,8,A,C,E)(4-5)XX	U1E	U1C
(0,2,4,6,8,A,C,E)(6-7)XX	U1F	U1D
(0,2,4,6,8,A,C,E)(8-9)XX	U4E	U4C
(0,2,4,6,8,A,C,E)(A-B)XX	U4F	U4D
(0,2,4,6,8,A,C,E)(C-D)XX	U3E	U3C
(0,2,4,6,8,A,C,E)(E-F)XX	U3F	U3D
(1,3,5,7,9,B,D,F)(0-1)XX	U6E	U6C
(1,3,5,7,9,B,D,F)(2-3)XX	U6F	U6D
(1,3,5,7,9,B,D,F)(4-5)XX	U5E	U5C
(1,3,5,7,9,B,D,F)(6-7)XX	U5F	U5D
(1,3,5,7,9,B,D,F)(8-9)XX	U8E	U8C
(1,3,5,7,9,B,D,F)(A-B)XX	U8F	U8D
(1,3,5,7,9,B,D,F)(C-D)XX	U7E	U7C
(1,3,5,7,9,B,D,F)(E-F)XX	U7F	U7D

X = DON'T CARE

CDP18S623

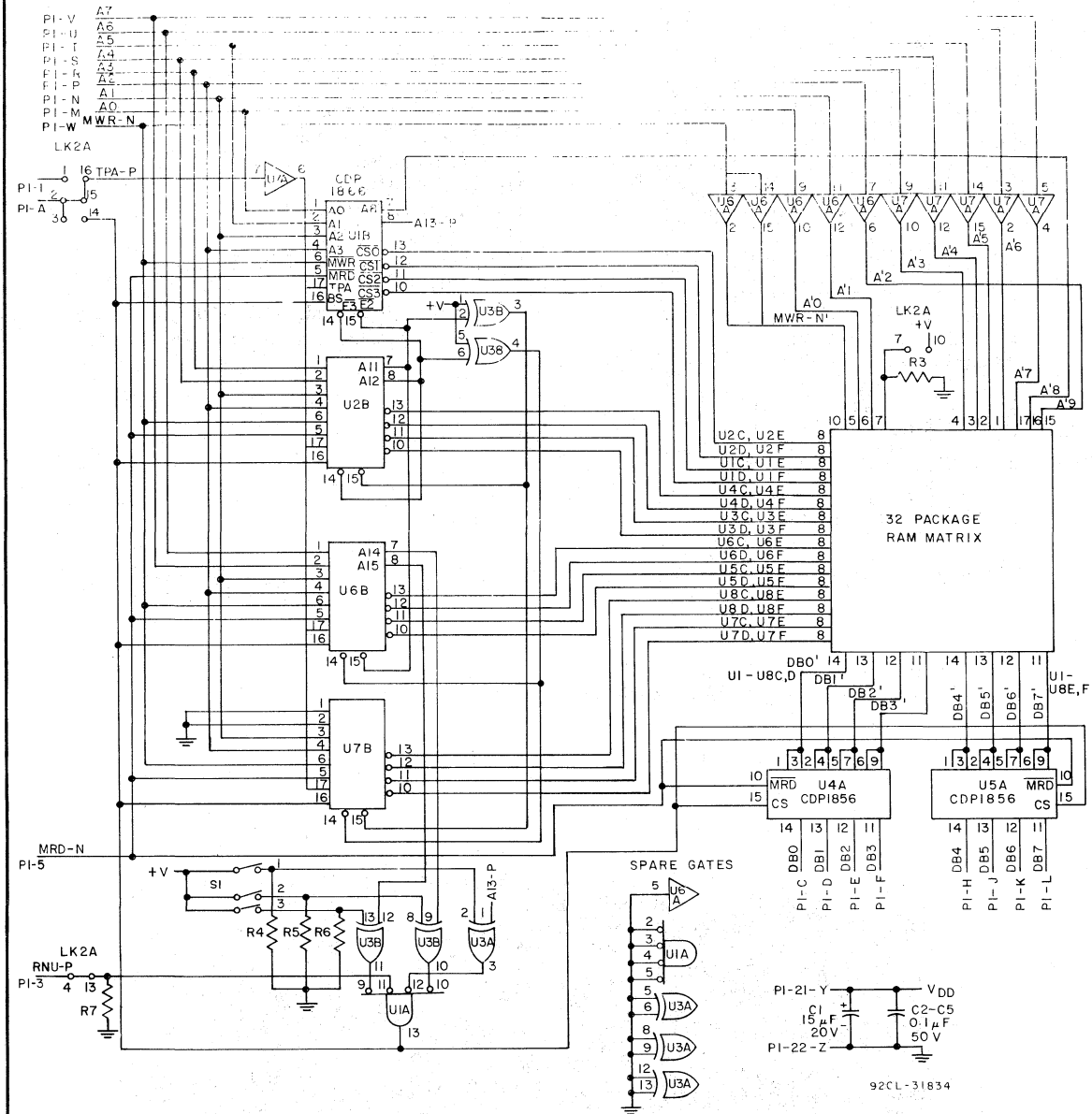
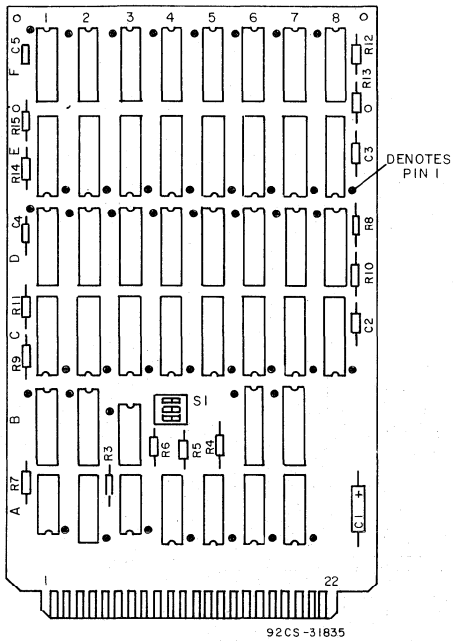


Fig. 2 - Logic diagram for RCA COSMAC Microboard 8-kilobyte RAM CDP18S623.

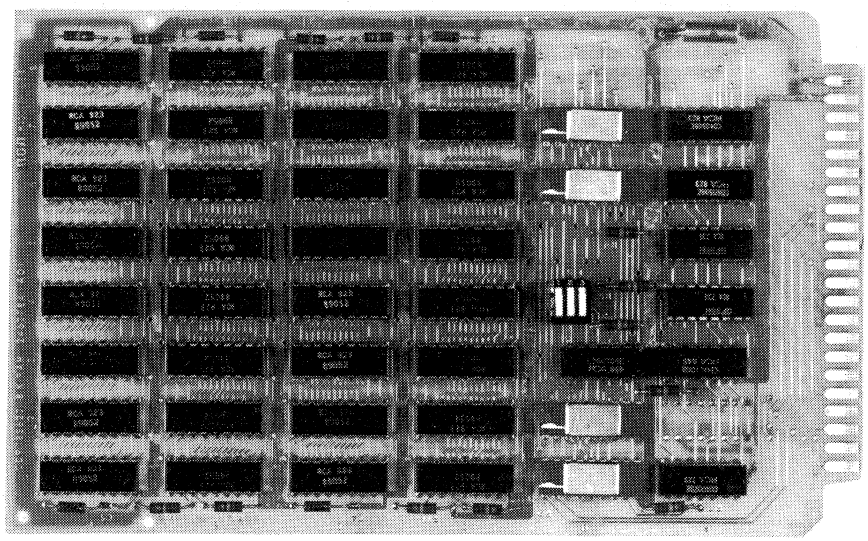
CDP18S623



Parts List

C1 = 15 μF, 20 V
C2 – C5 = 0.1 μF, 50 V
R3 – R15 = 22 kilohms, ¼ W
S1 = 3-rocker DIP switch
U1A = CD4002BE
U3A = CD4081BE
U4A, U5A = CDP1856CE
U6A, U7A = CD4050BE
U1B, U2B, U6B, U7B = CDP1866CE
U3B = CD4070BE
U1C – U8C, U1D – U8D, U1E – U8E, U1F – U8F = 89051/2 (replacement part: MWS5114E-5)

Fig. 3 - Layout diagram of RCA COSMAC Microboard 8-Kilobyte RAM CDP18S623.



RCA COSMAC Microboard 8/16/32-Kilobyte ROM/PROM

The RCA Microboard 8/16/32-Kilobyte ROM/PROM CDP18S625 provides eight sockets for up to 32 kilobytes of non-volatile storage. The address latching and decoding are on board, as well as the switches and links for selection of ROM type, quantity, and address map. The ROM positions are divided into two groups of four. Each group may be placed independently in any area of the 64-kilobyte memory space.

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- Small board size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- Fully buffered
- High noise immunity
- Flexible address assignment
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range: 0 °C to 70 °C

Specifications

Memory Capacity
Eight sockets for 1 to 32 kilobytes of ROM using the CDP18S834, 2758, 2716, or 2716, or 2732

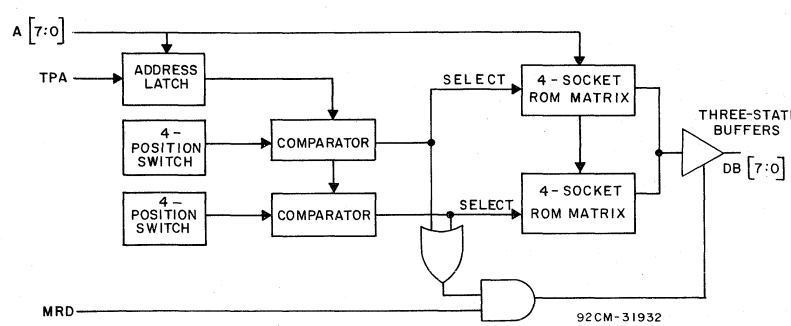
Memory Addressing
Two blocks, each occupying any contiguous block of 1 to 16 kilobytes depending on ROM type selected
User-selectable block address

Operating Temperature
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
+5 volts at 10 milliamperes typical, operating at 2-MHz system clock and using eight CDP1834 CMOS ROM's

Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers



Block diagram of RCA COSMAC Microboard 8/16/32-Kilobyte ROM CDP18S625.

CDP18S640, CDP18S640V1

RCA COSMAC Microboard Control and Display Modules

Advance Data

The RCA COSMAC Microboard Control and Display Module CDP18S640 provides the operating controls and the display for any Microboard system. It includes four switches (RESET, RUN U, RUN P, and STEP/CONT), six hexadecimal display digits, six LED status indicators, two sockets which may be used for either 2 kilobytes of mask-programmed ROM (CDP1834) or 2 kilobytes of EPROM (2708 or 2758) a Utility ROM, a one-page (256-byte) RAM for use by either the utility program or the user program, and an interface for Microterminal CDP18S021.

The CDP18S640 and CDP18S640V1 are identical except for the utility program and the way the program communicates with the user terminal. In the CDP18S640, communication is through the Q and EF4 lines on the associated Microboard Computer. In the CDP18S640V1, communication is through a UART in an associated Microboard module (either the CDP18S602 Microboard Computer or the CDP18S641 Microboard UART Interface).

The six digit hexadecimal **display** utilizes four of the digits for current memory address and two for current data bus content. The six indicator LED's display the status of the following lines: S0, S1 (state code), Q (programmable latched output), WT, CLR (machine mode indicators), and RUN (machine running, not idle, not reset).

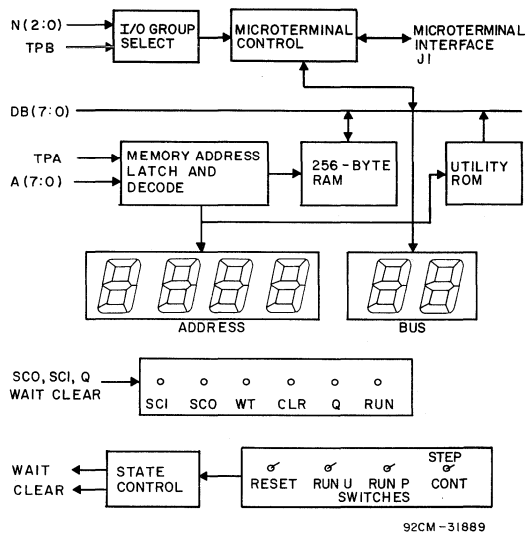
The four **control** switches, labeled RESET, RUN P, RUN U, STEP/CONT, enable the operator to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch. By means of this facility, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles.

The ROM-based **Utility Program** operates through any standard data terminal (RS232C or 20 milliampere loop) to allow the user to examine memory, alter memory, or begin execution at any specified address. These functions are accomplished through a series of commands initiated by a ?, !, or $. The functions include memory insert (!M), memory display (?M), memory move ($M), memory fill ($F), memory substitute (!S), and run program ($P). The move and fill functions can also be called by user programs.

The Utility Program includes read and type routines which provide communication with the user terminal.

Features

- Low-power static CMOS
- High noise immunity
- Small size (4.5 x 7.5 inches)
- Operable from single 5-V supply
- Compatible with COSMAC Development Systems
- Interface for Microterminal CDP18S021
- Member of extensive Microboard family
- Uses Microboard Universal Backplane
- Provides control and display for any Microboard system
- Four control switches: RESET, RUN PROGRAM, RUN UTILITY, STEP/CONTINUOUS
- Six hexadecimal display digits
- Six LED status displays
- One-page (256-byte) RAM for either utility or user programs
- Utility ROM on board
- 0° to 70°C temperature range



Block diagram of RCA COSMAC Microboard Control and Display Module CDP18S640.

CDP18S640, CDP18S640V1

Once the system has been reset, the user can either press RUN P to begin program execution at location 0000_{16} or press RUN U to begin execution of the Utility Program at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and an (LF) half-duplex operation and, at the same time, calculate the time constant to match the baud rate of the data terminal, if required.

The Utility Program also includes user-callable routines which help to simplify user programming. These routines provided register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are destroyed, however, by the process. The CPU register contents can be examined by displaying memory (?M) beginning at $8C00_{16}$ for 20_{16} bytes.

When the Utility Program is ready to accept commands, it types out an asterisk (*) as a user prompt.

Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P	*	2	DMAO-N	*
C	DB0-P	*	3	RNU-P	*
D	DB1-P	*	4	INT-N	
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	*
H	DB4-P	*	7	SC0-P	*
J	DB5-P	*	8	SC1-P	*
K	DB6-P	*	9	CLEAR-N	*
L	DB7-P	*	10	WAIT-N	*
M	A0-P	*	11	−5 V/−15 V	
N	A1-P	*	12	SPARE	
P	A2-P	*	13	CLOCK OUT	
R	A3-P	*	14	N0-P	*
S	A4-P	*	15	N1-P	*
T	A5-P	*	16	N2-P	*
U	A6-P	*	17	EF1-N	
V	A7-P	*	18	EF2-N	
W	MWR-N	*	19	EF3-N	*
X	EF4-N		20	+12 V/+15 V	
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard 8-Kilobyte RAM CDP18S640.

Specifications

Control Switches

RESET—Clears system and holds it in reset state

RUN P—Initializes system and starts program execution at 0000_{16}

RUN U—Initializes system and starts UT60 execution at 8000_{16}

STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution

Displays

4 hex digits for address

2 hex digits for data

6 discrete LED's for status:

S0, S1 = State code

Q = Programmable latched output

WT, CLR = Machine mode indicators

RUN = Machine running, not at idle, not reset

Memory Capacity

RAM—256 bytes

ROM—1 kilobyte preprogrammed with Utility Program UT60 (CDP18S640) or UT61 (CDP18S640V1)

Operating Temperature Range

0° to 70 °C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum

Connectors

System interface: edge fingers, 44 pins (dual 22) on 0.156-inch centers

Microterminal interface: connector, 20 pins

Power Requirements

+5 volts at 350 milliamperes, typical operating

Terminal Baud Rates

CDP18S640 (UT60) works with 110, 300, or 1200 baud. Software detects baud rate of terminal and generates a matching rate.

CDP18S640V1 (UT61) works with 50 to 19,200 baud, switch-selected at UART baud-rate generator.

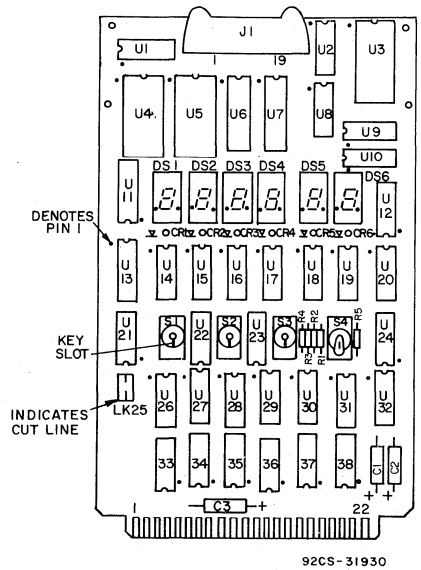
CDP18S640, CDP18S640V1

Parts List

C1, C2, C3 = 15 μF, 20 V
CR1-CR6 = LED
DS1-DS6 = 7-segment display
J1 = connector, 20 pin
R1-R5 = 22 kΩ, ¼ W, 5%
S1, S2, S3 = switch, momentary
S4 = switch, SPDT
U1 = CDP1858CE
U2, U8 = CDP1856CE
U3 = CDP1852CE
U4 = Utility ROM
U6, U7 = MWS5101EL-3
U9, U10 = CDP1857CE
U11, U13 = CDP1866CE
U12 = CD4078BE
U14-U19 = MC14495P
U20 = CDP1853CE
U21 = CD4023BE
U22 = CD4071BE
U23 = CD40106BE
U24 = CD4081BE
U26 = CD4042BE
U27 = CD4069BE
U28, U33, U36 = CD4050BE
U29 = CD4025BE
U30 = CD4011BE
U31 = CD4076BE
U32, U34 = CD4013BE
U35 = CD4016BE
U37 = CD4001BE
U38 = CD4012BE

XDS1-XDS6 = DIP socket, 10 pin
XU4, XU5 = IC socket, 24 pin

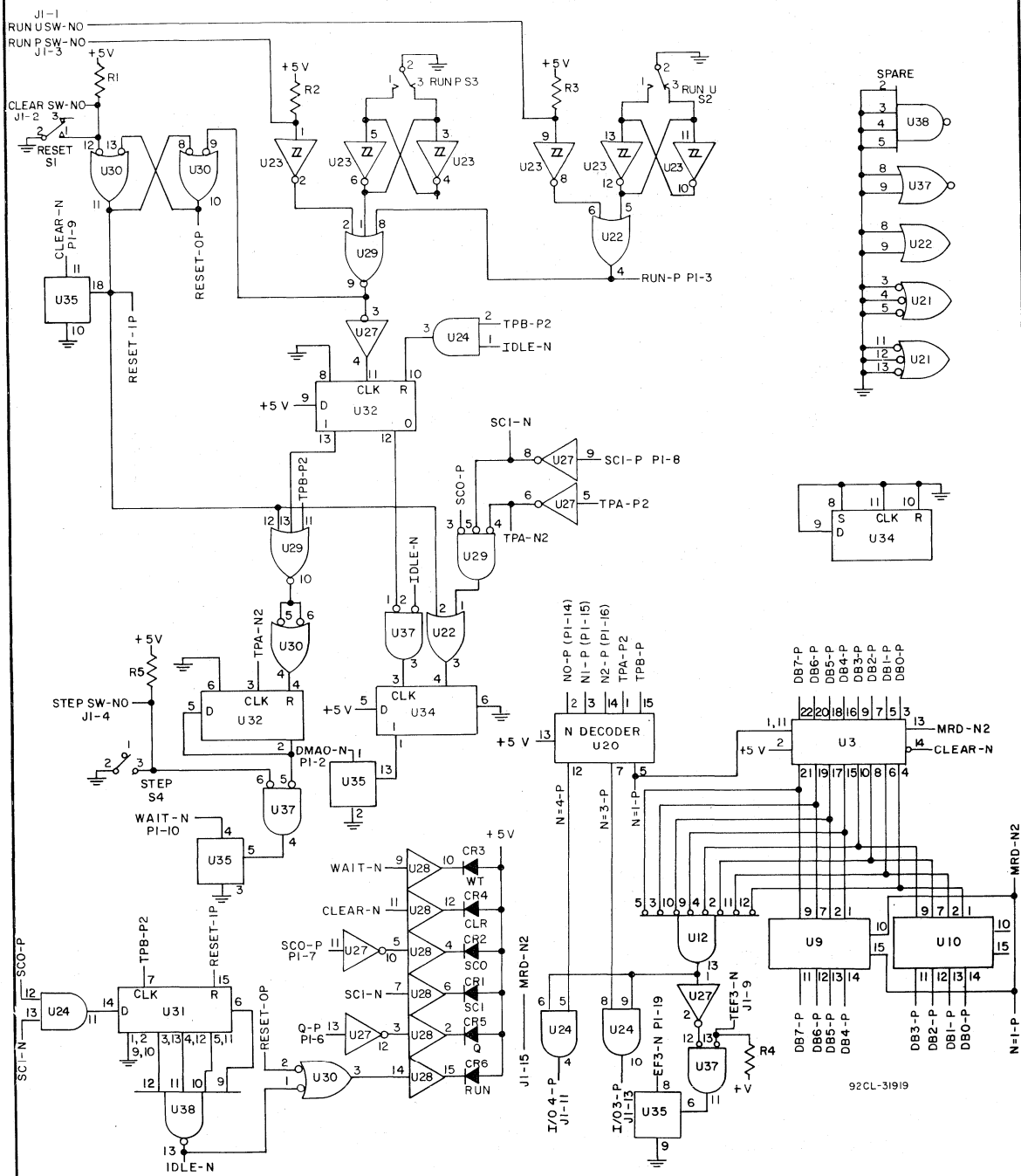
Layout diagram of RCA COSMAC Microboard Control and Display Module CDP18S640.



Microterminal CDP18S021 Connections on Microboard Control and Display Module CDP18S640 (J1)

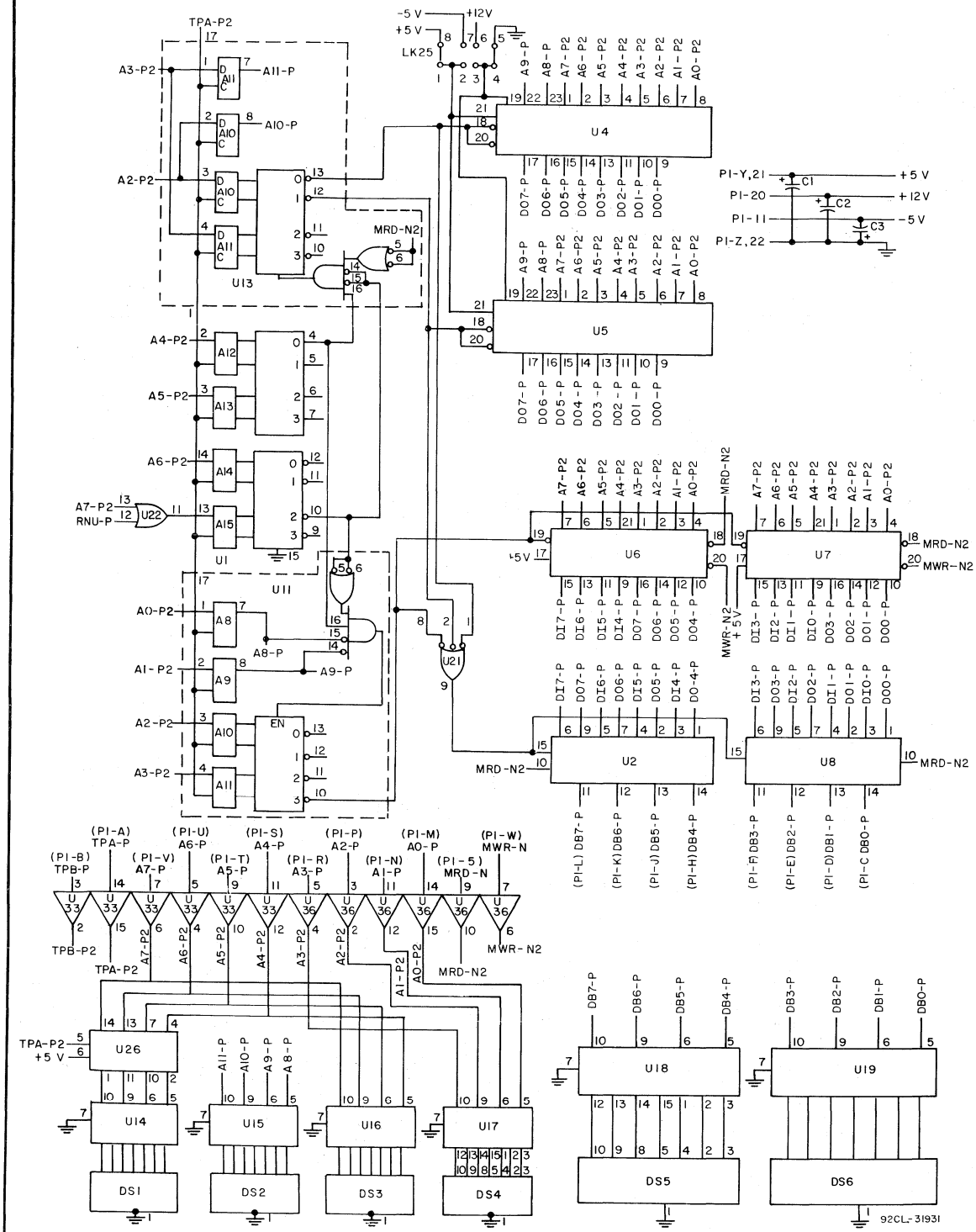
Pin	Signal	Pin	Signal
1	RUN U-N0	2	CLEAR-N0
3	RUN P-N0	4	STEP-N0
5	V_{LED}	6	DB0-P
7	V_{CC}	8	DB1-P
9	TEF3-N	10	DB2-P
11	IO4-P	12	DB3-P
13	IO3-P	14	DB4-P
15	MRD-N	16	DB5-P
17	TPB-P2	18	DB6-P
19	GND	20	DB7-P

CDP18S640, CDP18S640V1



Logic diagram of Microboard Control and Display Module CDP18S640—control and status indicator portion.

CDP18S640, CDP18S640V1



Logic diagram of Microboard Control and Display Module CDP18S640—memory and memory display portion.

CDP18S641

RCA COSMAC Microboard UART Interface

The RCA COSMAC Microboard UART (Universal Asynchronous Receiver Transmitter) Interface Module CDP18S641 is a parallel-to-serial I/O data controller utilizing the RCA CDP1854A UART. The CDP18S641 is designed for use in a Microboard computer system or in the COSMAC Development Systems CDP18S005 and CDP18S007. It provides an efficient byte interface to the system while serial data are transmitted and received at the remote interface. Baud rates from 110 to 19,200 are switch-selectable. It provides for full-duplex operation.

The CDP18S641 also provides two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations.

Features

- Low-power static CMOS
- High noise immunity
- Small board size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with COSMAC Development Systems
- Flexible address assignment
- Selectable baud rate
- Selectable serial interface: RS232C or 20-mA loop
- Paper-tape-reader run control
- Temperature range: 0 °C to 70 °C

Specifications

UART
CDP1854A, programmed mode.

Parity
Even or odd, or inhibited.

Stop Bits
One or two.

Word Length
5, 6, 7, or 8 bits.

Baud Rate
Crystal-controlled, switch-selectable for 110, 300, 1200, 4800, 9600, or 19,200 baud.

Addressing
I/O space, link-selectable for both N codes and I/O group number.

Serial Interface
20-mA loop or RS232C.

Operating-Temperature Range
0 °C to 70 °C.

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm);
Board pitch - 0.5 inch (12.7 mm) minimum.

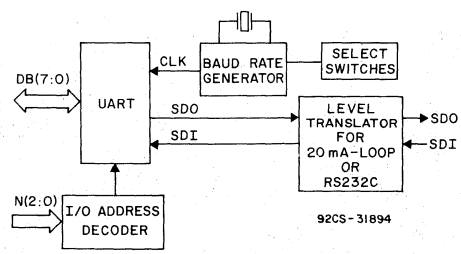
Power Requirements

Voltage (V)	With EIA RS232C Terminal	With 20-mA Loop Terminal
+5	2.0 mA	21 mA
−5 to −15	7.5 mA	not required
+12 to +15	8.5 mA	not required

Connectors

System interface: Edge fingers, 44 pins on 0.156-inch centers.

Serial interface: Two right-angle 10-pin headers to mate with connectors comprised of
housing - AMP 1-86148-2
contact - AMP 86016-1
keying plug - AMP 87077-1



Block diagram of RCA COSMAC Microboard UART Interface CDP18S641.

CDP18S641

Microboard Bus Interface Signals (Connector P1)

The RCA COSMAC Microboard UART Interface Module CDP18S641 makes use of the following signals in the Microboard Universal Bus Interface.

DB7 through DB0 - These eight bidirectional data bus lines communicate directly with the CDP1854A UART, which has internal controls to establish direction and timing. In addition, DB7 is used to set the paper-tape-reader control, and DB7 through DB0 are used, through a system of optional links, to define the I/O group chosen for this board.

N0, N1, N2 - The N lines, which define the primary I/O address, are wired to a CDP1853 decoder. The CDP1853 outputs 7 through 1 are connected through optional links to the CDP1854A UART.

MRD - The Memory Read line is used by the CDP1854A UART to identify proper direction of data flow on the bidirectional data bus. When true, this line indicates that data are being read from memory and, therefore, written to the I/O device, if an I/O operation is in progress. The direction is reversed when MRD is false.

TPA - This timing pulse is used only by the N decoder to set its output enable at the trailing edge of TPA.

TPB - This timing pulse is used by the CDP1854A UART to latch data written to it. It is also used by the N decoder to terminate its output enable at the trailing edge of TPB.

INT - This signal may be connected by optional link LK24 pins 1 and 14 to the INT output from the CDP1854A UART. This signal is buffered by a transmission gate so that wired-"OR" connection may be made with other devices driving the backplane INT line.

EF1, EF2, EF3, EF4 - Links are provided (link LK24) so that these flag lines may be wired to outputs from the CDP1854A UART. The outputs are Data Available (DA), Transmitter Holding Register Empty (THRE), Overrun Error or Parity Error (OE/PE), Framing Error (FE), and Serial Data In (SDI).

CLEAR - This signal provides an initialization signal for the CDP1854A UART and resets the paper-tape-motor control.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the RCA COSMAC Universal Backplane Connector (P1). The signals marked with an asterisk (*) are those used on the RCA COSMAC Microboard UART CDP18S641.

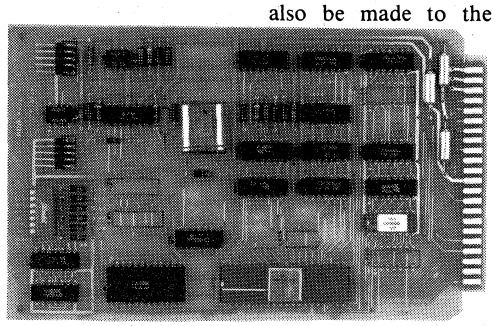
Table I - Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Pin	Signal		Pin	Signal	
A	TPA-P	*	1	DMAI-N	
B	TPB-P	*	2	DMAO-N	
C	DB0-P	*	3	RNU-P	
D	DB1-P	*	4	INT-N	*
E	DB2-P	*	5	MRD-N	*
F	DB3-P	*	6	Q-P	
H	DB4-P	*	7	SC0-P	
J	DB5-P	*	8	SC1-P	
K	DB6-P	*	9	CLEAR-N	*
L	DB7-P	*	10	WAIT-N	
M	A0-P		11	−5 V/−15 V	*
N	A1-P		12	SPARE	
P	A2-P		13	CLOCK OUT	
R	A3-P		14	N0-P	*
S	A4-P		15	N1-P	*
T	A5-P		16	N2-P	*
U	A6-P		17	EF1-N	*
V	A7-P		18	EF2-N	*
W	MWR-N		19	EF3-N	*
X	EF4-N	*	20	+12 V/+15 V	*
Y	+5 V	*	21	+5 V	*
Z	GND	*	22	GND	*

*Signals used on RCA COSMAC Microboard UART Interface CDP18S641.

Operation

The operation of the RCA COSMAC Microboard UART Interface CDP18S641 can be understood by reference to the logic diagrams. Reference should also be made to the technical data sheet for the



CDP1854A UART (U10 on the logic diagram) for Mode 1 operation details.

The crystal-controlled oscillator circuit and the divide-by-N counter CD4059AE (U4) provide a clock for the UART at a frequency 16 times the rate selected by the user via the baud rate switch (S1), as required by the UART.

The clear-to-send-in signal CTS-IN from the connector J2 to the UART may be left floating, if desired, and it will assume the true state at the UART. The clear-to-send-out signal CTS-OUT is driven by the data available signal DA from the UART with a trailing edge delay. This signal may be used for handshaking, for example, between two UART modules. This output may be made true all the time by changing link LK18 to the A position.

Any communication with the UART Interface CDP18S641, or with any Microboard I/O Controller, must be started by the transmittal of the I/O group select number assigned to the controller. The system software transmits the group number by issuing an OUT1 (61_{16}) command whose data is the group number desired. This group number then stays selected until another OUT1 command supersedes it. Group number assignment details are given in the next section on **Installation.**

To operate the paper-tape reader, the system software should issue an output instruction 67 with the data byte containing a 1 in bit seven (most significant bit). The CD4096BE J-K flip-flop (U16) is triggered to the set state by this command, making the signal PT RDR low, thus enabling the tape reader. As soon as the reader starts to transmit data, the signal Serial Data In (SDI) causes the J-K flip-flop (U16) to be triggered to the reset state. As a result, one byte is transmitted to the UART and the tape is stopped before the next byte. Another 67 instruction, therefore, must be issued for each successive byte.

Installation in a Microboard Computer System

Installation of the Microboard UART Interface CDP18S641 in a Microboard Computer System requires only the setting of the proper baud rate switch (S1), as marked, unless the preselected addresses are not appropriate. The preselected addresses are as follows:

I/O GROUP = 02_{16}
DATA INPUT = IN2 ($6A_{16}$)
DATA OUTPUT = OUT2 (62_{16})
STATUS INPUT = IN3 ($6B_{16}$)
CONTROL OUTPUT = OUT3 (63_{16})
FLAG AND INTERRUPT LINES ARE OPEN

A system of link positions is provided so that the user can select variations of the above functions. The links are arranged and numbered in a DIP configuration for ease of identification and to allow installation of DIP switches, headers, or other aids in the event frequent changes are anticipated.

For changes in the I/O group assignment, refer to Table II for links LK5 and LK14.

The primary addresses for data transfer and status/control transfer are prewired for Input/Output 2 and Input/Output 3, respectively. Should different I/O instructions be required, Link LK20 should be wired as follows.

For data transfer, wire link LK20 pin 4 to:

Pin 11 = INPUT 2, OUTPUT 2
Pin 9 = INPUT 3, OUTPUT 3
Pin 14 = INPUT 4, OUTPUT 4
Pin 12 = INPUT 5, OUTPUT 5
Pin 10 = INPUT 6, OUTPUT 6
Pin 8 = INPUT 7, OUTPUT 7

For status in or control out, wire link LK20 pin 6 to:

Pin 11 = INPUT 2, OUTPUT 2
Pin 9 = INPUT 3, OUTPUT 3
Pin 14 = INPUT 4, OUTPUT 4
Pin 12 = INPUT 5, OUTPUT 5
Pin 10 = INPUT 6, OUTPUT 6
Pin 8 = INPUT 7, OUTPUT 7

Link LK24 provides a means of connecting the UART interrupt to the system interrupt, as well as the UART status bits to the external flags EF1 through EF4 of the system. The interrupt is then unconditioned, but the flags are enabled by the group select. Thus, an interrupt-identification polling scheme may be implemented by system software. Polling may also be accomplished by reading status from the UART, if the user does not wish to connect the links for status or interrupt. Connections for selecting interrupt or any of the status bits may be identified on the logic diagram.

CDP18S641

Installation in a COSMAC Development System CDP18S005 or CDP18S007

Installation in the CDS II (CDP18S005) or the CDS III (CDP18S007) is the same as for installation in a Microboard computer system except that the Development System backplane must have certain signals wired to the UART location. The user should select an empty slot in the I/O section (slots 19 and 20 should be avoided), and then install the following wires in that slot.

Pin 9 to pin 13	RESET-OP
Pin 14 to Slot 13 pin 14	N0-P
Pin 15 to Slot 13 pin 15	N1-P
Pin 16 to Slot 13 pin 16	N2-P

Table II - I/O Group Select Link Connections

	LK5								LK14				
I/O Group	1-16	3-14	5-12	7-10	2-15	4-13	6-11	8-9	1-10	2-9	3-8	4-7	5-6
01	O	O	O	S	S	S	S	O	O	O	O	O	S
02*	O	O	O	S	S	S	S	O	O	O	O	S	O
04	O	O	O	S	S	S	S	O	O	O	S	O	O
08	O	O	O	S	S	S	S	O	O	S	O	O	O
10	O	O	O	S	S	S	S	O	S	O	O	O	O
20	O	O	S	O	S	S	O	S	S	O	O	O	O
30	O	O	S	S	S	S	O	O	S	O	O	O	O
40	O	S	O	O	S	O	S	S	S	O	O	O	O
50	O	S	O	S	S	O	S	O	S	O	O	O	O
60	O	S	S	O	S	O	O	S	S	O	O	O	O
70	O	S	S	S	S	O	O	O	S	O	O	O	O
80	S	O	O	O	O	S	S	S	S	O	O	O	O
90	S	O	O	S	O	S	S	O	S	O	O	O	O
A0	S	O	S	O	O	S	O	S	S	O	O	O	O
B0	S	O	S	S	O	S	O	O	S	O	O	O	O
C0	S	S	O	O	O	O	S	S	S	O	O	O	O
D0	S	S	O	S	O	O	S	O	S	O	O	O	O
E0	S	S	S	O	O	O	O	S	S	O	O	O	O
F0	S	S	S	S	O	O	O	O	S	O	O	O	O

*Group 02 is preprinted. O = Open S = Shorted

Parts List

C1, C2, C3 = 15 μF, 50 V
C4 = 0.33 μF, 50 V

CR1 – CR7 = 1N914

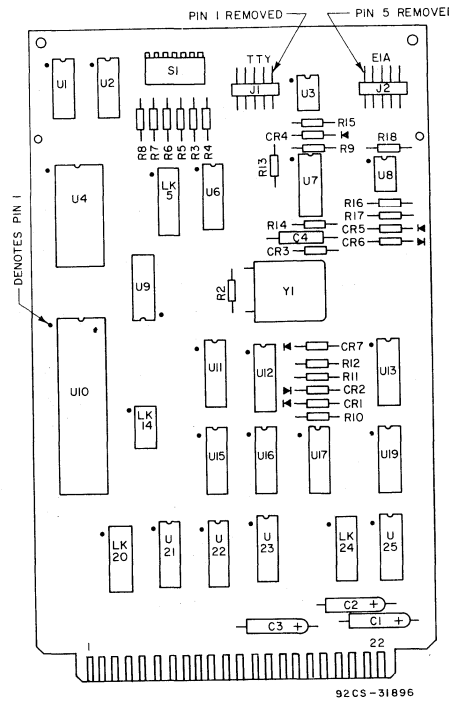
J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP 86016-1, keying plug — AMP 87077-1, or equivalent)

R2 = 10 MΩ, ¼ W
R3 – R8 = 22 kΩ, ¼ W
R9 = 910 Ω, ¼ W
R10, R15 = 10 kΩ, ¼ W
R11, R16 = 47 kΩ, ¼ W
R12 = 4.7 kΩ, ¼ W
R13, R14 = 470 Ω, ¼ W
R17 = 4.3 kΩ, ¼ W
R18 = 560 Ω, ¼ W

S1 = 7-position DIP

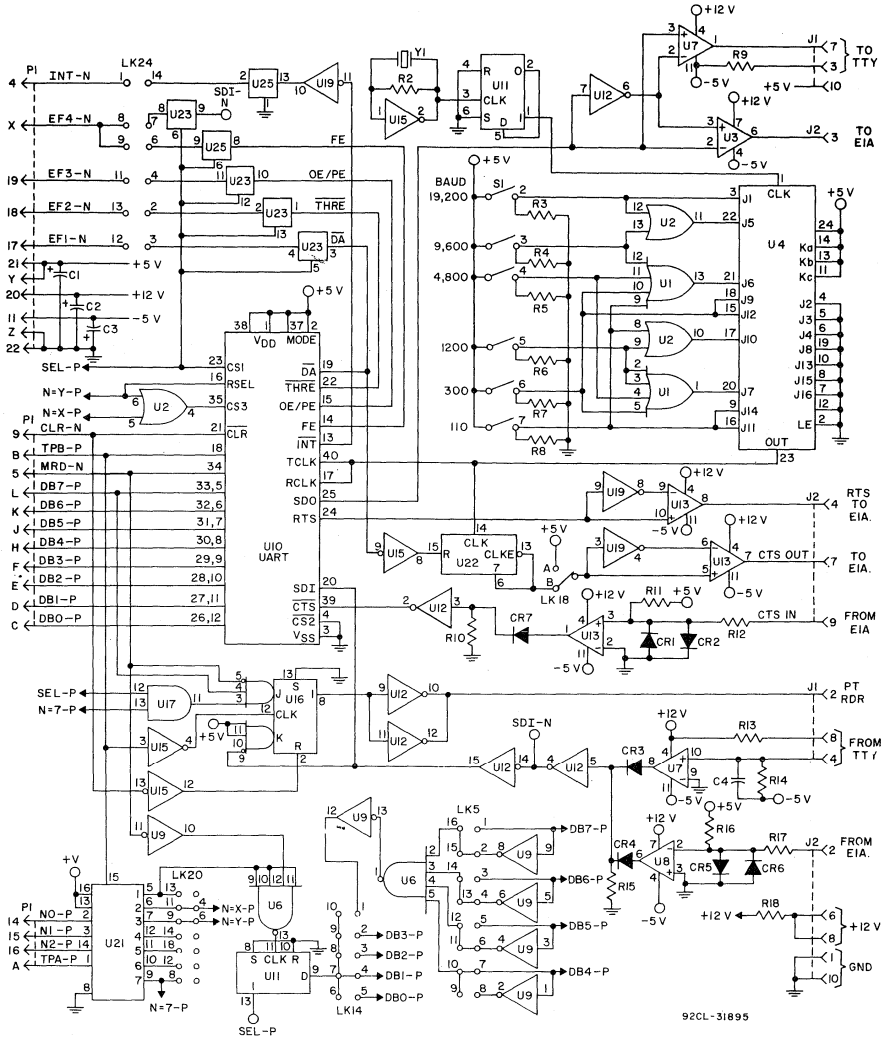
U1 = CD4072BE
U2 = CD4071BE
U3, U8 = CA3140E
U4 = CD4059AE
U6 = CD4012BE
U7, U13 = CA324E
U9, U15, U19 = CD4069BE
U10 = CDP1854ACE
U11 = CD4013BE
U12 = CD4049BE
U16 = CD4096BE
U17 = CD4081BE
U21 = CDP1853CE
U22 = CD4017AE
U23, U25 = CD4016BE

Y1 = 1.8432-MHz crystal



Layout diagram of RCA COSMAC Microboard UART Interface Module CDP18S641.

CDP18S641



Logic diagram of RCA COSMAC Microboard UART Interface Module CDP18S641.

CDP18S642
Advance Data

RCA COSMAC Microboard D/A Converter

The RCA Microboard D/A Converter CDP18S642 is a two-channel digital-to-analog converter having 12-bit or 8-bit resolution. The user can select either a current output, a bipolar voltage output, or a unipolar voltage output. The settling time is 5 microseconds. Its I/O address is assignable. The CDP18S642 requires +15 volts and −15 volts in addition to +5 volts.

Features

- Low-power static CMOS
- Small board size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- High noise immunity
- Assignable I/O address
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range: 0 °C to 70 °C

Specifications

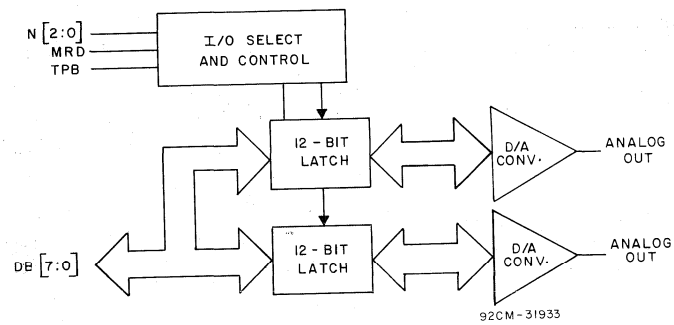
Operating Temperature
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
+5 volts at 24 milliamperes typical
+15 volts at 25 milliamperes typical
−15 volts at 25 milliamperes typical

Output Options
±10 volts at 5 milliamperes
±5 volts at 5 milliamperes
±2.5 volts at 5 milliamperes
0 to +10 volts at 5 milliamperes
0 to +5 volts at 5 milliamperes
0 to −2 milliamperes

Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers



Block diagram of RCA COSMAC Microboard D/A Converter CDP18S642.

CDP18S643

RCA COSMAC Microboard A/D Converter

Advance Data

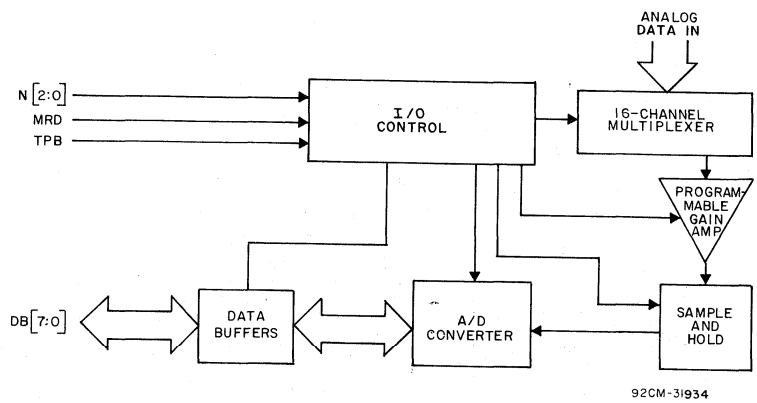
The RCA Microboard A/D Converter CDP18S643 is an analog-to-digital converter having 12-bit or 8-bit resolution. It handles 16 multiplexed analog inputs and has an 8-bit buffered output. The gain of its input amplifier is under program control. The input amplifier feeds into a sample-and-hold circuit. Conversion completion can be recognized by interrupt or by polling. The I/O address is assignable. The CDP18S643 requires +15 volts in addition to +5 volts.

Features

- Low-power static CMOS
- Small board size (4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- High noise immunity
- Assignable I/O address
- Member of extensive Microboard family
- Simple system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Temperature range: 0 °C to 70 °C

Specifications

Operating Temperature
0 °C to 70 °C
Dimensions
4.5 inches x 7.5 inches (114.3 mm x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum
Power Requirements
+5 volts at 80 milliamperes typical
+15 volts at 43 milliamperes typical
−15 volts at 43 milliamperes typical
Input Options
8 channel differential
16 channel, single-ended
Conversion Time
25 microseconds for 12 bits
Connector
System interface: edge finger, 44 pins (dual 22) on 0.156-inch centers



Block diagram of RCA COSMAC Microboard A/D Converter CDP18S643.

CDP18S659

RCA COSMAC Microboard Breadboard

Advance Data

The RCA COSMAC Microboard Breadboard CDP18S659 is a blank module designed to mate with the Microboard Universal Backplane connector and to provide the user with the ability to breadboard modules of his own design and to try them out quickly and efficiently in one of the RCA Microboard chassis.

CDP18S660

RCA COSMAC Microboard Combination Memory and I/O Module

Advance Data

The RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660 contains 40 programmable I/O lines, 2 kilobytes of static RAM, and four on-board sockets for read-only memory enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or EPROM, depending on the applications. The CDP18S660 is designed for use in a Microboard computer system or in the COSMAC Development Systems CDP18S005 and CDP18S007.

By means of the two CMOS programmable I/O interface CDP1851's, the CD18S660 provides 40 programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit programmable, with or without unique "handshaking" signals for each application. Edge connectors are provided for the parallel I/O lines as well as for the Microboard Universal Backplane Interface.

By means of four MWS5114 static CMOS RAM's, the CDP18S660 provides two kilobytes of read-write memory. In addition, four sockets are provided for four to eight kilobytes of non-volatile read-only memory. RCA-CDP1834 mask-programmed ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in the 65,536-byte memory space on one kilobyte boundaries.

Because of the CMOS design and low current requirements, the CDP18S660 power supply and cooling requirements are minimal.

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- High noise immunity
- Compatible with COSMAC Development Systems
- 2 kilobytes of read/write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- 40 programmable I/O lines
- 44-pin system interface
- Temperature range: 0 °C to 70 °C
- Small board size: 4.5 x 7.5 inches
- RAM and ROM independently assignable within memory space
- Assignable I/O addresses

Specifications

Memory Capacity
On-board RAM: 2 kilobytes
On-board ROM/EPROM: 4 sockets for up to 8 kilobytes (CDP1834, 2708, 2758, 2716)

Memory Address Map
On-board RAM: Any even 2-kilobyte block
On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block

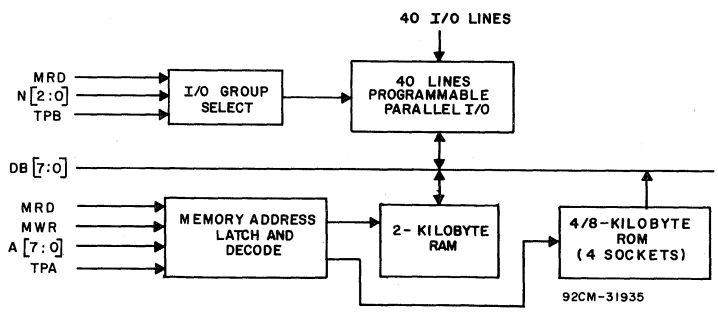
I/O Capacity
40 parallel lines programmable as input, output, or bidirectional

Operating-Temperature Range
0 °C to 70 °C

Dimensions
4.5 inches x 7.5 inches (114.3 x 190.5 mm)
Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements
With CMOS ROM's: +5 V at 8 mA, typical operating

Connectors
System Interface: Edge fingers, 44 pins on 0.156-inch centers
Parallel I/O: Edge fingers, 50 pins on 0.100-inch centers



Block diagram of RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660.

CDP18S670

RCA COSMAC Microboard 25-Card Chassis with Case and Power Supply

Advance Data

Features

- Preprinted Microboard Universal Backplane for 20 cards
- 5 additional slots with power and ground only for user-option cards
- Power supply for three voltages: +5 V, +15 V, and −15 V
- Mountable on 19-inch rack
- Metal protective case
- Swing-open front panel

The RCA COSMAC Microboard 25-Card Chassis with Case and Power Supply CDP18S670 provides a convenient, versatile means for assembling a computer system utilizing an extensive number of RCA Microboard Milliwatt Computer System modules or compatible user-designed modules. The chassis consists of twenty-five sockets with integral card guides mounted on a printed-circuit backplane. Twenty of the positions are preprinted with the RCA Microboard Universal Backplane. The other five positions are provided with power and ground only and can be wired to suit the user application.

The metal protective case is provided with access holes for the connection of flat cables to the end of the Microboard modules having outboard connectors.

CDP18S675, CDP18S676

RCA COSMAC Microboard 5-Card Chassis

The RCA COSMAC Microboard 5-Card Chassis CDP18S675 and CDP18S676 provide compact, low-cost means for assembling systems comprised of members of the RCA Microboard milliwatt computer system family. The chassis consists of five sockets with integral card guides mounted on the RCA COSMAC universal printed-circuit backplane. The backplane pin-connection configuration is shown in Table I. For expansion beyond five cards, multiple chassis can be stacked by the soldering of an edge socket connection to the pads provided on the backplane. The added chassis mates with the edge socket through the gold-plated edge fingers.

The CDP18S675 may be mounted by means of the threaded brass inserts in each card socket.

The CDP18S676 includes a CDP18S675 chassis plus a metal base and a protective cover. The base is provided with rubber feet as well as holes for vertical mounting. Access holes are provided for the connection of flat cables to either the backplane or to the opposite end of the Microboard modules having additional outboard connectors.

Specifications

Backplane
- 0.062-inch printed-circuit board
- Five locations for 44-pin connectors
- Universal wiring (like pins connected)
- Power bus (+5 volts) on pins 21 and X
- Ground bus on pins 22 and Z

Card Socket Connectors
- 44 pin (22 dual) on 0.156-inch centers
- Integral plastic card guides

Features

- Universal backplane
- Five card slots
- Expansion and nesting interface
- Protective base and metal cover (CDP18S676 only)
- Integral card guides

Edge Connector
- Gold-plated fingers on 0.100-inch centers
- 50 pins (dual 25)
- Mates with industry-standard flat cable connectors

Edge Connector Socket Provision
- Provision is made for lap-solder mounting of an edge-connector socket (AMP PN 530278-2 or 530282-2) that will mate with the edge fingers described above for stacking two or more chassis.

Dimensions

CDP18S675 (See photo)
- Length (L) = 5 inches (127 mm)
- Depth (D) = 4 inches (102 mm)
- Height (H) = 3 inches (76 mm)

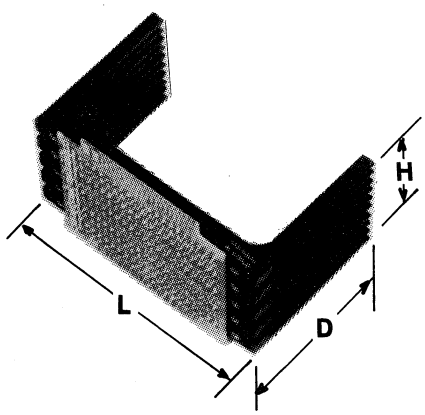
CDP18S676
- Length = 9-7/16 inches (240 mm)
- Width = 5-1/4 inches (133 mm)
- Height = 3-1/2 inches (89 mm)

Weight
- CDP18S675: 5-1/2 ounces (155 grams)
- CDP18S676: 3 pounds 11 ounces (1.67 kilograms)

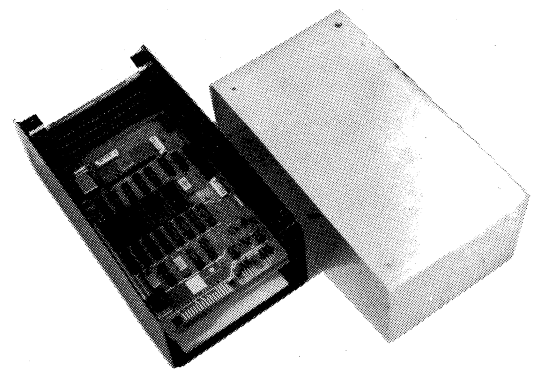
CDP18S675, CDP18S676

Pin Terminals and Signals for the RCA COSMAC Microboard Universal Backplane Connector (P1)

Pin	Signal	Pin	Signal
A	TPA-P	1	DMAI-N
B	TPB-P	2	DMAO-N
C	DB0-P	3	RNU-P
D	DB1-P	4	INT-N
E	DB2-P	5	MRD-N
F	DB3-P	6	Q-P
H	DB4-P	7	SC0-P
J	DB5-P	8	SC1-P
K	DB6-P	9	CLEAR-N
L	DB7-P	10	WAIT-N
M	A0-P	11	−5V/−15V
N	A1-P	12	SPARE
P	A2-P	13	CLOCK OUT
R	A3-P	14	N0-P
S	A4-P	15	N1-P
T	A5-P	16	N2-P
U	A6-P	17	EF1-N
V	A7-P	18	EF2-N
W	MRW-N	19	EF3-N
X	EF4-N	20	+12V/+15V
Y	+5V	21	+5V
Z	GND	22	GND



CDP18S675
5-Card Chassis



CDP18S676
5-Card Chassis with Base and Cover (Microboard Module - not included - shown in position)

CDP18S691

RCA COSMAC Microboard Prototyping System

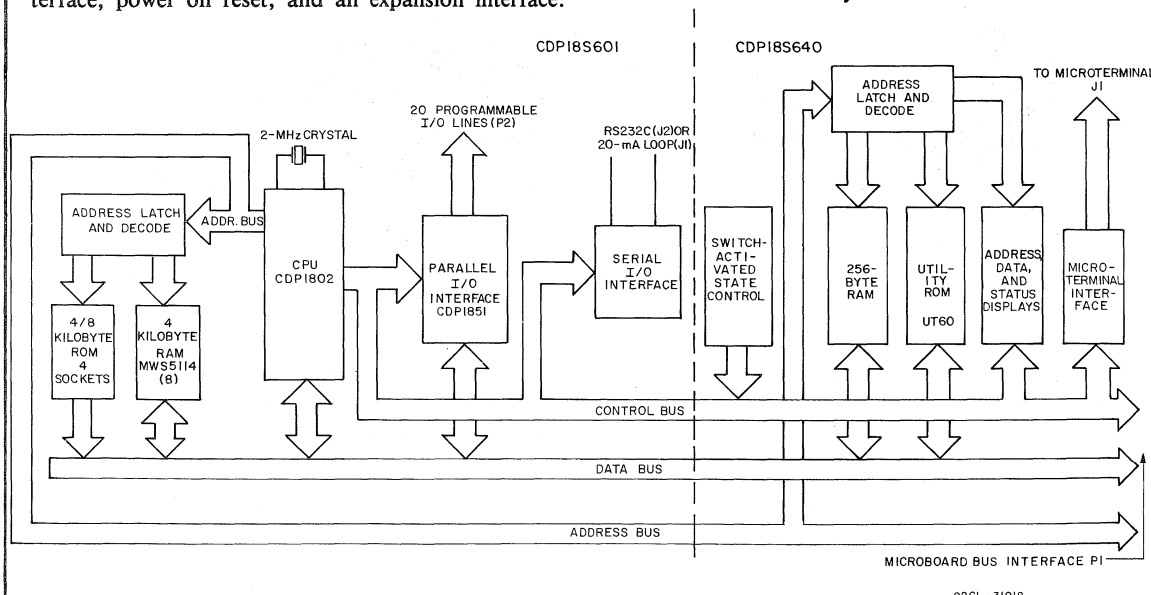
Advance Data

The RCA COSMAC Microboard Prototyping System CDP18S691 is a fully assembled package that includes hardware, software, and technical literature needed to enable the user to design a microcomputer system. It provides a quick, inexpensive way to investigate and evaluate the Microboard family of components, to train personnel in microprocessor usage, and to develop computer systems for custom applications. It has 4 kilobytes of read/write memory and provides for the addition of 4/8 kilobytes of mask programmed ROM or EPROM, depending on the application requirements. The CDP18S691 Prototyping System includes a CDP18S601 Microboard Computer to provide the complete computer function, the CDP18S640 Microboard Control and Display Module to provide the switches and displays for prototyping operation, the CDP18S675 5-Card Chassis containing the preprinted Universal Backplane for all five card positions, the CDP18S023 Power Converter, the CDP18S659 Microboard Breadboard for expansion flexibility, the UT60 ROM-based utility program, technical literature, a protective metal case of functional design, and cables for terminals and I/O.

The **CDP18S601 Microboard Computer** contains a CDP1802 CPU, a crystal-controlled clock, read-write memory, parallel I/O ports, a serial communications interface, power on reset, and an expansion interface.

Features

- Low-power static CMOS
- High noise immunity
- Simple to use
- Easy to expand or modify
- Selectable serial interface—
  RS232C or 20 mA loop
- COSMAC Microprocessor architecture
- Temperature range—0 °C to 70 °C
- 65,536-byte addressable memory range
- Power on rest
- All I/O lines on edge connectors
- Microterminal interface
- Uses COSMAC Microboard Universal Backplane
- CDP18S601 Microboard Computer
- CDP18S640 Control/Display Module
- Five-card chassis
- Protective metal case
- Four control switches
- Six hexadecimal display digits
- 600-mA power converter—regulated
- Six LED displays
- ROM-based monitor software (UT60)
- 2-MHz crystal clock
- Sockets for 4/8-KB ROM/PROM
- 4-KB read/write memory



Block diagram of RCA COSMAC Microboard Prototyping System CDP18S691.

Four on-board sockets are provided for read-only memory, enabling the user to select 4 or 8 kilobytes of mask-programmable ROM or PROM, depending on the applications. Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal.

The **central processor** for the CDP18S601 is the 8-bit silicon-gate CMOS RCA COSMAC Microprocessor CDP1802. The CDP1802 has 16 general-purpose registers each 16 bits wide. Any one of these registers may be dynamically designated as the program counter, thereby giving the system multiiple program states. Each register may also be used for data storage or as memory pointers for subroutines, I/O stacks, and the like. One register each is designated for DMA and Interrupt pointers. The CDP1802 provides a serial data out connection, Q, and four external flag input pins, EF1 through EF4, which may be used as test and branch conditions independently.

By means of eight MWS5114 RAM's, the CDP18S601 provides the Prototyping System with 4 kilobytes of CMOS **read-write memory**. Four sockets are provided for four or eight kilobytes of non-volatile **read-only memory**. RCA CDP1834 mask-programmed CMOS ROM's or 2708, 2758, or 2716 EPROM's may be used in these sockets. Each of these memory types may be placed independently in any of the 16 four-kilobyte blocks comprising the 64-kilobyte system memory space.

By means of the CMOS programmable I/O Interface CDP1851, the CDP18S601 provides the Prototyping System with 20 programmable I/O lines. The software customizes each of these lines as input, output, bidirectional, or bit-programmable with or without unique handshaking signals for each application. A serial communications interface, provided with both 20-milliampere loop and EIA RS232C capability, is driven by the Q and EF4 serial I/O lines of the CPU. The baud rate and the data format are determined by software. Edge connectors are provided for the parallel I/O lines and the Microboard Universal Backplane. Right-angle header connections are provided for the serial communications interfaces.

The **CDP18S640 Control and Display Module** provides the Prototyping System with its operating controls, consisting of four switches, and its display system, consisting of six hexadecimal digits and six status indicators. In addition, the CDP18S640 provides two sockets which may be used for either 2 kilobytes of mask-programmable ROM (CDP1834) or 4 kilobytes of EPROM (2708, 2758, or 2716). The first of these sockets contains UT60, a utility program. The second is available for expansion. A one-page (256-byte) RAM for use by either the utility program or the user program and an interface for Microterminal CDP18S021 are included.

The four control switches, labeled RESET, RUN P, RUN U, and STEP/CONT, enable the operator of the CDP18S691 Prototyping System to clear the system and hold it in the reset state, to initialize and start the user program at address 0000_{16}, to initialize and start the utility program at address 8000_{16}, or to operate the system in either the single-step mode or in the continuous mode. The STEP/CONT switch may also be used as a manual pause during program operation. The single-step mode permits execution of a single machine cycle for each pressing of the RUN U or RUN P switch.

The six-digit hexadecimal display utilizes four of the digits for current memory address and two for current data bus content. The six LED indicators provide machine status information. By means of these facilities, the operator can observe on the six-digit hexadecimal display the address and data sequences of both the fetch and the execute cycles.

The ROM-based Utility Program UT60 operates through any standard data terminal (EIA RS232C or 20-milliampere loop) to allow the user to monitor and alter the contents of memory and to start execution at any address. Operating details for the UT60 are given in a subsequent section.

The **chassis** provided with the CDP18S691 Prototyping System can accommodate three Microboard modules in addition to the CDP18S601 and CDP18S640 supplied with the System. Because the chassis utilizes the RCA COSMAC Microboard Universal Backplane (See Table I for the Backplane Connector Pin List), the Prototyping System can be readily expanded with any of the Microboard Milliwatt Computer System Modules or with a user-designed module, as needed. One side of the backplane has gold-plated edge fingers to assure positive continuous electrical contact. The other side has solder pads on which an edge-connector socket may be mounted. Access holes for the cable connections are provided in the chassis base. In addition, rubber feet are provided, as well as holes for vertical mounting.

The **CDP18S023 Power Converter** is a convenient, compact power supply that plugs into any standard 110-volt 60-Hz wall outlet. It has a regulated output of +5 volts dc ±5% at 600 milliamperes, thus providing enough reserve power to operate additional Microboard Memory or other 5-volt expansion modules. The CDP18S023 can operate the 20 milliampere loop interface and 5-volt ROM's such as the CDP1834, the 2758, or the 2716. Provision is made for the addition of two auxiliary voltages. Backplane pins 11 and 20 are for a negative and a positive voltage, respectively. For example, +12 volts and −5 volts on these terminals allow the use of 2708 EPROM's as well as the RS232C interface. The provision of +15 volts and −15 volts would allow the use of analog circuits as well as the RS232C interface.

The **CDP18S659 Microboard Breadboard**, supplied with the Prototyping System, is a blank module designed to mate with the Microboard Universal Backplane Connector. It provides the user with a convenient means for expansion flexibility and custom design.

CDP18S691

Utility Program UT60

The Utility Program UT60 is designed to examine memory, alter memory, and begin program execution at a specified location. These functions are accomplished through a series of commands initiated by a (?), (!), or ($). The functions described include memory insert (!M), memory display (?M), memory move ($M), memory fill ($F), memory substitute (!S), and run program ($P). The move and fill functions can also be called by user programs.

The UT60 includes read and type routines which provide communication with the user terminal. A "software UART" is provided which uses the Q and EF4 lines for output and input, respectively. The timing constant and duplex mode are determined when the utilities are entered from reset. Once the system has been RESET, the user can either press RUN P to begin program execution at location 0000_{16}, or press RUN U to begin execution of UT60 at location 8000_{16}. After pressing RUN U, the user enters either a CR (carriage return) or LF (line feed). A (CR) will establish full-duplex operation and a (LF) half-duplex operation and, at the same time, calculate the time constant to match the baud rate of the data terminal. Acceptable baud rates are 110, 300, or 1200.

The UT60 also includes user-callable routines which help to simplify user programming. These routines provide register initialization, variable delays, text output, and subroutine call and return.

Some debugging capability is provided by a register-save operation. After RESET and RUN U are pressed, the contents of the CPU registers are saved in RAM beginning at location $8C00_{16}$. The contents of R0, R1, and R4.1 are lost, however, by the process. The CPU register contents can be examined by displaying memory (see ?M command below) beginning at $8C00_{16}$ for 20_{16} bytes.

When UT60 is ready to accept commands, it types out an asterisk (*) as a user prompt. The commands described below may then be entered. Where addresses are specified, leading zeroes are assumed, and if more than four digits are entered, only the last four are retained. In all cases, a command is terminated by a carriage return (CR). If a syntactical error is detected during the entry of a command, UT60 will respond with a (?) and re-prompt the user with an asterisk (*).

UT60 Commands

?M Commands

Name: Memory Display

Purpose: To allow a specified area of memory to be displayed on the user terminal.

Format: ?M(START ADDR)(OPTION)(CR)

Action: The contents of memory, beginning at the specified (START ADDR) will be transmitted to the user terminal. (OPTION) allows the transmission of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. If the option is not specified, a default value of 1 byte is permitted.

Examples: ?M2F8 8(CR)
?M2F8-02FF(CR)
Both of these examples produce the same output.

!M Commands

Name: Memory Insert

Purpose: To alter the contents of memory beginning at the specified address.

Format: !M (START ADDR)(SPACE) (DATA)[(CONT)](CR)

Action: A memory location is accessed at the specified (START ADDR). The (DATA) required is one byte specified by two hex digits. The (CONT) option allows data to be continued onto the next line on the terminal with or without changing the current memory address. A (COMMA) will not change the address and after the user inserts (CR)(LF), additional data may be entered. If a (SEMICOLON) is entered and after a user-inserted (CR)(LF), a new address is anticipated. The semicolon allows non-contiguous memory to be loaded with a single insert command. The command may be terminated at any point by the entry of a (CR) not preceded by a (COMMA) or (SEMICOLON).

Examples: !M02F8 7100F840B0F88CB1(CR)

!M02F8 7100F840,(CR)(LF)
B0F8,(CR)(LF)
8CB1(CR)

!M02F8 7100F840B0;(CR)(LF)
03B6 94FB903A0F(CR)
The first and second examples give identical results. The second provides improved readability at the data terminal output. The third example enters data into two memory areas, starting at 02F8 and 03B6.

$M Commands

Name: Memory Move

Purpose: To move a block of data from one area of memory to another area.

Format: $M(SOURCE ADDR)(OPTION) (SPACE)(DEST ADDR)(CR)

Action: Data is copied from memory location beginning at the (SOURCE ADDR) into locations specified by the (DEST

ADDR). (OPTION) allows the transfer of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen. There is no restriction on the direction of the move and the areas may overlap.

Examples: $M02F8 8 03F8(CR)

$M02F8-02FF 03F8(CR)

$M03B0-03BF 02B0(CR)

$M03B0-03BF 03B2(CR)

$F Commands

Name: Memory Fill

Purpose: To load a defined area of memory with a specified constant.

Format: $F(START ADDR)(OPTION)(SPACE)(DATA)(CR)

Action: The specified (DATA) is loaded into memory beginning at the (START ADDR). (OPTION) allows the loading of either a specific number of bytes preceded by a space or an inclusive address range preceded by a hyphen.

Examples: $F02F8 8 00(CR)

$F02F8-02FF 00(CR)

These examples fill with zeros the eight bytes beginning at location 02F8.

!S Commands

Name: Memory Substitute

Purpose: To display and, if desired, alter the contents of sequential memory locations beginning at the specified address.

Format: !S(START ADDR)(OPTION)(CR)

Action: A memory location is accessed at the specified (START ADDR). Its contents will not be displayed, however, until (OPTIONS) is entered. (OPTIONS) allows two methods of display. If (SPACE) is entered, the current data will be displayed on the same line followed by a hyphen. New data may be entered at this point. Only the last byte entered will be written. If no data is entered, the current data will remain unchanged. If a (LF) is entered, a (CR)(LF) will result and the current memory address will be echoed to the terminal prior to the printing of the current data. New data may be entered as described above. The command can be terminated by a (CR) or continued by the entry of any number of (OPTIONS).

Examples: !S02F8 63-71 00- 0F-C0(CR)

The current data of 63 is changed to 71. The 00 data is retained, and the 0F is changed to C0.

!S02F8 71- 00- C0- 11-82(LF)
02FC 52-AE(LF)
02FD 00-F8 11-40 23-A3(CR)

In this example, the 71, 00, and C0 are retained and the 11 is changed to 82. Each (LF) causes the next address to be typed followed by its data.

$P Commands

Name: Program Run

Purpose: To allow a user program to be run beginning at the specified address.

Format: $P[(START ADDR)](CR)

Action: The user program will begin execution at the specified (START ADDR) with P = 0 and X = 0. If the (START ADDR) is not specified, the default value is 0000_{16}.

Specifications

System Contents

CDP18S601 Microboard Computer
CDP18S640 Microboard Control and Display Module
CDP18S675 Microboard 5-Card Chassis
CDP18S023 Power Converter
CDP18S659 Microboard Breadboard
Cable for TTY terminal (20 mA loop)
Cable for RS232C terminal
Flat cable and connector for parallel I/O, 34 pin
Two-part metal case
ROM-based utility software (UT60)
Technical literature

RAM

4 kilobytes on CDP18S601
256 bytes on CDP18S640

ROM

4 sockets for up to 8 kilobytes on CDP18S601
1 kilobyte preprogrammed with UT60 on CDP18S640

Parallel I/O

20 lines, programmable
4 external flag inputs
1 Q line output

CDP18S691

Serial I/O
RS232C or 20 mA loop, software driven, automatic baud rate selection of 110, 300, or 1200.

Interface Option
CDP18S021 Microterminal, hand held, low cost.

Control Switches
RESET—Clears system and holds it in reset state
RUN P—Initializes system and starts program execution at 0000_{16}
RUN U—Initializes system and starts program execution at 8000_{16}.
STEP/CONT—In step position, allows execution of a single machine cycle upon depression of RUN P. May be used as manual pause during program execution.

Displays
4 hex digits for address
2 hex digits for data
6 discrete LED's for status:
S 0 , S 1 = State code
Q = Programmable latched output
WT, CLR = Machine mode indicators
RUN = Machine running, not at idle, not reset

Table I—Pin Terminals and Signals for the RCA COSMAC Universal Backplane Connector (P1)

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
A	TPA-P	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P	In/Out	Data Bus	4	INT-P	In	Interrupt Request
E	DB2-P	In/Out	Data Bus	5	MRD-N	Out	Memory Read
F	DB3-P	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P	In/Out	Data Bus	9	CLEAR-N	In	Clear-Mode Request
L	DB7-P	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	−5V/−15V	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N	In	External Flag
X	EF4-N	In	External Flag	20	+12V/+15V	—	Auxiliary Power
Y	+5V	In	+5 volts dc	21	+5V	In	+5 volts dc
Z	GND	In	Digital Ground	22	GND	In	Digital Ground

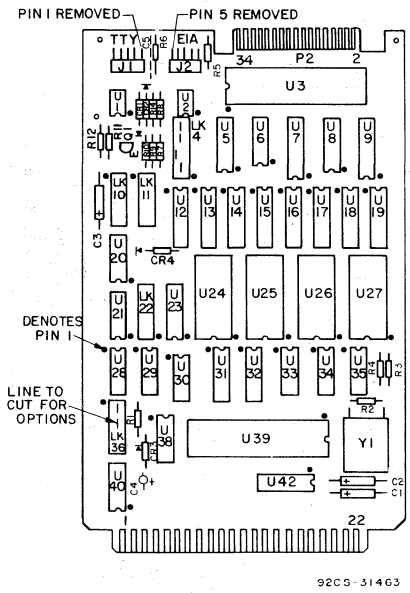
Microboard Computer 20-mA Serial Interface (J1)

Pin	Signal	Pin	Signal
1	VACANT (KEY)	6	NC
2	NC	7	DATA OUT SOURCE
3	DATA OUT RETURN	8	DATA IN SOURCE
4	DATA IN RETURN	9	NC
5	NC	10	NC

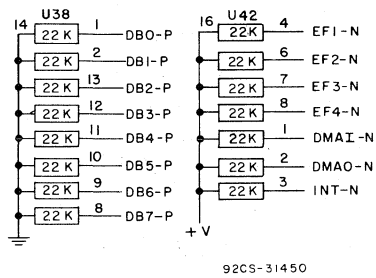
Microboard Computer EIA RS232C Serial Interface (J2)

Pin	Signal	Pin	Signal
1	GND	6	HIGH LEVEL
2	DATA IN	7	HIGH LEVEL
3	DATA OUT	8	HIGH LEVEL
4	NC	9	NC
5	VACANT (KEY)	10	GND

CDP18S691



Layout diagram of RCA COSMAC Microboard Computer CDP18S601.



Pull-down and pull-up resistors.

CDP18S601 Parts List

C1, C2, C3=15μF, 20 V
C4=1.5 μF, 35 V

CR1, CR2, CR3, CR4=1N270

J1, J2=connector, right angle (mates with connector comprised of housing - AMP 1-86148-2, contact - AMP 86016-1, keying plug - AMP 87077-1, or equivalent)

Q1=2N5139

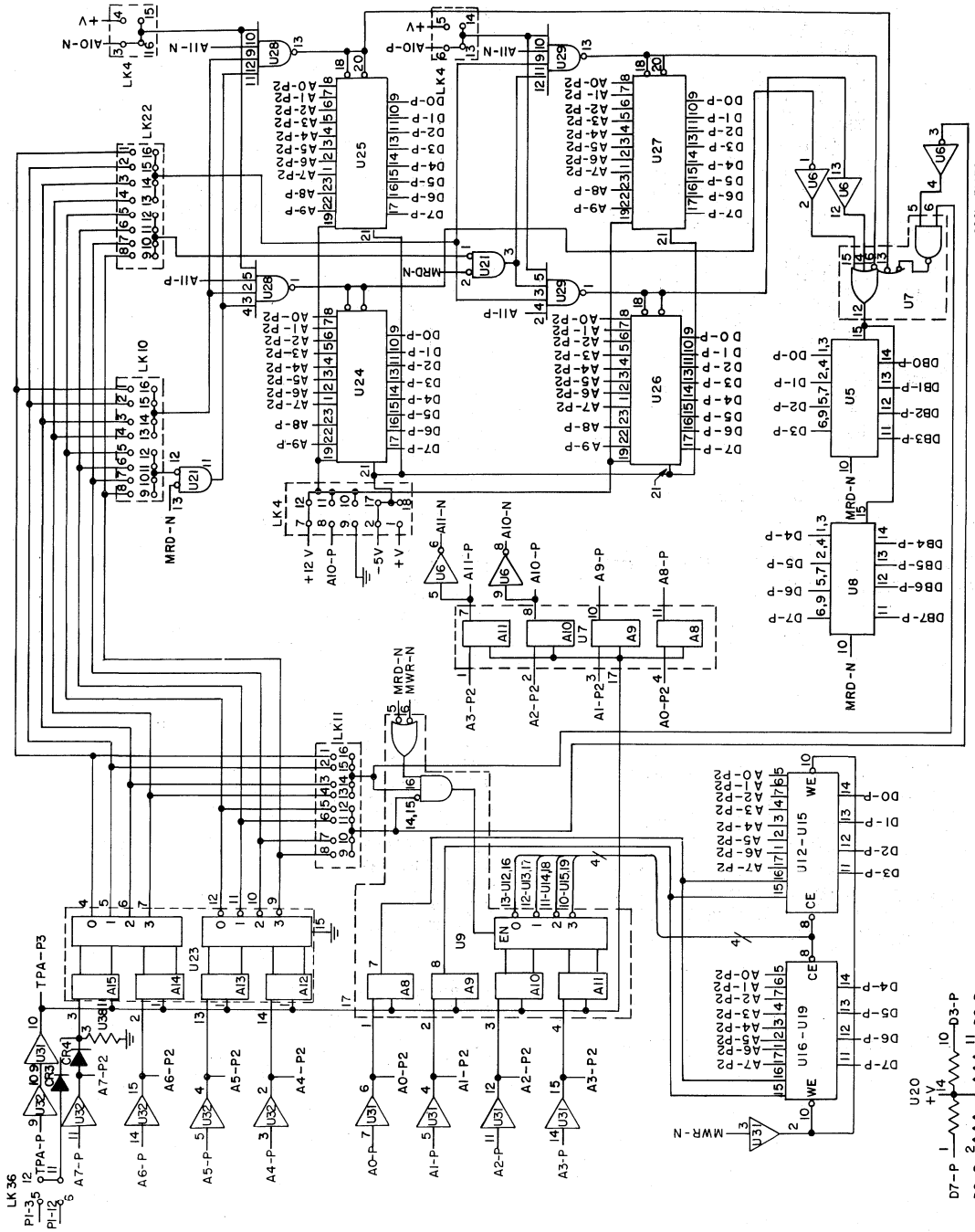
R1=100 kΩ, ¼ W, 5%
R2=22 MΩ, ¼ W, 5%
R3, R4,=22 kΩ, ¼ W, 5%
R5=3 kΩ, ¼ W, 5%
R6, R14=1 kΩ, ¼ W, 5%
R7=11 kΩ, ¼ W, 5%
R8=4.3 kΩ, ¼ W 5%
R9=130 Ω, ¼ W, 5%
R10=10 kΩ, ¼ W, 5%
R11=2.7 kΩ, ¼ W, 5%
R12=220 Ω, ¼ W, 5%

U1=CA3160
U2=CA3140
U3=CDP1851CE
U5, U8=CDP1856CE
U6=CD4069BE
U7=CDP1867CE
U9=CDP1866CE
U12-U19=MWS5114E-5
U20, U38=resistor module, 22 kΩ, 14 pin
U21=CD4001BE
U23=CDP1858CE
U28, U29=CD4012BE
U30=CD4016BE
U31, U32=CD4050BE
U33=CD4025BE
U34=CD4013BE
U35=CD4023BE
U39=CDP1802CE
U40=CD4093BE
U42=resistor module, 22 kΩ, 16 pin

XU24-XU27=24-pin socket
XU39=40-pin socket

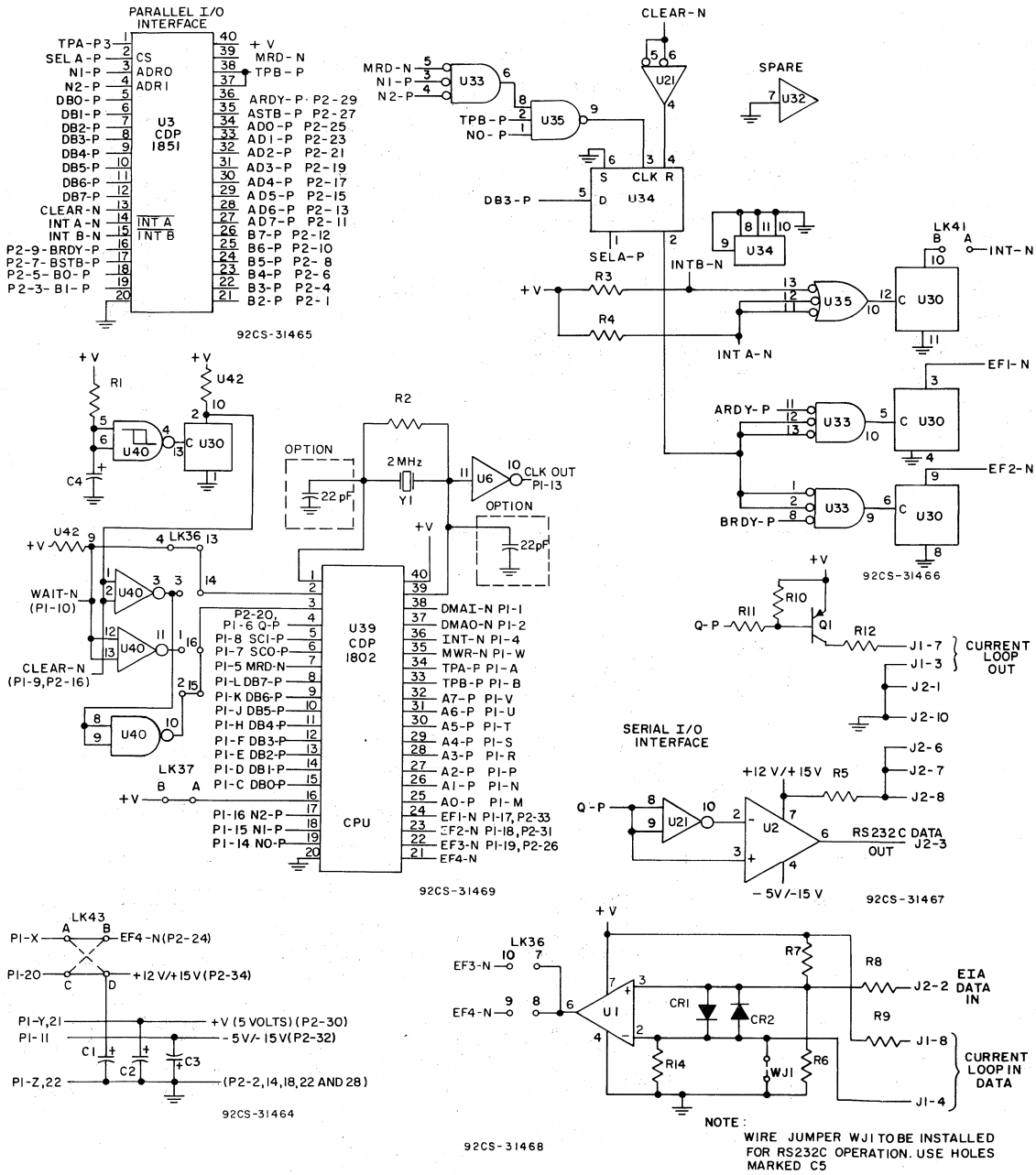
Y1=2.00-MHz crystal

CDP18S691



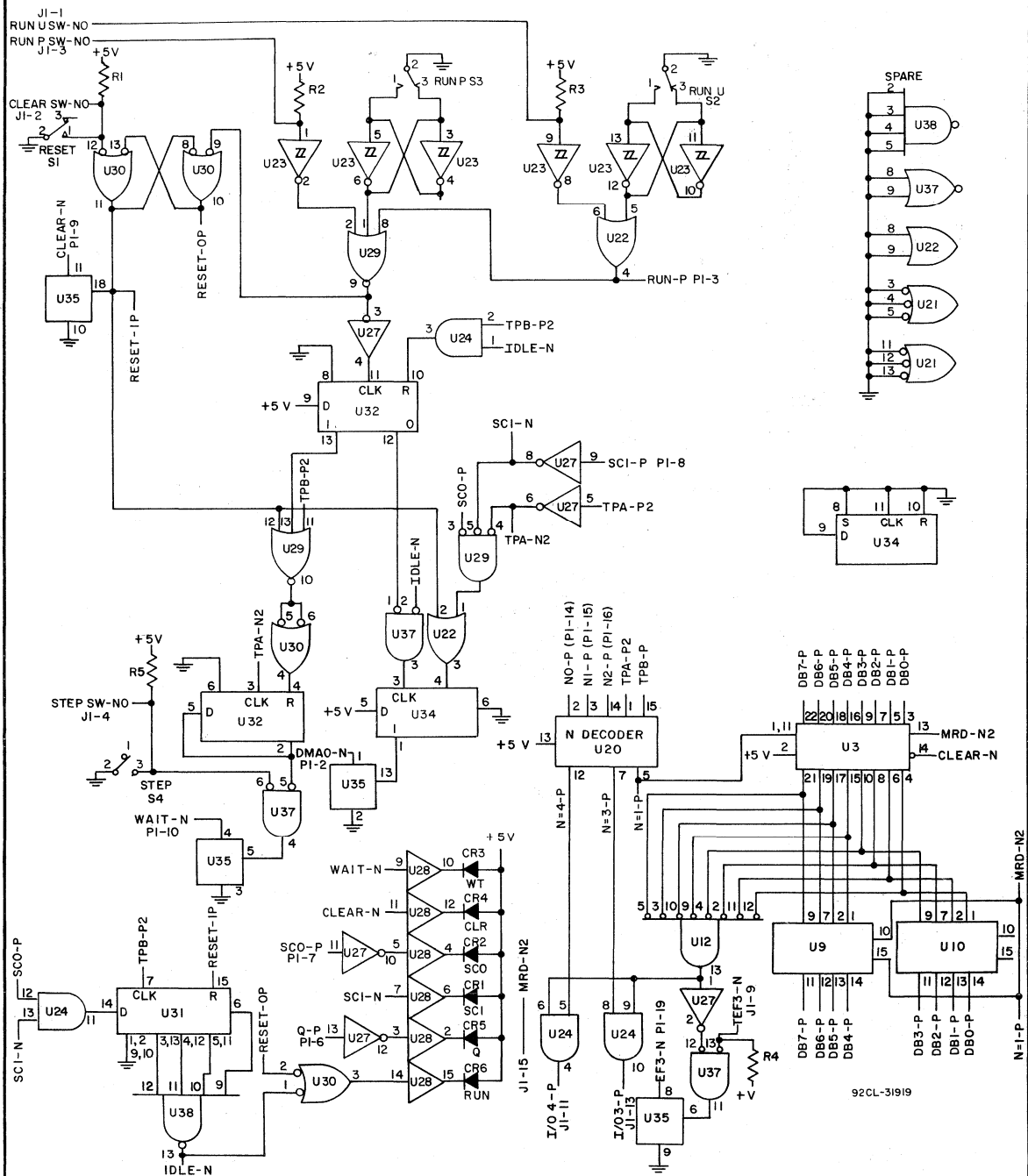
Logic diagram of Microboard Computer CDP18S601 - memory portions.

CDP18S691



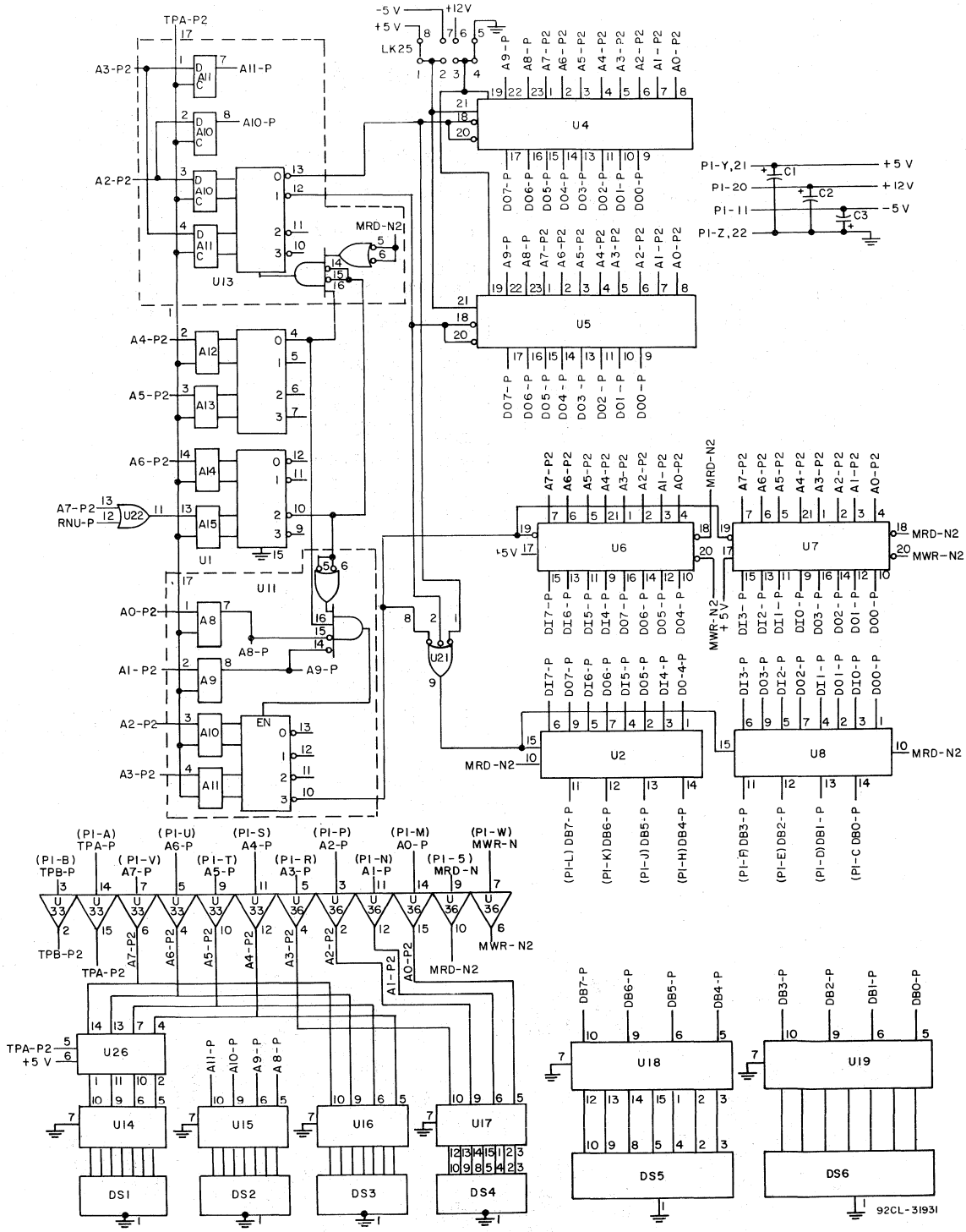
Logic diagram of Microboard Computer CDP18S601 - CPU and interface portions.

CDP18S691



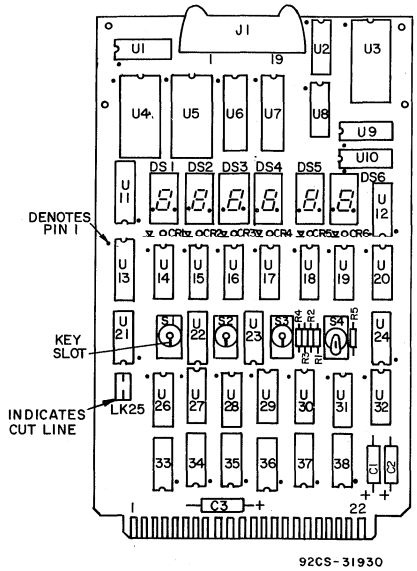
Logic diagram of Microboard Control and Display Module CDP18S640 - control and status indicator portion.

CDP18S691



Logic diagram of Microboard Control and Display Module CDP18S640 - memory and memory display portion.

CDP18S691



Layout diagram of RCA COSMAC Microboard Computer CDP18S640.

Microterminal CDP18S021 Connections on Microboard Control and Display Module CDP18S640 (J1)

Pin	Signal	Pin	Signal
1	RUN U-N0	2	CLEAR-N0
3	RUN P-N0	4	STEP-N0
5	V_{LED}	6	DB0-P
7	V_{CC}	8	DB1-P
9	TEF3-N	10	DB2-P
11	IO4-P	12	DB3-P
13	IO3-P	14	DB4-P
15	MRD-N	16	DB5-P
17	TPB-P2	18	DB6-P
19	GND	20	DB7-P

CDP18S640
Parts List

C1, C2, C3 = 15 μF, 20 V

CR1 – CR6 = LED

DS1 – DS6 = 7-segment display

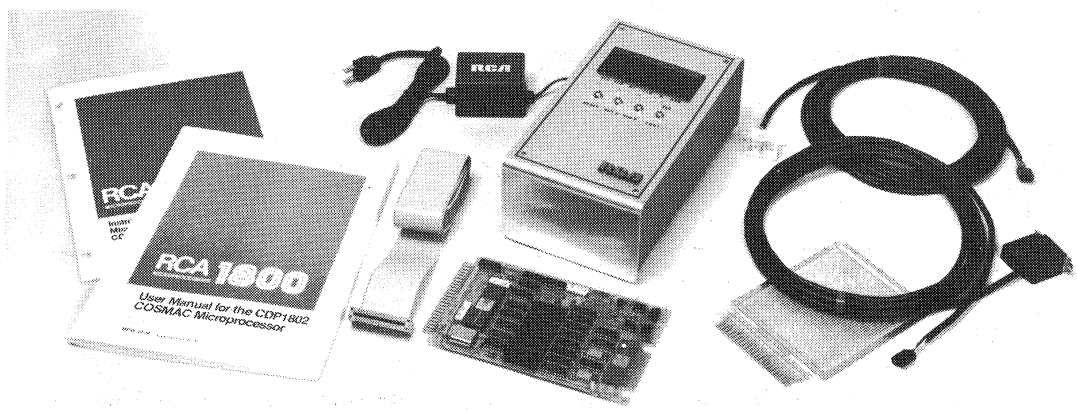
J1 = connector, 20 pin

R1 – R5 = 22 k, ¼ W, 5%

S1, S2, S3 = switch, momentary
S4 = switch, SPDT

U1 = CDP1858CE
U2, U8 = CDP1856CE
U3 = CDP1852CE
U6, U7 = MWS5101EL-3
U9, U10 = CDP1857CE
U11, U13 = CDP1866CE
U12 = CD4078BE
U14-U19 = MC14495P
U20 = CDP1853CE
U21 = CD4023BE
U22 = CD4071BE
U23 = CD40106BE
U24 = CD4081BE
U26 = CD4042BE
U27 = CD4069BE
U28, U33, U36 = CD4050BE
U29 = CD4025BE
U30 = CD4011BE
U31 = CD4076BE
U32, U34 = CD4013BE
U35 = CD4016BE
U37 = CD4001BE
U38 = CD4012BE

XDS – XDS6 = DIP socket, 10 pin
XU4, XU5 = IC socket, 24 pin



CDP18S692
Advance Data

RCA COSMAC Microboard Prototyping System

Features

- Low-power static CMOS
- COSMAC Microprocessor architecture
- High noise immunity
- Simple to use
- Easy to expand or modify
- Selectable serial interface — RS232C or 20-mA loop
- Temperature range: 0° to 70°C
- 65,536-byte memory address range
- Power-on reset
- All I/O lines on edge connectors
- Microterminal interface
- UART with selectable baud rate
- Uses COSMAC Microboard Universal Backplane
- CDP18S602 Microboard Computer
- CDP18S640 Control/Display Module
- Five-card chassis — expandable
- Protective metal case
- Four control switches
- Six hexadecimal display digits
- Six LED status indicators
- ROM-based monitor software (UT61)
- Selectable clock frequency
- Sockets for 1/2/4/8-kilobyte ROM/PROM
- 2-kilobyte read/write memory
- Includes +5-volt power supply

The RCA COSMAC Microboard Prototyping System CDP18S692 is a fully assembled package that includes the hardware, a ROM-based utility program, and the technical literature needed to enable the user to design a microcomputer system. It provides a quick, inexpensive way to investigate and evaluate the Microboard family of components, to train personnel in microprocessor usage, and to develop computer systems for custom applications. It has two kilobytes of read/write memory and provides for the addition of 1/2/4/8-kilobytes of mask-programmed ROM or EPROM, depending on the application requirements. It needs only a data terminal to become immediately operational.

The CDP18S692 Prototyping System includes a CDP18S602 Microboard Computer to provide the complete computer function, the CDP18S640 Microboard Control and Display Module to provide the switches and the displays for prototyping operation, the CDP18S675 5-Card Chassis containing the preprinted Universal Backplane for all five card positions, the CDP18S023 Power Converter, the CDP18S659 Microboard Breadboard for expansion flexibility, the UT61 ROM-based utility program, technical literature, a protective metal case of functional design, and the required cabling.

The RCA COSMAC Microboard Prototyping System CDP18S692 is the same as the CDP18S691 Prototyping System except that the CDP18S692 uses the CDP18S602 Microboard Computer. All other components are the same. For additional information refer to the data for the CDP18S602, the CDP18S640, and the CDP18S691.

COSMAC Microprocessor Support and Development Systems

Technical Data

Features and Functional Classifications

The RCA CDP18S series of COSMAC microprocessor development and support systems include an extensive line of hardware, software, and accessory items. This series offers the following basic features:

- Full spectrum of design aids, including software, hardware, support, and literature
- Low-cost systems for complete system design and debugging functions
- Readily available hardware and software applications support
- "Graduated steps" to microprocessor design
- Complete series of technical manuals and other literature that provide detailed explanations of the operation and use of various hardware and software systems.

RCA's approach in the development of the CDP18S-series hardware and software has been "graduated steps to microprocessing." With respect to both function and dollar investment, the user is given logical steps that help him progress from a learning stage on through integral hardware/software system prototyping. And for each step, he is provided with an appropriate tool, as shown in the chart below.

CDP18S-Series COSMAC Microprocessor Development and Support Systems (Key Products)

Type No.	Descriptive Title	Function
CDP18S012	COSMAC Microtutor	To learn about programming and microprocessors
CDP18S005 CDP18S007	COSMAC Development System II COSMAC DOS Development System (CDS III)	For complete hardware and software system development
CDP18S805	Floppy Disk System	For high-speed program development
CDP18S020 CDP18S024	COSMAC Evaluation Kit EK/Assembler-Editor Kit	Complete system for machine-language programming and prototyping
CDP18S021	COSMAC Microterminal	Low-cost alternative for TTY, CRT, or other terminals in a CDP1800-series microprocessor-based system
CDP18S023	Power Supply	Lightweight inexpensive system power supply
CDP18S025	Evaluation Kit, Microterminal, and Power Supply	Combination package—unassembled
CDP18S030	COSMAC Micromonitor	For in-circuit real-time hardware and software debugging
CDP18S831	Micromonitor Operating System (MOPS)	Optional package for operating Micromonitor with disk files
CDP18S826 CDP18S827	Fixed-Point Arithmetic Package Floating-Point Arithmetic Package	To ease programming of often used routines
CDP18S834	Basic 1 Compiler/Interpreter	To simplify program development
CDP18S837	CDOS Upgrade Package (to CDS III)	Adds disk file management to disk-based development systems

As guidance for choosing appropriate equipment for your specific needs, the following are some suggested RCA Development Systems configurations:

Development System (CDP18S005 and CDP18S5030)
This development system configuration provides an economical tape-based system complete with resident assembler/editor for assembly language software development as well as prototype system real-time hardware and software dubugging capability.

Disk-Based Development System (CDP18S007, CDP18S030, and CDP18S831)
The CDP18S007 is a complete floppy-disk-based development system featuring a development system chassis with 28K bytes of RAM, and a dual-drive floppy disk system for mass memory storage. Its software includes a disk-based editor, a Level II Macroassembler, utility program, and a new disk operating system (CDOS) which provides the user with a powerful disk file-management system.

The Micromonitor and MOPS offer complete hardware and software debug capability for prototype as well as programmable automated production testing.

Add-on to CDP18S005 Development System (CDP18S805 and CDP18S837)
For those already having the COSMAC Development System CDP18S005, RCA offers the ability to enhance the system to a complete disk-based development system having disk-operating-system capability by the addition of the RCA Floppy Disk System (CDP18S805) and CDOS Upgrade Package (CDP18S837). These enhancements provide mass memory storage and disk-file-management software essential for facilitation of program development with any of the RCA disk-based high level languages.

CDP18S005, CDP18S007, CDP18S007V3

COSMAC DOS Development System and COSMAC Development System II

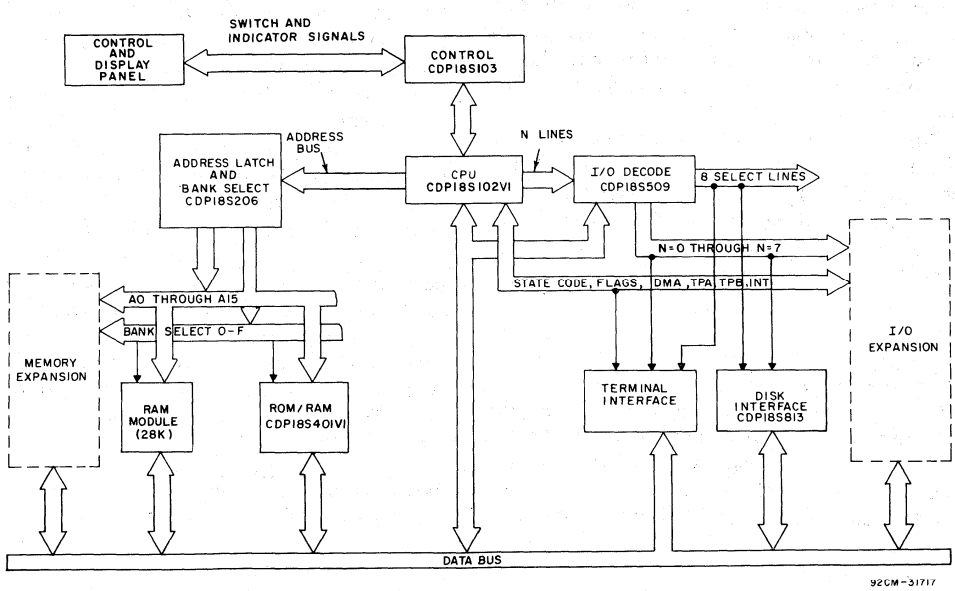
The COSMAC Development Systems are a family of support aids designed to facilitate the development of hardware and software for products based on the RCA-1800 series of CMOS microprocessor devices. The COSMAC Development Systems offer a wide range of cost/performance features from a minimum tape-based system (CDS II - CDP18S005) to a full developmental system having floppy disk mass-memory storage and operating system software (CDS III - CDP18S007V1,V3). The systems have many common features so that upgrading from CDS II to CDS III is easily accomplished by means of Upgrade Package CDP18S837. Because the systems use a plug-in-card architecture providing space for additional I/O devices, they are convenient to use for hardware prototyping. A series of CDS modules, as well as the Microboard CDP18S600-series, is available for system expansion and prototyping. Various levels of software support, including resident editors, assemblers, and operating systems are also available to speed program development.

Features Common to All Three Systems

The COSMAC Development Systems are comprised of the following common elements:

- A 19-inch rack-mountable chassis with printed-circuit backplane
- Internal power supplies, clock, and controls
- A front panel with controls and display
- Plug-in printed-circuit modules including: CPU, Address Latch and Bank Select, RAM, ROM, I/O Decoder, and Terminal Interface Modules
- Blue metal case easily removable with four screws
- Resident ROM-based utility program

The CDS (see block diagram), designed for flexibility and expansion, provides PC module positions for spare memory and spare I/O. Extra memory and optional I/O modules are available, or the user may design and add his own. The RCA CDP18S600 Microboard series is compatible with the CDS backplane so that this broad



Block diagram of CDS Central Processor for the CDP18S007.

CDP18S005, CDP18S007, CDP18S007V3

selection of memory, I/O, and computer boards can be used for customization of the CDS.

Provision is made for two-level I/O in the systems so that I/O instructions normally reserved for CDS interfaces can be freed for user functions. I/O selection is under user program control.

Backplane wirewrapping permits easy reconfiguration to meet a particular system requirement. As delivered, the CDS is completely assembled and needs only the addition of a data terminal to become operational.

Interfacing for both 20-mA current loop and EIA RS232C terminals is standard so that a wide variety of terminals can be used with the CDS. Data terminals are handled by the CDP18S007 (CDS III) via a UART Interface Module CDP18S508 having switch-selectable baud rates of 110, 300, 1200, 4800, 9600, or 19,200 baud with full- or half-duplex operation. In the CDP18S005 (CDS II), data terminals are handled via a Terminal Interface Module CDP18S507 having automatically adjustable baud rates of 110, 300, and 1200 baud with full- or half-duplex operation.

A ROM-based **System Utility** program allows the user to inspect and modify memory and start program execution at any location. When the Utility Program is started, it stores 13½ of the CPU's registers in its dedicated RAM from which the registers can subsequently be printed out. For debugging purposes, the CDS provides a single-step mode and a front-panel display showing current memory address and either the data bus or the last data byte transferred as the result of an I/O instruction. In addition, a full monitor facility may be provided by the optional Micromonitor CDP18S030.

The Utility Program also provides various user-callable routines including disk and terminal I/O routines. In the CDS III various parameters (such as the presence or absence of parity) initialized by the Utility Program can be changed under software control to meet specific applications requirements.

System Description

The COSMAC Development Systems differ principally in the amount of RAM supplied and in the type of software support. Following is a brief description of the special features of each system. The preceding section gave the features common to all three systems.

CDP18S005 - COSMAC Development System II (CDS II)

This system contains 4 kilobytes of static CMOS RAM and comes with a resident editor and Level-I assembler on paper tape (for operation on a Teletype* terminal) and on magnetic cassette (for operation on a TI Silent 700** terminal). The 4-kilobyte RAM supplied is sufficient to hold the Resident Editor program and provide a working buffer of about 1 kilobyte or to hold the Resident Assembler with storage for about 100 labels. Either program will automatically make use of any user-added memory.

The CDS II can be upgraded to the CDS III by the addition of (1) a floppy disk system CDP18S805, (2) eight or more kilobytes of RAM such as two CDP18S620 Microboard 4-Kilobyte RAM's, and (3) Upgrade Package CDP18S837. As an intermediate expedient to relieve the user of the burdens of paper-tape or cassette media, the floppy disk system CDP18S805 only can be added. With this expedient, however, the diskette files must be kept track of manually by track number.

CDP18S007 - COSMAC DOS Development System

The COSMAC DOS Development System is the most powerful system of the series. It includes a CDS Central Processor containing 28 kilobytes of user-accessible RAM, a single-density dual-drive floppy-disk system, and a companion CDOS disk operating system. The additional system software includes an editor, a Level-II macroassembler, and various diskette utility programs.

Program development is considerably facilitated by the CDOS disk-file management and operating system. Because CDOS references files by file name rather than by track number, the user is provided rapid access to the files and need not be concerned about file size or disk space allocation. Assembler outputs can be directed to a disk file or to a line printer, if one is available, with symbol table and references either added or suppressed.

Versions for both domestic and overseas operation are available. Model CDP18S007V1 operates on 115 volts, 60 Hz; model CDP18S007V3 operates on 220 volts, 50 Hz.

*Registered trademark, Teletype Corp.

**Registered trademark, Texas Instrument Corp.

Upgrade Options

Floppy Disk System CDP18S805. This system consists of a single-density, dual-drive floppy-disk mechanism plus an interface module that plugs into the CDS chassis. It is supplied as part of the CDS III (CDP18S007) system, but can be ordered separately to upgrade a CDP18S005. When ordered separately, the CDP18S805 is supplied with disk-based versions of the resident editor and various assemblers (including a macro assembler) and with various utility programs. These programs are non-CDOS versions of the software and require the user to keep file records by track number assignments. It is to the user's advantage to order an additional 8 kilobytes of RAM along with this system to be able to take full advantage of the software supplied. For a full upgrade to a CDS III system (CDP18S007), the user should order a Floppy Disk System CDP18S805, 8 kilobytes of additional RAM, and the Upgrade Package CDP18S837. (Part number: CDP18S805V1 for 115-volt, 60-Hz operation; CDP18S805V3 for 220-volt, 50-Hz operation; product description: PD17; instruction manual: MPM-217)

Upgrade Package CDP18S837. This package contains hardware, firmware, and software needed to upgrade a CDS II (CDP18S005) equipped with a floppy disk system and a minimum of 12 kilobytes of RAM to a CDS III (CDP18S007). The Package includes 16-kilobytes of static CMOS RAM, a UART terminal interface module, a replacement PROM for the Utility Program, a CDOS system diskette, and appropriate instruction manuals. (Part number: CDP18S837; product description: PD37)

Optional Accessories

COSMAC Micromonitor CDP18S030. The Micromonitor, a powerful self-contained debugging tool, may be used to considerable advantage with the COSMAC Development Systems. It permits in-circuit debugging in real time of both hardware and software. The Micromonitor includes a built-in 28-key keyboard with an 8-digit LED display, 14 status indicator lights, and software debugging routines. It significantly increases the speed with which hardware and software can be integrated and software debugged. It is specifically recommended for the development of programs of more than one kilobyte in length. (Part number: CDP18S030; product description: PD18; instruction manual: MPM-218)

PROM Programmer CDP18S480. This hardware/software package when installed in the CDS enables the user to program Intel 2704, 2708, 2758, 2716, or equivalent PROM's. In addition, it will read, but not program, 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's. The software is available on disk, paper tape, and magnetic tape in cassette. (Part number: CDP18S480 -disk version, CDP18S480V1 - paper-tape version, CDP18S480V2 - cassette version; product description: PD22; instruction manual: MPM-222)

Optional Software

Basic 1 Compiler/Interpreter CDP18S834. This high-level language supplied on a diskette is designed to facilitate rapid program development with the COSMAC CDOS Development Systems (CDS III) CDP18S007 V1 and V3. Basic 1 is an easily learned language for the beginning programmer and may be extended indefinitely by the addition of machine language routines. (Part number: CDP18S834; product description: PD34; instruction manual: MPM-234)

Binary Fixed-Point Arithmetic Subroutines CDP18S826. This software package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines including addition, subtraction, multiplication, and division. Also included are binary-to-BCD and BCD-to-binary conversion subroutines plus various utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number: CDP18S826 - disk version, CDP18S826V1 - paper-tape version, CDP18S826V2 - cassette version; product description: PD6; instruction manual: MPM-206)

Binary Floating-Point Arithmetic Subroutines CDP18S827. This software package is a set of 32-bit floating-point arithmetic subroutines including addition, subtraction, multiplication, division, sine, cosine, arctan, natural log, e^x, and square root. Also included are binary-to-BCD and BCD-to-binary conversion plus other utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number: CDP18S827 - disk version, CDP18S827V1 -paper-tape version, CDP18S827V2 - cassette version; product description: PD7; instruction manual: MPM-207)

CDP18S005, CDP18S007, CDP18S007V3

COSMAC Micromonitor Operating System (MOPS) CDP18S831. This software package enhances the capabilities of the Micromonitor by providing interfacing to disk files. MOPS provides the user with such options as saving the state of the CPU for subsequent reloading and driving the Micromonitor with commands from a disk file to perform automated testing. (Part number: CDP18S831; product description: PD31; instruction manual: MPM-231)

Literature

Supplied with CDP18S005:

MPM-216 - Operator Manual for the RCA COSMAC Development System II CDP18S005
MPM-201 - User Manual for the CDP1802 COSMAC Microprocessor

Supplied with CDP18S007:

MPM-232 - Operator Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007
MPM-233 - Hardware Reference Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007
MPM-201 - User Manual for the CDP1802 COSMAC Microprocessor

Supplied with Available Options:

MPM-206 - Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-207 - Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-217 - RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual
MPM-218 - Instruction Manual for the RCA COSMAC Micromonitor CDP18S030
MPM-222 - Operator's Manual for PROM Programmer CDP18S480
MPM-223 - Instruction Guide for the COSMAC Macro Assembler (CMAC)
MPM-231 - Micromonitor Operating System (MOPS) CDP18S831 Users' Guide
MPM-234 - Use of Basic 1 Compiler/Interpreter CDP18S834 with the COSMAC CDOS Development System (CDS III)
PD37 - COSMAC Disk Operating System Upgrade Package CDP18S837

Specifications for CDP18S007V1 and V3 (CDS III)

CDS Central Processor

Dimensions (with case):
Rack Mountable
Width 19-3/8 inches (492 mm)
Depth 12-3/4 inches (324 mm)
Height 5-3/4 inches (146 mm)
Weight 27 lbs. (approx.) (12.2 kg.)

Front Panel:
Controls:
Power ON/OFF
Reset
Run Program
Run Utility
Load
Single Step or Continuous
Data Bus or Last I/O Byte Display
Display:
Six Hexadecimal Digits for Memory Address and Data Bus or Last I/O Byte
Six LED Indicators: RUN, Q, SC0, SC1, CLEAR

Power Requirements:
CDP18S007V1 - 100-120 V ac, 60 Hz, 125 W
CDP18S007V3 - 220-240 V ac, 50 Hz, 125 W
Fuse: 1¼ A

Internal Power Supplies:
+5 V dc at 6.0 A, 5% regulation
−5 V dc at 0.5 A, 5% regulation
+12 V dc at 0.5 A, 5% regulation

Operating-Temperature Range:
0° to 43 °C

Cabling Supplied:
AC power cord - 8 feet
Terminal Interface: TTY - 15 feet; 6-wire, terminated in Molex connector
EIA - 15 feet; 6-wire, terminated in 25-pin Cinch connector

CDP18S005, CDP18S007, CDP18S007V3

Module Nest:
Total Slots: 25
Spare I/O slots: 9
Spare memory slots: 4
PC backplane with wire-wrap connections

Module Sizes:
4.5 x 3 in. or 4.5 x 7 in.
(114.3 x 76.2 mm or 114.3 x 177.8 mm)

Connectors:
44-pin; 0.156 in. pin spacing; wire-wrap pins 0.015 x 0.041 in.
0.5 in. connector spacing

Standard Plug-in Modules (supplied):

Function	Part Number
CPU	CDP18S102V1
Address Latch and Bank Select	CDP18S206
Control	CDP18S103
28-Kilobytes of Static CMOS RAM:	
Three 4-Kilobyte RAM's	CDP18S205V1 or CDP18S620 and
One 16-Kilobyte RAM or	CDP18S621
One 4-Kilobyte RAM	CDP18S205V1 or CDP18S620 and
Three 8-Kilobyte RAM's	CDP18S623
UART Interface (Terminal)	CDP18S508
Disk Interface	CDP18S813
I/O Decode	CDP18S509
ROM/RAM	CDP18S401V1
Extender Card	CDP18S502

Optional Modules (available separately):
Byte I/O CDP18S510
UART Interface CDP18S508
Microboard Computer System Modules CDP18S600-series - See Booklet CMB-250

Optional Accessories (available separately):
Micromonitor CDP18S030
PROM Programmer
CDP18S480 (Diskette)
CDP18S480V1 (Paper Tape)
CDP18S480V2 (Cassette)

Terminal Interface:
20 mA or RS232C (EIA)
110, 300, 1200, 4800, 9600, or 19,200 baud Serial ASCII

Word Size:
Data: 8 bits
Address: 16 bits
Instruction: 1, 2, or 3 bytes

Instruction Set:
91 easy-to-use CDP1802 microprocessor instructions

Memory Size:
Up to 65 kilobytes max.
Supplied RAM: 28 kilobytes
Supplied ROM: 2 kilobytes

System Clock:
Crystal Oscillator at 2.5 MHz

Internal Signal Lines:
+5 V, TTL-compatible signal levels
Bidirectional data bus

Dual-Disk Drive Mechanism CDP18S801V1 and CDP18S801V3

Power Requirements:
CDP18S801V1 - 100-120 V ac, 60 Hz, 250 W
CDP18S801V3 - 220-240 V ac, 50 Hz, 250 W

Dimensions:
Length 20-3/4 in. (527 mm)
Height 7-1/4 in. (184 mm)
Width 19-1/4 in. (489 mm)
Weight 75 lbs. (34 kg.) approx.

Cabling Supplied:
AC power cord - 5 feet
CDS interface - 4 feet

Number of Drives:
2

Total System Capacity:
512,512 bytes

Display Lights:
BUSY, CRC ERROR, READY, DRIVE 0, DRIVE 1

Operating Timing:
Seek:
Track to track: 10 ms
Head Load and Settling Time: 40 ms max.
Max. Seek Time: 820 ms
Read/Write:
Sector Read/Write Time: 6 ms
Average Latency: 83 ms

CDP18S005, CDP18S007, CDP18S007V3

Diskette Format:
IBM compatible
77 tracks per diskette
26 sectors per track
128 bytes per sector
256,256 bytes per diskette

System Software:

CDOS Operating System Commands:
List Directory
List Free Space on Disk
Copy Disk File to Terminal, Line Printer, or Another File
Delete File Name
Rename File
Convert ASCII-Hex File to Binary
Copy Pre-CDOS File to CDOS System
Format a New Disk
Verify Disk Files for Match
Save CDS Memory under File Name
Examine Diskette File Contents

Resident Editor Commands:

Move pointer	Save
Delete	Search & Substitute
Append	Type
Insert	Output
Find	

Resident Assembler Operation:
Input: Source files - Level I, II, Macro
Output: Hexadecimal or Listing Files to Disk or Line Printer

Utility Program Commands:
Read or modify memory
Read saved state of 13½ CPU registers
Start Program execution at given location
Load CDOS Operating System

Optional Software:
Binary Arithmetic Subroutine Fixed-Point Package Diskette (CDP18S826)
Binary Arithmetic Subroutine Floating-Point Package Diskette (CDP18S827)
Micromonitor Operating System (MOPS) Diskette (CDP18S831)
Basic 1 Compiler/Interpreter Diskette CDP18S834

Blank Diskettes:
CDP18S829 (one supplied; additional diskettes are available separately)

Specifications for CDP18S005

Dimensions (with case):
Rack Mountable
Width 19-3/8 in. (492 mm)
Depth 12-3/4 in. (324 mm)
Height 5-3/4 in. (146 mm)
Weight 27 lbs. (approx.) (12.2 kg.)

Front Panel:
Controls:
Power ON/OFF
Reset
Run Program
Run Utility
Load
Single Step or Continuous
Data Bus or Last I/O Byte Display
Display:
Six Hexadecimal Digits for Memory Address and Data Bus or Last I/O Byte
Six LED Indicators: RUN, Q, SC0, SC1, WAIT, CLEAR

Power Requirements:
100, 115, 220, 230 or 240 V ac
50/60 Hz, 125 W
Fuse: 1¼ A

Internal Power Supplies:
+5 V dc at 6.0 A, 5% regulation
−5 V dc at 0.5 A, 5% regulation
+12 V dc at 0.5 A, 5% regulation

Operating-Temperature Range:
0° to 43 °C

Cabling Supplied:
AC power cord - 8 feet
Terminal Interface: TTY - 15 feet; 6-wire, terminated in Molex connector
EIA - 15 feet; 6-wire, terminated in 25-pin Cinch connector

Module Nest:
Total slots: 25
Spare I/O slots: 10
Spare memory slots: 7
PC backplane with wire-wrap connections

CDP18S005, CDP18S007, CDP18S007V3

Module Sizes:
4.5 x 3 in. or 4.5 x 7 in.
(114.3 x 76.2 mm or 114.3 x 177.8 mm)

Connectors:
44-pin; 0.156 in. pin spacing; wire-wrap pins 0.015 x 0.041 in.
0.5 in. connector spacing

Standard Plug-in Modules (supplied):

Function	Part Number
CPU	CDP18S102V1
Address Latch and Bank Select	CDP18S206
Control	CDP18S103
4-Kilobyte RAM	CDP18S205V1
I/O Decode	CDP18S509
Terminal Interface	CDP18S507
ROM/RAM	CDP18S401
Extender Card	CDP18S502

Optional Modules (available separately):

Disk Interface	CDP18S813
Byte I/O	CDP18S510
UART Interface	CDP18S508

Microboard Computer System Modules
CDP18S600-series - See Booklet CMB-250

Optional Accessories (available separately):
Floppy-Disk System
CDP18S805V1
100-120 V ac, 60 Hz
CDP18S805V3
220-240 V ac, 50 Hz
Micromonitor CDP18S030
Microterminal CDP18S021
PROM Programmer
CDP18S480 (Diskette)
CDP18S480V1 (Paper Tape)
CDP18S480V2 (Cassette)

Appropriate Terminal (with paper tape or magnetic-tape cassette):
Teletype Terminal with Reader/Punch,
TI "Silent 700", Model 733, with Remote Device Control & Tape Cassette Options
Baud Rates: 110, 300, 1200 baud

Instruction Set:
91 easy-to-use CDP1802 microprocessor instructions

Memory Size:
Up to 65 kilobytes max.
Supplied RAM: 4 kilobytes
Supplied ROM: 2 kilobytes

System Clock:
Crystal Oscillator at 2 MHz

Internal Signal Lines:
+5 V, TTL-compatible signal levels
Bidirectional data bus

System Software
Utility Program Commands:
Read or modify memory
Read saved state of 13½ CPU registers
Start program execution at given location
Start floppy-disk loader program (see Optional Accessories)

Optional Software:
Binary Arithmetic Subroutine Fixed-Point Package
Paper tape (CDP18S826V1)
Cassette (CDP18S826V2)
Binary Arithmetic Subroutine Floating-Point Package
Paper tape (CDP18S827V1)
Cassette (CDP18S827V2)

System Software
Resident Editor Commands:

Move pointer	Save
Delete	Search & Substitute
Append	Type
Insert	Output
Find	

Resident Assembler Operation:
Multipass Output
Output to paper tape or cassette

Resident Editor and Assembler Media:
Paper tape - supplied
Magnetic-tape cassette - supplied

CDP18S012
COSMAC Microtutor II

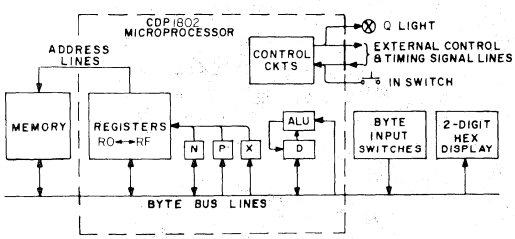
The COSMAC Microtutor II CDP18S012 is a complete basic microcomputer system intended for engineers, students, or hobbyists who wish to understand and use microprocessors. Preassembled and containing its own regulated power supply, Microtutor II provides quick and easy hands-on microprocessor experience. The 64-page instruction manual accompanying the Microtutor II is written in a light style with the beginner in mind. It provides numerous application examples and stresses that computers can be entertaining. The manual assumes that the user has minimal experience with computer systems. By following the step by step procedures, the user will be entering and operating programs within minutes.

System Features

Microtutor II is designed around the RCA CDP1802 COSMAC CPU, as shown in the block diagram. Inputs are provided via eight binary toggle switches; hexadecimal outputs are displayed on two 7-segment LED (hexadecimal digit) displays along with the Q light output. Additional toggle switches are provided for all the required controls to examine and alter memory locations and to initiate program execution. A memory protect switch is included which inhibits the memory write operation to prevent an improperly running program from writing into itself. Programs are loaded via the on-chip DMA (Direct Memory Access) facility which eliminates the need for a "bootstrap" loading routine. A crystal clock is used for stable timing applications. A regulated power supply is also provided.

Microtutor II is provided with 256 bytes of CMOS RAM mounted on a memory card which attaches to the base through a standard 44-pin connector. An additional prewired socket (E1 in the photograph) and a set of connector holes (E2) are provided through which all the COSMAC Microtutor II signals are available for system expansion. Additional RAM and user I/O interfaces can be connected to this extra socket, and an operating system described in the manual can be loaded into the additional RAM to provide a utility memory. The operating system greatly expands the Microtutor II capability, and the memory and I/O extendibility allows the use of Microtutor II in an almost unlimited spectrum of experimental applications.

With the detailed documentation and its ease of operation, Microtutor II is a very desirable introduction to microcomputers for everyone.



Microtutor II block diagram

Specifications

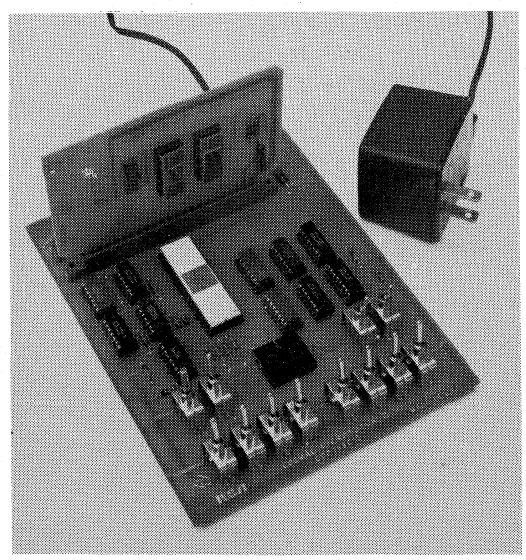
Dimensions: Length 7 inches (179 mm),
Width 5½ inches (141 mm),
Height 3½ inches (90 mm)
Weight: 1 lb. 2 oz., approx.
Power Requirements: 115 V ac, 50/60 Hz
Power Available: 5 V dc at 350 mA (regulated)
Inputs: 8 binary toggle switches in two 4-bit hexadecimal groupings
Outputs: Two 7-segment LED (hexadecimal digit) displays including single-bit Q light
Controls: 4 toggle switches:
RN Run Program
LD Load Memory Enable
MP Memory Protect
IN Input Instruction/Data

Features

256-byte RAM Card
Prewired External Socket and Set of Connector Holes for User Expansion
5-volt Regulated Power Supply
Crystal Oscillator
Debounce Circuitry

Literature

Detailed 64-page **COSMAC Microtutor II Manual** MPM-209



CDP18S020, CDP18S024

COSMAC Evaluation Kit and EK/Assembler-Editor Design Kit

The COSMAC Evaluation Kit CDP18S020 and the COSMAC EK/Assembler-Editor Design Kit CDP18S024 provide a convenient means of learning about the design, hardware interfacing, and programming of microcomputer systems based on the RCA1800-series microprocessor. Each Kit can also serve as the basis for breadboarding and prototyping user-designed microcomputer systems. A feature of the EK/Assembler-Editor Design Kit is a software package containing an assembler and editor program on either magnetic tape (CDP18S024V2) or paper tape (CDP18S024V1), as required by the user, to facilitate the development of assembly language programs. Shipped in kit form, either Kit can be put together in about five hours. All the parts needed are included: IC's, discrete devices, connectors, the PC board, switches, crystal, LED's, and detailed assembly, check-out, trouble-shooting, and operating instructions.

External equipment required to operate the assembled Evaluation Kit includes a 5-V, 600-mA power supply such as the RCA CDP18S023 and either a standard serial ASCII terminal or an RCA Microterminal CDP18S021.

External equipment required to operate the assembled EK/Assembler-Editor Design Kit includes a power supply of +10 and +5 volts and a standard ASCII terminal.

System Functions

The heart of the Evaluation Kit and the EK/Assembler-Editor Design Kit is the CDP1802 8-bit microprocessor. Surrounding the CPU in this all-CMOS system are RAM's, ROM's, and I/O ports. The system contains basic controls, terminal interface (20-mA loop or RS232C), and room for expansion.

As illustrated in the layout diagram, the system can be divided into three functional areas: control and communications, RAM memory, and user I/O.

The **control and communications area** contains the CPU, the utility ROM and RAM, the I/O ports, the control logic and switches, the terminal interface, and the display. The **user I/O** area is available for expansion and customizing the performance of the Kit. A standard 44-pin connector is used for all required system communications and power; a separate connector makes all 40 pins of the CDP1802 available to the user; and a third 44-pin connector is provided for the user I/O area.

In the **control and communications area** two CDP1852D byte I/O ports provide a parallel byte interface to the system, one in and one out. A data byte is strobed into the output port and a service request flag on the CDP1852D is pulsed by an output instruction execution. Data strobed into an input port sets the service request flag and is transferred to the CPU on execution of an input instruction. This service request flag, indicating that data is available, may be strapped to either the interrupt or one of the flag lines in the CPU. These 16 data lines are dedicated to user data. A third CDP1852D is used as the high-order memory address latch to allow addressing a field of 65 kilobytes of memory, if necessary.

The Utility ROM and RAM section consists of a CDPR-512D, which is a CDP1832D 512-byte ROM preprogrammed with a Utility Program UT4, and a CDP1824D 32 x 8 RAM used as a dedicated stack. In this board area a pre-wired socket is available for a CDP1831 512 x 8 ROM which can be used for custom mask pattern verification.

Also in the control and communications area is a row of 29 LED's used to indicate the status of the 16 memory address lines, the 8-bit data bus, the state codes, the control lines, and the Q flip-flop. When used with the single-step control, the LED's provide an important diagnostic and debugging capability.

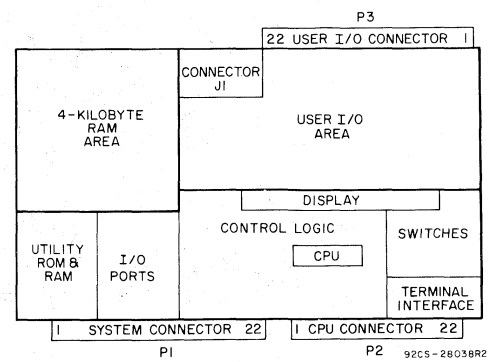
The **RAM memory area** has a total on-board capacity of 4 kilobytes. RAM memory included with the Evaluation Kit CDP18S020 is 256 x 8 configured from two 256 x 4 CDP1822D static CMOS RAM's. There are pre-wired locations on the board for 30 additional CDP1822D's. RAM memory included with the EK/Assembler-Editor Design Kit CDP18S024 is 32 CDP1822D (256 x 4) static CMOS RAM's filling the entire on-board 4-kilobyte capacity.

The **user I/O area** is a 7" x 4" section of the board reserved for user-designed circuits. The area is prebussed and drilled for 14-, 16-, 28- and 40-pin dual-in-line integrated circuits and other components. Because it is isolated from the main portion of the board, this section is suitable for PROM's, user interface circuits, additional byte I/O ports, memory expansion, displays, and the like. The 44-pin connector adjacent to this section is provided for convenient access.

System Software and Firmware

The **Resident System Utility** program UT4 comes with both Kits in the form of a preprogrammed 512 x 8 ROM (CDPR512D). This utility program allows the user to inspect and modify memory and start program execution at any location. When it is started, the utility program stores 13½ of the CPU's registers in its dedicated RAM from which they can subsequently be printed out for debugging purposes. Additional debugging capability is provided by a single-step mode and LED display showing current memory address and data bus status.

The utility program also provides the capability for program load, memory dump, and terminal interfacing for



Layout of Evaluation Kit CDP18S020 and EK/Assembler-Editor Design Kit CDP18S024 from the component side.

CDP18S020, CDP18S024

serial ASCII data terminals. It automatically adjusts to baud rates of 110 and 300 and operates in the full duplex mode. The utility program makes use of the CDP1824D 32 x 8 RAM as a dedicated 32-byte deep stack for register-save functions.

A complete source listing of the resident utility program UT4 is provided and its read and type routines are user-accessible.

The **Resident Editor** program supplied with the EK/Assembler-Editor Design Kit CDP18S024 permits standard text editing such as adding or deleting characters, word, or lines. It uses an implicit pointer to identify the area of text being operated on. The programmer controls the position of the pointer and the operations to be performed relative to its location. Keyboard or magnetic or paper tapes are acceptable inputs, and outputs of magnetic or paper tape are obtained.

The **Resident Assembler** program supplied with the EK/Assembler-Editor Design Kit CDP18S024 converts instruction mnemonics into machine code. The assembly process consists of two or three passes of source statements through the assembler. The first pass constructs the symbol table in RAM, prints it on the terminal, and flags syntactic errors. The second pass generates the appropriate COSMAC hexadecimal code and outputs a complete assembly listing showing each source line and the associated COSMAC machine code. Error messages are also generated as the assembler finds coding mistakes. Once the program is assembled, it may be loaded into the Design Kit via the UT4 program.

The 4-kilobyte RAM supplied with the CDP18S024 is sufficient to hold the resident editor program and provide a working buffer of about 1 kilobyte or the assembler with storage for about 100 labels. There is no limit to the number of lines that can be assembled or edited.

Two versions of the COSMAC EK/Assembler-Editor Design Kit are available. They differ only in the media on which the assembler and editor are provided. The CDP18S024V1 supplies the software on paper tape suitable for use on a Model 33 Teletype• terminal operating at 10 characters per second. The CDP18S024V2 supplies the software on magnetic tape for use on a TI Silent 700* terminal operating at 30 characters per second. When a teletypewriter is used with the CDP18S024V1, a reader-control relay must be installed. When a TI Silent 700 terminal is used with the CDP18S024V2, it must be equipped with dual tape drives, remote (**not** automatic) device control, and must not be equipped with automatic search control.

System Operation

The system is operated by four control switches: RESET, RUN U, RUN P, and CONT/STEP.

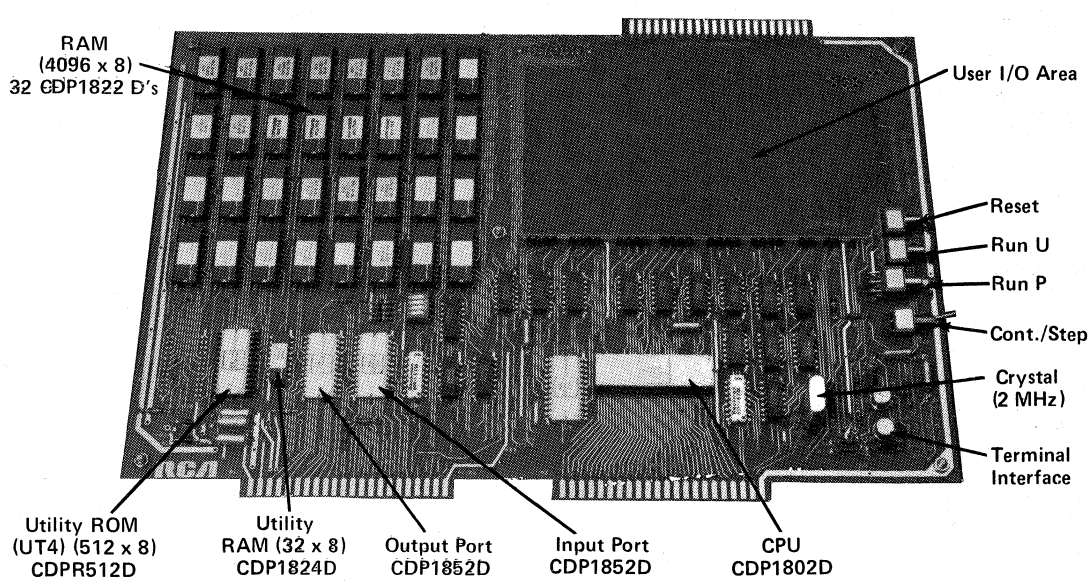
RESET initializes the CPU and other board logic to be ready for any of a series of commands. RUN U transfers control of the system to the resident utility program. The registers may then be examined or the editor, assembler, or user-written programs may then be loaded. RUN P starts execution of the user-supplied programs at address 0000 or restarts the editor or assembler.

The CONT/STEP toggle switch determines the operating mode. In the CONTINUOUS mode the CPU runs normally. In the SINGLE-STEP mode, one machine cycle of a program is executed every time the RUN P or RUN U control is pressed.

Features

- Elementary debugging functions are available combining the single-step feature, the display LED's, and the CPU signals available on a separate connector.
- Advanced debugging capability is available through the use of the optional Micromonitor CDP18S030.

• Registered trademark, Teletype Corporation
* Registered trademark, Texas Instruments Corporation



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Photograph of assembled PC board for the EK/Assembler-Editor Design Kit CDP18S024 with major components and areas called out.

- A write-protection system.
- Industry-standard UV-erasable PROM's can be accommodated in either the UT4 ROM socket or in the user I/O area.
- With its flexibility, either Kit lends itself to frequent use and experimentation. To provide the user with additional information on the COSMAC Microprocessor and Kit applications, a request form for a COSMAC update service is included with the Kit.

Options

The **COSMAC Micromonitor** CDP18S030 is a self-contained, powerful debugging tool for use with any CDP-1802 microprocessor system. It permits debugging of both hardware and software in real time. The Micromonitor includes a built-in keyboard and display, status indicator lights, and software debugging routines. Its primary use is for prototype-system software and hardware debugging. However, because of its easy portability, it is also useful as a field service tool. In addition, it can be used as a versatile production tester. (Product Description: PD18; Manual: MPM-218)

The **COSMAC Microterminal** CDP18S021 is a small hand-held terminal available to run the Evaluation Kit and the EK/Assembler-Editor Design Kit. It comes as a fully assembled unit capable of controlling the system and loading the RAM. It is, however, not designed to operate with the assembler or editor programs. The area on the Kit labeled "J1 connector" is pre-wired for the Microterminal. Its installation, therefore, is very simple. (Product Description: PD12; Manual: MPM-212)

The power supply CDP18S023 is also available for use with the Evaluation Kit. Rated to supply 600 mA at 5 V ± 5%, it will power an Evaluation Kit with 4 kilobytes of RAM plus the Microterminal. Input requirements are 110 V at 50/60 Hz. It can also be used as the +5-V supply for the EK/Assembler-Editor Design Kit.

Literature

Supplied with each Kit is a loose-leaf Manual giving detailed information on assembly, operation, troubleshooting of hardware, checkout of software, and the use of the Assembler-Editor program. This Manual, titled **Instruction Manual for the RCA COSMAC Evaluation Kit CDP18S020 and EK/Assembler-Editor Design Kit CDP-18S024**, is in loose-leaf form to facilitate the addition of updated material. The Manual is also available separately in bound form under the designation MPM-224.

Specifications

(For both Kits CDP18S020 and CDP18S024V1 or V2, except where indicated)

Microprocessor: CDP1802D CMOS 8-bit CPU
RAM: CDP18S020 - 256 words by 8 bits (2 CDP1822D's)
CDP18S024V1 - 4096 words by 8 bits (32 CDP1822D's)
CDP18S024V2 - 4096 words by 8 bits (32 CDP1822D's)
Resident Firmware: Utility Program UT4.
ROM CDPR512D (Preprogrammed CDP1832)
RAM CDP1824D (32 by 8)
Resident Software: Assembler and Editor Programs -
CDP18S024V1 and CDP18S024V2 only
CDP18S920V1 - paper tape (CDP18S024V1)
CDP18S920V2 - magnetic tape (CDP18S024V2)
I/O: Direct terminal interface (20 mA or RS232C serial ASCII)
2 byte I/O ports (2 CDP1852D's)
1 address latch (1 CDP1852D)
All CPU signals accessible
Separate user I/O area and connector
LED display
Connections: 3 standard 44-pin connectors: System, CPU, User I/O plus Microterminal connector location
Controls: RESET: initializes CPU and control logic
RUN U: starts resident utility program UT4
RUN P: starts user program (from memory location 0000)
restarts editor or assembler
CONT/STEP: selects continuous or single-step operating mode
Power Required: CDP18S020 - 5 V dc at 500 mA total; or, 10 V dc at 200 mA plus 5 V at 400 mA for LED's
CDP18S024 - 10 V dc at 200 mA plus 5 V at 400 mA for LED's
Dimensions: PC Board: 14" x 10"
User I/O Area: 7" x 4"
Parts List: 1 CDP1802D
2 CDP1822D (CDP18S020) 32 CDP1822D (CDP18S-024V1 or V2)
1 CDP1824D
1 CDPR512D
3 CDP1852D
29 LED's
1 2.0-MHz Crystal
4 DIP Sockets (CDP18S020) 34 DIP Sockets (CDP18S-024V1 or V2)
1 Edge Connector
1 PC Board
– Discretes, Resistors, Capacitors, Support IC's, Switches, Hardware
1 **Instruction Manual for the RCA COSMAC Evaluation Kit CDP18S020 and EK/Assembler-Editor Design Kit CDP18S024**
1 **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201
1 CDP18S920V1 - paper tape (CDP18S024V1) or
1 CDP18S920V2 - magnetic tape (CDP18S024V2)

CDP18S021

COSMAC Microterminal

The COSMAC Microterminal CDP18S021 is a fully assembled, compact, hand-held terminal designed for interfacing with CDP1802-based microcomputer systems. Combined with its Utility program (UT5) supplied as firmware, the Microterminal:

- Is specifically suited for use with the COSMAC Evaluation Kit or comparable user-designed systems.
- Can be easily used in portable or battery-operated applications.
- Performs standard control, communications, and debug functions.
- Is a low-cost, convenient non-hard-copy alternative to more expensive conventional terminals.

Data and memory addresses as well as the control functions are entered through the keyboard; both the address and data are displayed.

The COSMAC Microterminal directly interfaces with the Evaluation Kit (CDP18S020) without the need for any additional hardware or software. The combination of the two provides a low-cost microcomputer development system.

Functions

The many functions performed by the Microterminal are regulated principally by its keyboard. Control signals include:

Key	Function	Description
R	Reset	Initializes and resets the microprocessor system.
RU	Run Utility	Starts execution of the Utility Program UT5.
RP	Run Program	Starts program execution at memory location 0000.
SP	Start Program	Starts program execution at the address shown on display.
INC	Increment	Writes data into memory and increments the memory address.
CA	Clear Address	Clears memory address to 0000.
⟷	Mode Selection	Switches the operating mode to data entry or address entry.
STEP/CONT		Selects either continuous or single-step program execution.

The **keyboard**, used for data and memory address entry, includes all the above control functions (except STEP/CONT) along with 16 standard hexadecimal input keys. Of the total 24 keys, one is not used but can easily be accessed for custom functions.

The **display** is a field of eight 7-segment LED's for full hexadecimal displays. The left four digits normally display the memory address, and the two right-hand digits show the data. The decimal points in the appropriate field are lit to indicate the current addressing mode (data entry or address entry). A 20-wire ribbon cable is supplied for all necessary interfacing signals.

The **Utility program UT5**, supplied as firmware (CDPR-522), is the controller of the Microterminal. It contains a series of useful subroutines linked together to run the system to do custom functions as organized by the programmer.

UT5 routines include:

- Display formatting and control.
- Keyboard scan, debounce, and decode.
- CPU register initialization for the CDP1802 call-and-return subroutine linkage.
- Independent control of all eight display digits and decimal points.
- Readout control of CPU registers R1 through RF.
- Consecutive readout of memory locations at 1-Hz rate.
- Display of registers RA and RB in a user's program.
- Read and modify RAM.

Operation

Operation of the Microterminal is both basic and straightforward. Following are three examples of basic programming and execution routines that can be done with the Microterminal and a COSMAC Evaluation Kit or similar user-built system.

1. **Display the contents of memory location 801F**. Memory addresses are entered highest-to-lowest order of significance and are shifted through the display right to left.

Enter	Press	Display	Comments
–	R		Reset the system.
–	RU	0.0.0.0. X X *	Run the Utility Program. The Microterminal is in the address entry mode.
8	–	0.0.0.8. X X	Enter address location "801F" to read and display the contents (in this example, 32).
0	–	0.0.8.0. X X	
1	–	0.8.0.1. X X	
F	–	8.0.1.F. 3 2	

*X indicates a don't care or intermediate output.

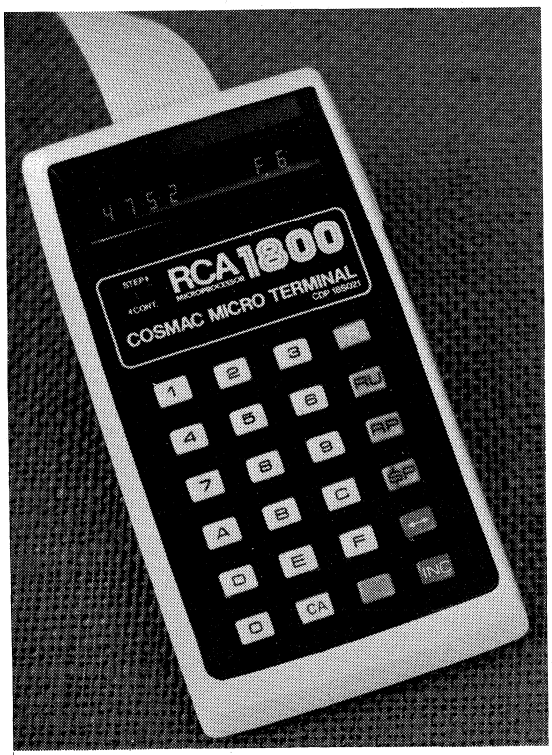
2. **Insert program commands FF, 03, B4 starting at memory location 0041**. Go to the desired starting address, switch to the data entry mode, and enter the program information for this operation.

Enter	Press	Display	Comments
–	CA	0.0.0.0. X X	Clear address to 0000.
4	–	0.0.0.4. X X	Enter address 0041.
1	–	0.0.4.1. X X	
–	↔	0 0 4 1 X.X.	Switch to data entry mode.
F	–	0 0 4 1 X.F.	Enter program information; e.g., FF.
F	–	0 0 4 1 F.F.	
–	INC	0 0 4 2 X.X.	Write "FF" to location 0041 and advance to next memory location.
0	–	0 0 4 2 X.0.	Enter data.
3	–	0 0 4 2 0.3.	
–	INC	0 0 4 3 X.X.	Write and advance.
B	–	0 0 4 3 X.B.	Enter data.
4	–	0 0 4 3 B.4.	
–	INC	0 0 4 4 X.X.	Write and advance.

3. **Start program execution at memory location 0005.** Simply enter the starting address and issue the start program execution command.

Enter	Press	Display	Comments
–	CA	0 0 0 0 X.X.	Clear address.
–	↔	0.0.0.0. X X	Switch to address entry mode.
5	–	0.0.0.5. X X	Enter address 0005.
–	$P		Blank display.

During user-program execution the display is blanked unless the program calls the Microterminal as an output. The control subroutine for this operation is part of UT5.



To examine operation of the Microterminal as a program analyzer or debugger, which utilizes routines in UT5, consider this example:

4. **Examine the contents of the 16x16 register matrix of the CDP1802 microprocessor after execution of the instruction at memory location 0020.** By breaking into the program at location 0021 (after execution of the instruction at 0020), successive Run Utility commands will display the registers' contents on the memory address display LED's of the COSMAC Evaluation Kit.

Enter	Press	Display	Comments
	R		Reset.
	RU	0.0.0.0. X X	Run utility.
2		0.0.0.2. X X	Enter address 0021.
1		0.0.2.1. X X	
	↔	0 0 2 1 X.X.	Switch to data entry mode.
0		0 0 2 1 X.0.	Enter data "00".
0		0 0 2 1 0.0.	
	INC	0 0 2 2 X.X.	Write and advance. (The "00" op code is an idle instruction. It freezes CPU operation at its execution until signalled to continue. Thus, program execution will break at location 0021 as desired.)
	RP		Start program execution at 0000. Program will stop execution at location 0021, containing the "00" op code.
	R		Reset. Switch to the STEP mode (STEP/CONT switch).
	RU		Initialization cycle.
	RU		Execute first 3 instructions of UT5. (In the STEP mode, RU permits execution of one instruction.
	RU		
	RU		
	RU		Fourth instruction will display R2 on memory address LED's on Evaluation Kit.
	RU		Display R3.
	RU		
	·		·
	·		·
	·		·
	·		·
	·		·
	·		·
–	RU	–	Display RF.
–	RU	–	Display R1.
–	RU	–	

In addition, the operator can control and use the Microterminal as an output display by use of the subroutines provided. A complete listing of the UT5 program and further applications information are included in the **Instruction Manual for RCA COSMAC Microterminal CDP18S021**, the MPM-212.

CDP18S021

Features

- Lightweight, compact, portable terminal; requires less than 375 mA at 5 V.
- User can exercise program debug functions through the versatile single-step mode.
- Programming, memory and register inspection, and control of the COSMAC Evaluation Kit and user programs.
- Provides a low-cost, programmable display unit for prototyping or end use.
- User-accessible subroutines in UT5 offer system- and program-simplifying capabilities.
- Performs memory scan by sequentially displaying memory contents automatically.

Options

The COSMAC Microterminal CDP18S021 can interface with many user-designed COSMAC-based systems. It is especially well suited for use with the COSMAC Evaluation Kit, a complete evaluation and prototyping system using the CDP1802D. Product Description PD3 provides an in-depth description of the Evaluation Kit (Part number: CDP18S020; manual: MPM-203A).

The Microsupply, capable of powering the Evaluation Kit with 4 kilobytes of CDP1822S RAM and the Microterminal, is also available. The unit plugs into any standard 110-volt 50/60 Hz outlet and is rated to supply 600 milliamperes at 5 volts dc ± 5% (Part number: CDP18S023).

UT5, the Utility ROM, is available for purchase separately for custom-designed systems (Part number: CDPR522).

Specifications

Terminal

Dimensions: 5.5" x 3.0" x 0.7"
Weight: 5 ounces (approximately)
Power Requirements:
V_{LED} = 250 mA (max.) @ 5 V, and
V_{CC} = 110 mA @ 5 V
5 V ≤ V_{CC} ≤ 12 V
Terminal Interface:
V_{SS} to V_{CC} at CMOS logic levels.
(V_{CC}, V_{LED}, and V_{SS} are all available from the COSMAC Evaluation Kit.)
Display (Outputs):
Eight 1/4" x 1/16" 7-segment LED's.
Keyboard (Inputs):
Twenty-four keys; 23 specific functions, 1 unused key; plus STEP/CONT switch.
Interfacing:
20-wire ribbon cable (15"), with connector; mating connector for COSMAC Evaluation Kit.

Utility ROM UT5

Mask-programmed CDP1832D ROM, part number CDPR522.
Replaces UT4 ROM (location U2) when the Microterminal is used with the COSMAC Evaluation Kit.

Literature

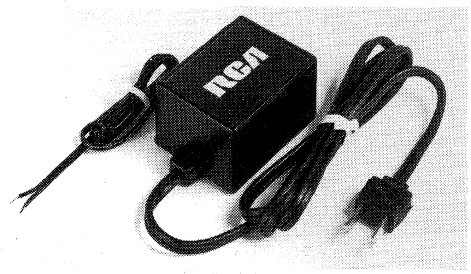
Operation, installation, and applications data are in the **Instruction Manual for RCA COSMAC Microterminal CDP18S021**, the MPM-212, which is included with the unit.

COSMAC Power Converter

CDP18S023
CDP18S023V1

The COSMAC Power Converters CDP18S023 and CDP18S023V3 are lightweight, inexpensive, convenient power supplies especially suitable for use with RCA COSMAC Microboard System modules or with the COSMAC Evaluation Kits CDP18S020 and CDP18S024. The CDP18S023 is supplied with the COSMAC Evaluation System CDP18S025. The CDP18S023 plugs into any standard 110-volt 50/60-Hz wall outlet and has a regulated output of +5 volts dc ± 5% at 600 milliamperes. Its over-all dimensions are 2.7 x 2.1 x 1.6 inches (69 x 53 x 41 mm); its weight is 12.5 ounces (354 grams).

The CDP18S023V3 operates with input voltages from 210 to 250 volts, 50 Hz, and provides a regulated output of +5 volts dc ± 5% at 600 milliamperes. It is supplied with a standard European-type two-pin molded plug. The CDP18S023V3 over-all dimensions are 5.12 x 2.5 x 2.0 inches (130 x 63.5 x 50.8 mm); its weight is 17 ounces (482 grams).



CDP18S023

CDP18S023V3

CDP18S025

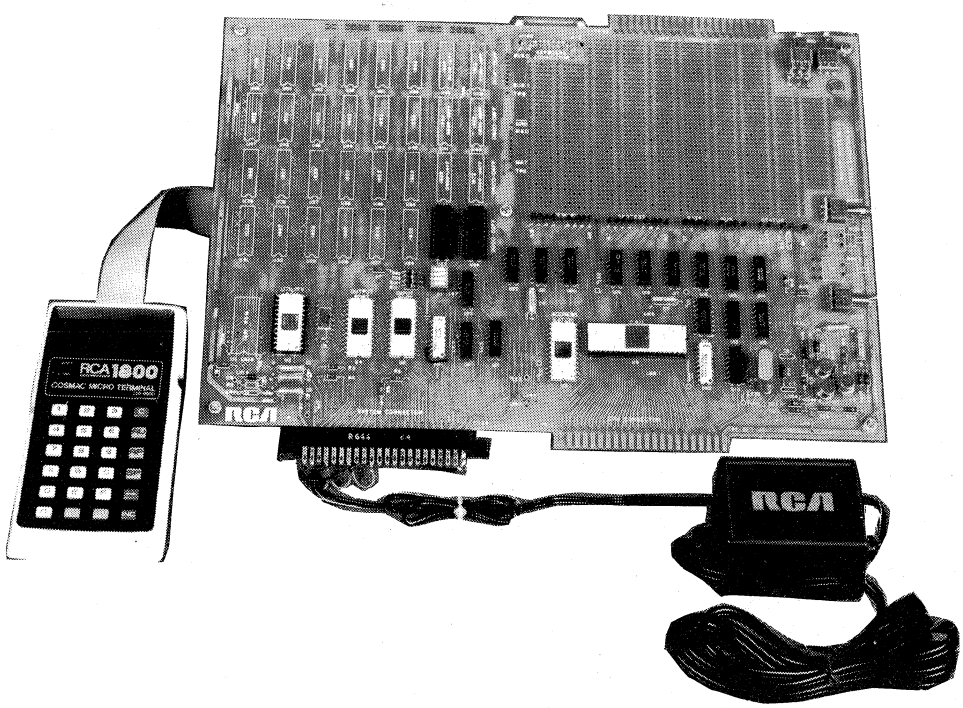
COSMAC Microprocessor Evaluation System

The COSMAC Microprocessor Evaluation System CDP18S025 includes a COSMAC Evaluation Kit, a Microterminal, and a Power Supply. This readily assembled system is a complete starting package for microprocessor evaluation through machine-language programming and prototyping.

For specifications and detailed information on the three components of the Evaluation System, see the data pages for the CDP18S020 Evaluation Kit, CDP18S021, Microterminal, and CDP18S023 Power Converter.

Features

- Low-cost complete prototyping and evaluation system for COSMAC family
- 256 bytes of RAM—expandable to 4 kilobytes
- Utility ROM
- Large board area for user functions
- Single-step capability for program analysis
- Memory Address, Data, State Code, Q-Line, Clear, Wait signals all monitored and displayed on LED's
- Extensive instruction literature
- Microterminal has 8-digit 7-segment LED hexadecimal display
- Microterminal displays memory address and data simultaneously
- Display usable as output under user-software control
- Low power CMOS components



CDP18S030

COSMAC Micromonitor

The COSMAC Micromonitor CDP18S030 is a self-contained, powerful debugging tool for use with any CDP1802 microprocessor system. It permits in-circuit debugging in real time of both hardware and software. The Micromonitor includes a built-in keyboard and display, status indicator lights, and software debugging routines. Its primary use is for prototype-system software and hardware debugging. However, because of its easy portability, it is also useful as a field service tool. In addition, it can be used as a versatile production tester.

By means of a single cable connection, the Micromonitor, as shown in the cover photograph, can be interposed between the CPU of a system under test and all the interfaces of the CPU, giving the user control of both hardware interfaces and program execution. The Micromonitor is controlled by its own internal microprocessor, but uses the microprocessor, power supply, clock, memory, etc. of the system under test to run a user program. In this way, the Micromonitor does not "emulate" the system but provides a reliable measure of true system performance.

The Micromonitor can be operated either from its own keyboard or from an external terminal if a hard copy record is desired. Remote operation from a floppy disk file of commands is also possible when the Micromonitor is used with the COSMAC Development System II (CDP18S005) equipped with Floppy Disk System (CDP18S805) and Micromonitor Operating System-MOPS (CDP18S831). With MOPS, the debugging techniques available to the user can extend to hands-off system testing with commands coming from disk files.

System Features

The Micromonitor provides an extensive set of debugging capabilities. Its 43 commands permit the user to examine or modify memory and all CPU registers and flags. The Micromonitor also provides read/write capability to any I/O device and can generate signals to all CPU control, request, and flag inputs and can either inhibit or allow system-generated requests to the DMA and Interrupt lines.

Break conditions can be programmed for all of the following: external flag lines, auxiliary break input, idle, interrupt response, or memory read/write. When a break occurs, the values of D,X,P, and R(P) are recorded, providing a trace function. A log of these values at the last 16 breaks is available to the user.

Three modes for running programs are available. One mode provides for real-time running, starting at a specified address or continuing from a break. The number of break conditions to be encountered before the Micromonitor takes control can be specified in this mode. Another mode provides for single or a specified number of instruction cycles. Data is logged after each instruction cycle in this mode. The third mode provides for a single or a specified number of machine cycles to be executed.

Applications

Prototype Debugging

The Micromonitor can be used with any CDP1802-based user prototype system, as shown in Fig. 1. It provides a powerful tool for both hardware and software debugging of the prototype system. The terminal, if used, can be shared between the Micromonitor and the prototype system without moving cables.

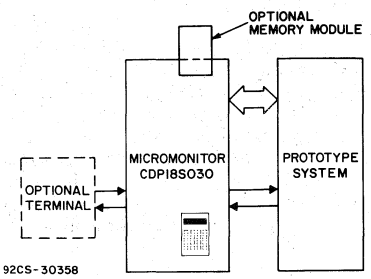


Fig. 1 — Use of Micromonitor as a prototype system debugging tool.

A user-designed memory module or the optional 4-kilobyte RAM module (CDP18S205V1) may be used in the external memory socket to serve as prototype memory prior to prototype memory construction or commitment of code to ROM.

The Micromonitor can also be used with the COSMAC Development System II, as shown in Fig. 2, to form a powerful hardware and software development system. The CDS II has resident editor and assembler capability for rapid program development and spare slots for the addition of user-designed hardware. By controlling the CPU of the CDS II with the Micromonitor, user programs and hardware can be most effectively debugged. The data terminal can be shared between the Micromonitor and CDS without moving the cables.

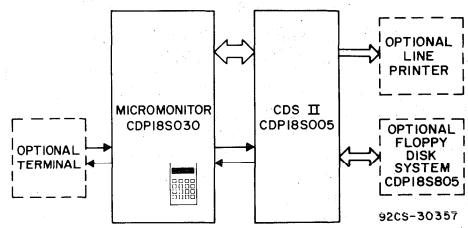


Fig. 2 – Use of Micromonitor as a prototype hardware and software debugging tool with COSMAC Developmental System II CDP18S005.

CDP18S030

Programmable Automated Testing

An optional configureation, shown in Fig. 3, permits the Micromonitor to be operated by a CDS II (CDP18S005) equipped with Floppy Disk System (CDP18S805) and Micromonitor Operating System (CDP18S831). The Micromonitor Operating System (MOPS) includes a UART module, an interface cable, and a Micromonitor Operating System diskette. With this system, lists of Micromonitor commands can be stored on a disk file and later be sent automatically to the Micromonitor. System responses can be directed to a user terminal, a floppy disk file, or both. Disk files can subsequently be sent to a line printer for high-speed printout or to a user terminal.

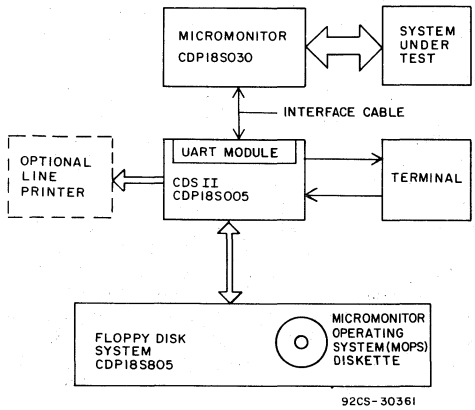


Fig. 3 – Use of Micromonitor as a programmable production or breadboard tester utilizing the Micromonitor Operating System (MOPS) CDP18S831.

Another technique for testing involves the installation of either a user-designed ROM/EROM module or the optional 4-kilobyte RAM module (CDP18S205V1) in the external memory socket of the Micromonitor. The RAM can be loaded via the Micromonitor. The CPU of the system under test can then execute its own test program.

A paper tape or cassette containing test commands can be used as shown in Fig. 4 for a production or breadboard tester provided spaces are left on the tape for responses to the terminal.

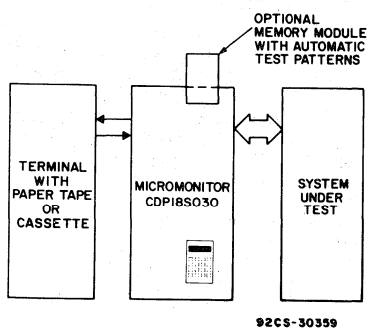


Fig. 4 – Use of Micromonitor as a programmable production or breadboard tester utilizing a data terminal equipped with paper tape or cassette.

Field Service

The Micromonitor is designed to be an effective field-service tool, as shown in Fig. 5. In its own carrying case, it weighs only 16 pounds and has a built-in tracking power supply. The complete debugging capability of the Micromonitor can be operated from its own built-in keyboard and displays. No additional components are required for its operation. In addition to manual operations, preprogrammed ROM-based test patterns can be exercised through an external memory socket on the Micromonitor.

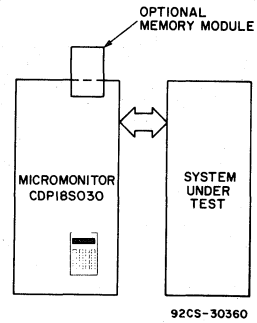


Fig. 5 – Use of Micromonitor as a field service tool.

Micromonitor Features

- Extensive set of debugging facilities.
- Operable from built-in keyboard and display, from external terminal, or from remote file.
- Useful for debugging prototypes, field servicing, or automated production or breadboard testing.
- Capable of bidirectional disk-to-system transfers of commands and data when operated with COSMAC Development System II, Floppy Disk System, and Micromonitor Operating System (MOPS) CDP18S831.
- Buffered terminal output so that a terminal can be shared between the Micromonitor and the system under test without transferring cables.
- Provision for external memory which can be substituted for the system memory for ROM simulation or system memory checkout.
- All address bits available and any size user-designed ROM or RAM may be added. A 4-kilobyte RAM plug-in module is an available option (CDP18S205V1).
- Tracking power supply automatically adjusts to the tested system's power supply over range of 4 to 11 volts.
- Easy recovery from erroneous number entry in command modes built into the software.
- Continuous display of all CPU control lines.
- Break conditions automatically displayed when Micromonitor takes control.
- Parameter-pass feature permits display of X, R(X), and MR(X) or P, R(P), and MR(P) with only three keystrokes.
- Accommodates terminals having rates of 10, 30, or 120 characters per second and 20-mA or RS232C interfaces.
- Self-test card simulates user system allowing verification of Micromonitor operation.

CDP18S030

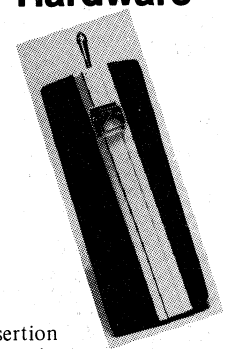
- Fully portable and self contained in attractive carrying case.
- Usable world wide on 110 or 220 volts, 50/60 Hz.

Specifications - User Functions

- Examine or modify memory.
- Examine or modify all CPU internal registers and flags.
- Read or write to I/O devices.
- Generate signals to all external control, request, and flag inputs to CPU.
- Inhibit external request signals.
- Set break conditions on external flags, auxiliary break input, idle, interrupt response or specified memory read/write, or both.
- Data log of D, X, P, and R(P) made on each break or single instruction cycle with sixteen previous states held.
- Three run modes:
  - real time with multiple pass of break conditions
  - single/multiple instructions
  - single/multiple machine cycles

  All modes may run from specified address or present state.

Specifications - Hardware



Dimensions:

Length: 18½ inches
Width: 14½ inches
Height: 6 inches

Weight: 16 lbs. approx.

Controls:

Crystal In/Out
Reset
Power On/Off

Connectors:

CPU socket; 40 pin, zero insertion
Cable socket; 40 pin, zero insertion
Crystal socket; 14 pin, zero insertion
External memory connector; 44-pin edge connector; 0.156 inch pin spacing
Terminal input; 25-pin female Cinch connector
Terminal output; 25-pin male Cinch connector
External break input jack–dual banana
Memory disable output jack–dual banana

Keyboard:

28 keys in 7x4 keyboard matrix; includes hex digit keys, function keys, and a shift key
Tactile response

Display:

8-digit, 7-segment hexadecimal LED
Decimal points lighted as cursor
14 status indicator LED's:
IDLE, MONITOR IN CONTROL, SC1, SC0, WAIT, CLEAR, Q, INTERRUPT, DMAIN, DMAOUT, EF1, EF2, EF3, and EF4

Power Requirements:

110/220 V ac, 50/60 Hz

Power Supply:

Micromonitor logic power supply tracks system under test from 4 to 11 volts. Presents input resistance of 9800 ohms to ground to user power supply.

Can supply up to 400 mA to external memory connector socket.

Operating Temperature Range: 0 to 43°C

Cabling Supplied: AC power cord–8 feet

System Cable:

40 wire, 3 feet long, terminated both ends in 40-pin Textool male connector
40 wire, 1 foot long, terminated both ends in 40-pin Textool male connector

Terminal Interface:

20 mA or RS232C (EIA)
110, 300, or 1200 baud

System Clock:

Uses clock from system under test to run user program
Internal clock: 2.112 MHz, crystal controlled

Self-test Card:

Plug-in card for checking Micromonitor operation.

Available Options

4-kilobyte RAM module CDP18S205V1.

Micromonitor Operating System (MOPS) CDP18S831 including UART module, interface card, and system diskette.

Literature

Operation, installation, and application information is provided in the Instruction Manual for the RCA COSMAC Micromonitor CDP18S030, MPM-218.

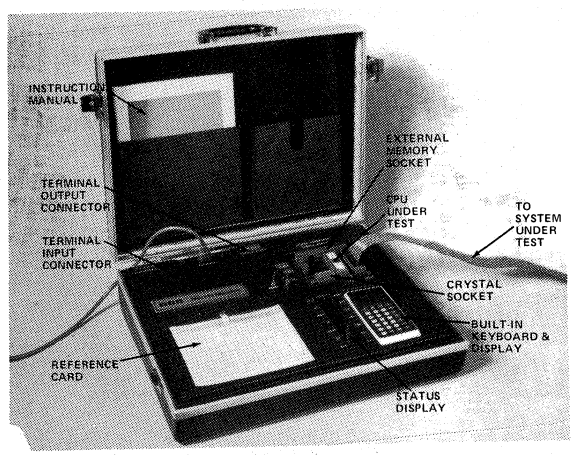


Fig. 6 – RCA COSMAC Micromonitor CDP18S030.

CDP18S205V1

RCA COSMAC 4-Kilobyte RAM Module

Advance Data

The RCA COSMAC 4-Kilobyte RAM Module CDP18S205V1 is a static read-write memory module having thirty-two 256 x 4 CMOS CDP1822 RAM's, two CDP1856 4-bit bus buffer/separators, and two CDP1853 N-bit 1-of-8 decoders. All inputs and outputs are buffered to minimize signal loading. The CDP18S205V1 is designed for use in the RCA COSMAC Micromonitor CDP18S030 or other applications in which a low-power static CMOS memory module having a wide supply-voltage range could be used advantageously.

Features

- Low-power static CMOS
- Operable from 4.0 to 10.5-volt single supply
- Small size—(4.5 x 7.5 inches)
- Compatible with COSMAC Development Systems
- High noise immunity
- Flexible address assignment
- Fully buffered
- Operating Temperature Range—0 to 43 °C

Specifications

Memory Capacity
4096 bytes (32 CMOS static RAM's 256 x 4)

Memory Addressing
Occupies any contiguous 4-kilobyte block within the available address space. Block address selected externally.

Operating Temperature Range
0 °C to 43 °C

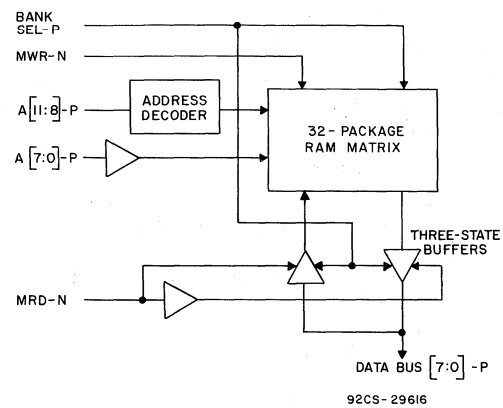
Dimensions
4.5 x 7.5 inches (114.3 x 190.5 mm)
Board pitch of 0.5 inch (12.7 mm) minimum.

Power Requirements
+4.0 to 10.5 volts; 10 milliamperes typical operating.

Connector
System interface: Edge fingers, 44 pins on 0.156-inch centers.

Pin List, Bus Interface Signals

Table I provides a list of the pins and the signals for the 44-pin system interface connector of the CDP18S205V1 4-Kilobyte RAM.



Block diagram of RCA COSMAC 4-Kilobyte RAM Module CDP18S205V1.

Table I—Pin Terminals and Signals for RCA COSMAC 4-Kilobyte RAM CDP18S205V1 (Connector P1)

Pin	Signal	Pin	Signal
A	—	1	—
B	—	2	—
C	DB0-P	3	—
D	DB1-P	4	—
E	DB2-P	5	MRD-N
F	DB3-P	6	—
H	DB4-P	7	A11-P
J	DB5-P	8	A10-P
K	DB6-P	9	A9-P
L	DB7-P	10	A8-P
M	A0-P	11	—
N	A1-P	12	—
P	A2-P	13	—
R	A3-P	14	—
S	A4-P	15	—
T	A5-P	16	—
U	A6-P	17	—
V	A7-P	18	—
W	MWR-N	19	—
X	BANK SEL-P	20	—
Y	+5 V	21	+5 V
Z	GND	22	GND

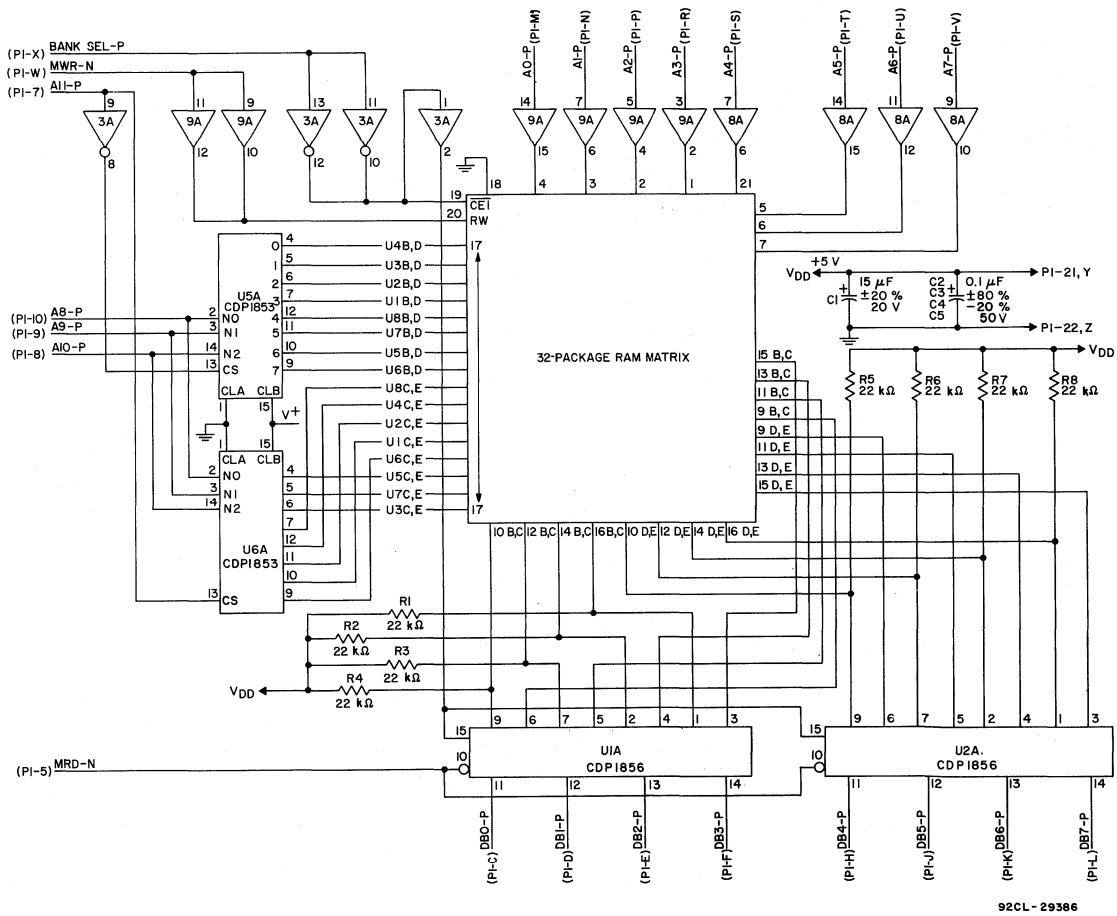
Installation in the COSMAC Micromonitor CDP18S030

The RCA COSMAC 4-Kilobyte RAM CDP18S205V1 may be installed in the Micromonitor CP18S030 to provide 4 kilobytes of additional RAM to the system under

test. After the power to the system under test is turned off, the CDP18S205V1 is installed in the external memory interface connector P1 of the Micromonitor. For additional information on the use of external memory with the Micromonitor, refer to the **Instruction Manual for the RCA COSMAC Micromonitor CDP18S030**, MPM-218.

Installation in COSMAC Development Systems CDP18S005 or CDP18S007

The RCA COSMAC 4-Kilobyte RAM CDP18S205V1 maybe installed in the COSMAC Development Systems CDP18S005 or CDP18S007 in any unused memory slot 1 through 9. A Bank Select Signal (BANK SEL-P) from the Address Latch and Bank Select Module CDP18S206 in Slot must be wired to Pin X of the slot holding the installed module. Consult the **Operator Manual for the RCA COSMAC Development System II CDP18S005**, MPM-216 or the **Hardware Reference Manual for the RCA COSMAC Development System (CDS III) CDP18S007**, MPM-233 to determine which 4-kilobyte banks are open in the system being used.



4-kilobyte RAM module CDP18S205V1 logic and circuit diagram.

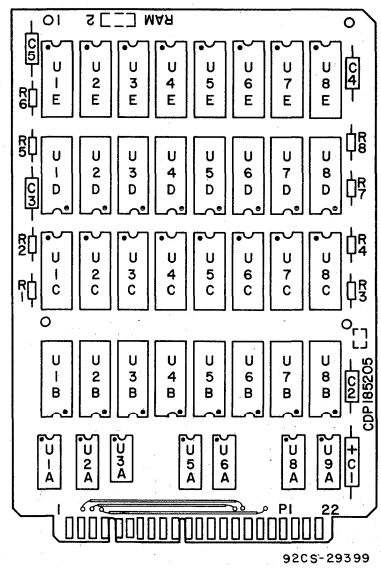
CDP18S205V1

Application Considerations

The CDP18S205V1 4-kilobyte RAM decodes twelve address lines (A0-A11) for the on-board address range. In any CDP1802-based system, it is necessary to latch four of the high-order address bits (A11, A10, A9, A8) to make up this complement. Without further decoding and with Pin X tied high, the 4-kilobyte RAM will be located from 0000_{16} to $3FFF_{16}$ and will "wrap" every four-kilobyte address. To locate the CDP18S205V1 4-kilobyte RAM precisely in the 65-kilobyte address range, it is necessary to latch and decode the highest four address bits and to apply the decoded signal to Pin X of the CDP18S205V1. A high ($+V_{DD}$) on Pin X enables the module; a low (V_{SS}) signal disables it.

Parts List for CDP18S205V1

C1 = 15 µF, ±20%, 20 volts
C2,C3,C4,C5 = 0.1 µF, +80%, −20%, 50 volts
R1 through R8 = 22 kilohms, ±5%, ¼ watt
U1A,U2A = CDP1856D
U1B through U8B
U1C through U8C
U1D through U8D
U1E through U8E
} = CDP1822
U3A = CD4069BE
U5A, U6A = CDP1853D
U8A, U9A = CD4050BE



4-kilobyte RAM module CDP18S205V1 layout diagram.

PROM Programmer for Use with COSMAC Development System II

CDP18S480
CDP18S480V1
CDP18S480V2

The PROM Programmer CDP18S480 is a hardware and software package designed to work with the COSMAC Development System II (CDP18S005) for programming industry-standard PROM's. The package includes a plug-in module for the CDS II and software containing a versatile operating program. The system will program Intel 2704, 2708, 2716, 2758, or any other equivalent PROM's. A further feature is that it facilitates the rapid programming of many PROM's from the same source. In addition, it can read but not program Intel 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's.

Three versions of the PROM Programmer are available differing only in the software media with which they operate. The disk-based version is designated CDP18S480; the paper-tape version is designated CDP18S480V1; and the magnetic-tape cassette version is designated CDP18S-480V2. Thus, the PROM Programmer will work with any configuration suitable for the CDS II.

Installation

A user-supplied external power supply is required for programming operations. In addition, a –9-volt supply is needed for reading 1702 PROM's. All other voltages needed are supplied from the CDS internal power supplies. Installation of the plug-in module is straightforward in that it only requires three jumpers to be added to the selected I/O slot. It can be plugged into any unused I/O slot in the CDS card nest. When the external power supply (and the –9-volt supply, if required) is connected and the program loaded, operation can begin.

Operation

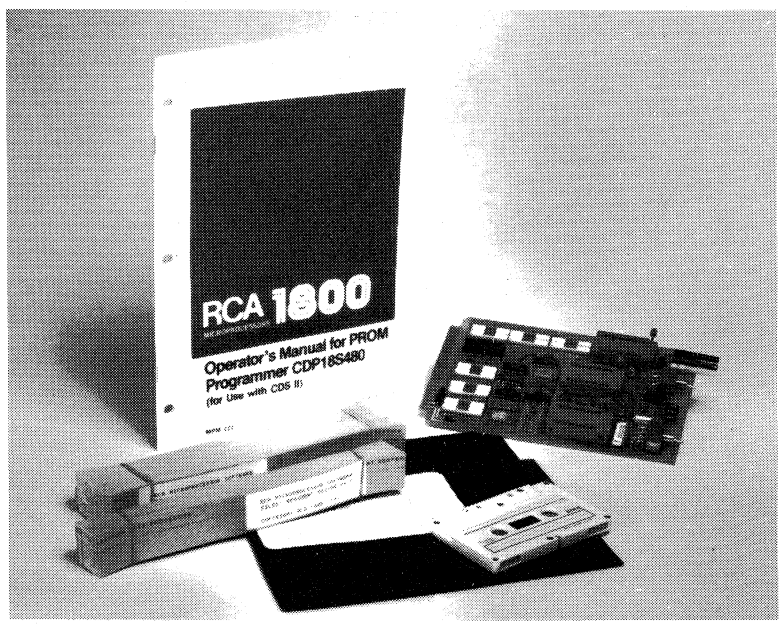
The software provides many types of operation including:

- Programming a PROM from a file or by copying another PROM
- Verifying a PROM against a file or another PROM
- Verifying erasure of a PROM
- Combining two smaller PROM's to program a larger one
- Saving PROM data on a file in reloadable format that can also be used for masked ROM production
- Performing any of the above operations with either positive (non-inverted) or negative (inverted) logic

The program is supplied in both object code and assembly language source. The PROM Programmer module is prewired for I/O Group Select 3 but may be reassigned to a different Group Select by the user.

The program occupies the first two kilobytes of memory in the CDS and uses the second two kilobytes as a buffer area for data. Thus, the program can run in a standard CDS II with the supplied four kilobytes of RAM. Any additional system memory available, however, can be used to advantage because the RAM buffer area for the various operations is user definable.

Installation instructions and details of operation for this system are given in the **Operator's Manual for PROM Programmer CDP18S480 (for Use with CDS II)**, MPM-222.



CDP18S480
Specifications

Basic Operations:

- Program a PROM from a RAM buffer or file; automatically followed by a verification
- Verify a PROM against RAM buffer or file
- Copy a PROM into RAM buffer; automatically followed by a verification
- Fill RAM buffer with all 1's or 0's; used in verifying PROM erasure
- Save RAM buffer onto a file

Operating Temperature Range:

0^{o} to $43^{o}C$

Plug-In Module:

Dimensions: 4.5 inches x 7.5 inches
Three Zero-Insertion-Force PROM Sockets
1 for a 1702
1 for a 2704/2708
1 for a 2716/2758
Plugs into any unused I/O slot
Assigned to Group Select 3

Power Supplies:

External – Programming Power:

+26 volts ± 0.1 volt at 50 mA for 2716/2758
+25 volts ± 0.1 volt at 20 mA for 2704/2708
–9 volts ± 5% at 70 mA for reading 1702 PROM's

From CDS II:

+5 volts at 200 mA
–5 volts at 50 mA
+12 volts at 70 mA

Other Required System Components:

COSMAC Development System II – CDP18S005
Power Supplies: Programming Power; –9 volts (see above)
COSMAC Floppy Disk System II – CDP18S805, or
Data Terminal – as required by CDS II

LED Indications:

Power ON to PROM
External Programming Power ON
Programming ON

Switches:

Power to PROM ON/OFF
Selector Switch

Programming Times:

2704 – 1 minute 25 seconds
2708 – 2 minutes 45 seconds
2716 – 1 minute 45 seconds
2758 – 50 seconds

PROM Programmer Components:

Plug-in Module for use with CDS II (CDP18S402)

Software:

Diskette (CDP18S480)
Paper tape (CDP18S480V1), or
Cassette (CDP18S480V2)

MPM-222 – **Operator's Manual for PROM Programmer CDP18S480 (for Use with CDS II)**

Types of PROM's Handled:

1702	256 word by 8 bit – read only	Intel PROM's or equivalent
2704	512 word by 8 bit	
2708	1024 word by 8 bit	
2758	1024 word by 8 bit	
2716	2048 word by 8 bit – single-voltage only	

CDP18S508

COSMAC UART Interface Module

The UART (Universal Asynchronous Receiver/Transmitter) Module CDP18S508 is a printed-circuit card designed to provide the COSMAC Development System CDS II (CDP18S005) with a serial interface for operating a teletypewriter (TTY), a CRT, or any of various data terminals. The CDP18S508 UART Interface Module also provides a paper-tape control for use with a TTY, and serial interfaces for 20-mA loop and EIA RS232C data terminals. The CMOS UART CDP1854 is used in the Module to provide a byte interface to the system and a serial interface to the terminal. The UART is used in its Mode 1 configuration so that word length, parity, and stop bits are software-programmed. A switch is provided to permit selection of a baud rate of 110, 300, 1200, 4800, 9600, or 19,200 baud.

Installation

The UART Interface Module CDP18S508 may be installed in any I/O slot in the CDS Card Nest. Slot 24 is usually used for disk and 14 for the terminal interface. Locations 14 through 18 and 21 through 24 provide all the signals required by this Module except the I/O address lines. These lines are chosen by the user. The combination of Select and N-Decode lines chosen must be unique so that no combination is used twice in the system. They are connected as follows:

Select – Wire-wrap to pin T the I/O select line chosen from SEL1 through SEL7 (SEL0 is assigned a specific I/O function).

N Decode – Wire-wrap to pins M and N the two decoded N lines chosen from N=1 through N=7. The connection to pin N fixes the N code for data read and write. The connection to pin M determines the N code for setting the control register or for reading the status register.

Paper-Tape Control – Wire-wrap pin W to N=7, if paper-tape control is needed. Location 14 in the CDS is prewired to this signal.

Various links or jumpers may be installed on the printed-circuit card for optional connections to the system. The interrupt signal from the CDP1854 may be jumpered at LK1 to INT on the CDS backplane. The CDP1854 signals DA, THRE, PE/OE, and FE may be jumpered in any order to EF1, EF2, EF3, and EF4. Because these bits are also available in the UART status register, the connections to the EF's are optional. Serial data in (SDI) may also be linked to EF1, EF2, EF3, or EF4.

Two connections are provided for the serial interface. J1 contains the 20-mA loop interface and J2 the EIA RS232C interface. These connections are right-angle headers and are labelled TTY and EIA, respectively. In addition, they are keyed by having one pin removed: pin 1 on J1 (TTY) and pin 5 on J2 (EIA). The mating socket for the connector should have the corresponding hole plugged so that the two connectors cannot be inadvertently misconnected.

Operation

Reference should be made to the technical data sheet for the CDP1854 UART for Mode 1 operation details.

The crystal-controlled oscillator circuit and the divide-by-N counter CD4059AE provide a clock for the UART at a frequency 16 times the rate selected by the user via the baud rate switch, as required by the UART.

The clear-to-send-in signal CTS-IN from the connector J2 to the UART may be left floating if desired, and it will assume the true state at the UART. The clear-to-send-out signal CTS-OUT is driven by the data-available signal DA from the UART with a trailing-edge delay. This signal may be used for handshaking, for example, between two UART Modules. This output may be made true all the time by changing Link 6 (LK6) to the A position.

To operate the paper-tape reader, an output instruction 67 is issued with the data byte containing a one in bit 7 (most significant bit). The J-K flip-flop U12 is triggered to the set state by this command, making the signal PT RDR low, which enables the tape reader. As soon as the tape reader starts to transmit data, the signal Serial Data In (SDI) causes the J-K flip-flop (U12) to be triggered to the reset state. As a result, one byte is transmitted to the UART and the tape is stopped before the next byte. Another 67 instruction, therefore, must be issued for each successive byte.

Literature

Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216.

Technical Data for the CDP1854, Universal Asynchronous Receiver/Transmitter (UART).

CDP18S508

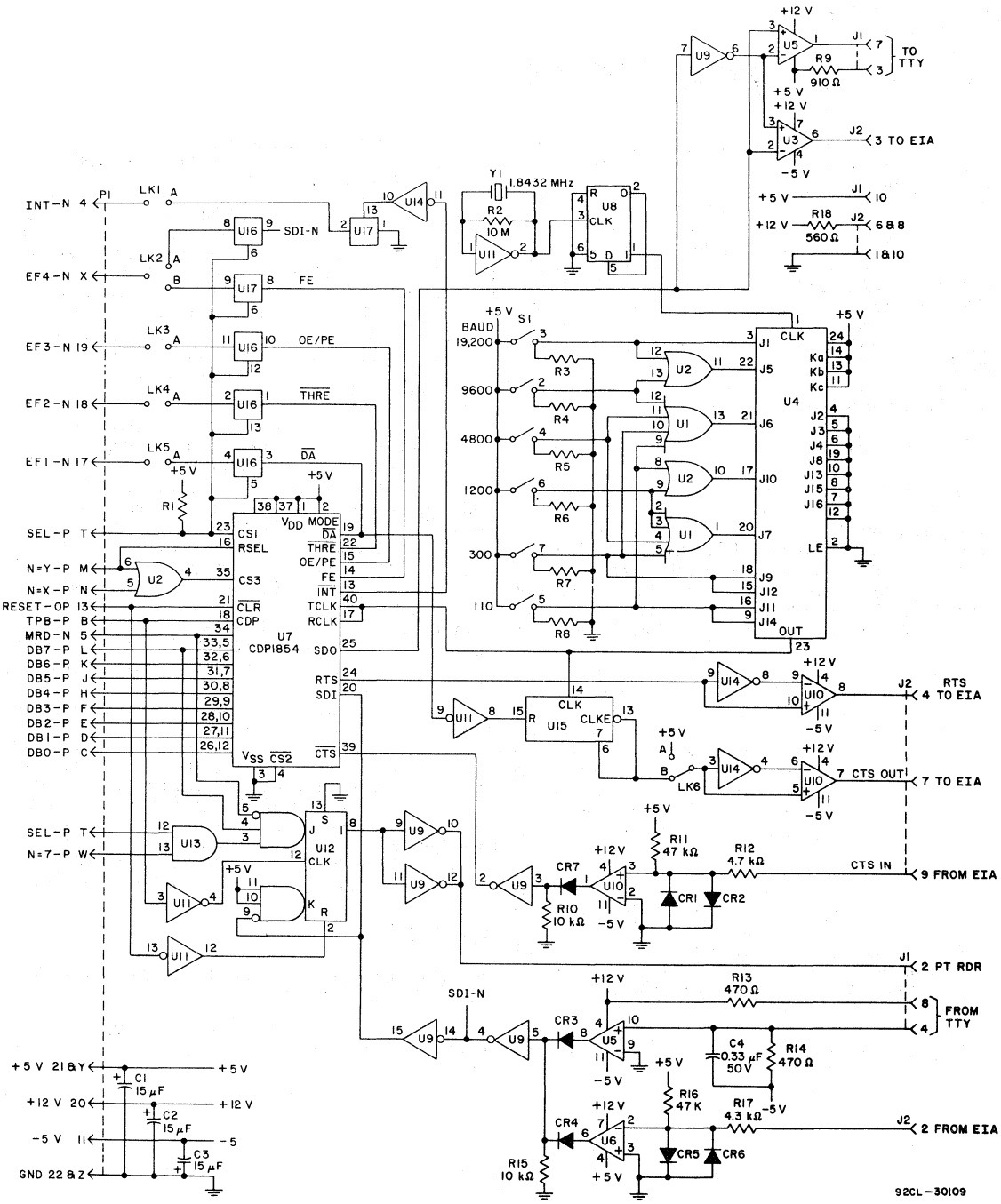


Fig. 1 – UART Interface Module CDP18S508 Logic Diagram

Parts List

C1, C2, C3 = 15 μF, ± 20%, 50 V
C4 = 0.33 μF, ± 20%, 50 V
CR1 through CR7 = 1N914
J1, J2 = connector (mates with connector comprised of
housing – AMP 1-86148-2
contact – AMP 86016-1
keying plug – AMP 87077-1)
R1, R3 through R8 = 22 kilohms, ± 5%, ¼ W
R2 = 10 megohms, ± 5%, ¼ W
R9 = 910 ohms, ± 5%, ¼ W
R10, R15 = 10 kilohms, ± 5%, ¼ W
R11, R16 = 47 kilohms, ± 5%, ¼ W
R12 = 4.7 kilohms, ± 5%, ¼ W
R13, R14 = 470 ohms, ± 5%, ¼ W
R17 = 4.3 kilohms, ± 5%, ¼ W
R18 = 560 ohms, ± 5%, ¼ W
S1 = DIP, 7 position
U1 = CD4072BE, dual 4-input OR gate
U2 = CD4071BE, quad 2-input OR gate
U3, U6 = CA3140S, op amp
U4 = CD4059AE, programmable divide-by-N counter
U5, U10 = CA324E, quad op amp
U7 = CDP1854, UART
U8 = CD4013BE, dual D-type flip-flop
U9 = CD4049BE, hex buffer/converter
U11, U14 = CD4069BE, hex inverter
U12 = CD4096BE, hex inverter
U13 = CD4081BE, quad 2-input AND gate
U15 = CD4017AE, decade counter/divider
U16, U17 = CD4016BE, quad bilateral switch
Y1 = 1.8432-MHz crystal

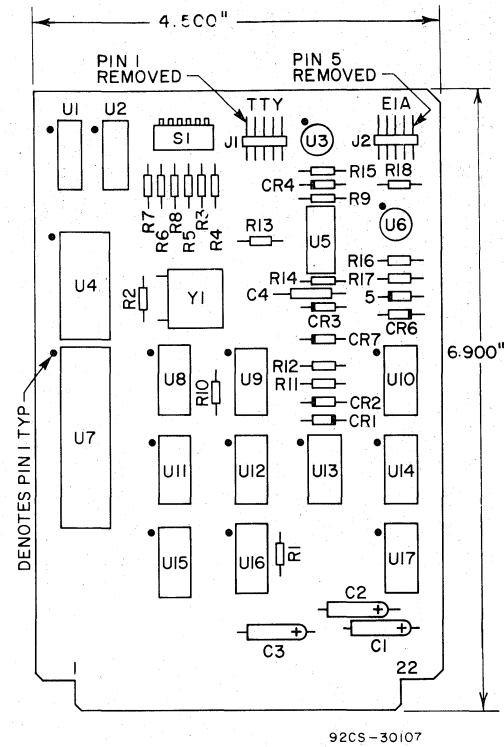


Fig. 2 – UART Interface Module CDP18S508 Layout Diagram

CDP18S510

COSMAC Byte I/O Module

The Byte I/O Module CDP18S510 is a printed-circuit card designed to provide the COSMAC Development System CDS II (CDP18S005) with four input-output channels, each one-byte (8 bits) wide. The Module provides two connectors with identical pin designations, each providing a one-byte input port and a one-byte output port as well as handshaking lines.

Installation

The Byte I/O Module CDP18S510 may be installed in any I/O slot in the CDS Card Nest. Slot 24 is usually used for disk and 14 for the terminal interface. Locations 14 through 18 and 21 through 24 provide all the signals required by this Module except the I/O address lines. These lines are chosen by the user. The combination of Select and N-Decode lines chosen must be unique so that no combination is used twice in the system. They are connected as follows:

Select – Wire-wrap to pin T the I/O select line chosen from SEL2 through SEL7 (SEL0 and SEL1 are assigned to specific I/O functions).

N Decode – Wire-wrap to pins M and N the decoded N lines chosen from N=1 through N=7. Pin M enables input port A and output port A; Pin N enables input port B and output port B.

Multiple Byte I/O Modules may be installed as required up to the availability of unique select addresses.

Operation

System Reset clears all ports.

The output ports latch the data at the trailing edge of TPB. The strobe output (OUT STB) signals that the data is latched. This pulse lasts until the leading edge of the next TPB (4 μs). A clear line is provided for resetting the data latches if desired. Two flag lines are provided to signal the system via EF2 and EF4. These signals may be used as data request signals, ready signals, or as two additional data bits.

The input ports latch the data at the trailing edge of the input strobe signal. When the input strobe is high, the latches are data following. A pull-up resistor is provided, therefore, so that this line may be unused. With the pull-up resistor, the input data is always available to the system. When an input strobe signal is used, the system is notified via EF1 or EF3 that a byte has been latched into the port. This flag line is also sent to the input device as INDA-N and its positive edge indicates that the system has taken the byte. If the input strobe is not used, no flags are generated.

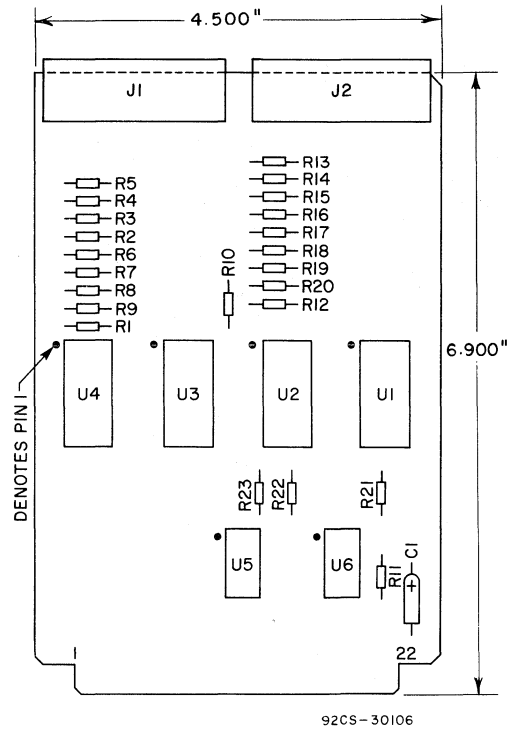


Fig. 1 – Byte I/O Module CDP18S510 Layout Diagram

Parts List

C1 = 15 μF, ± 20%, 20 V
J1, J2 = connector (mates with 34-contact ribbon cable connector 3M #3414-3000 or equivalent.
R1 through R23 = 22 kilohms, 5%, ¼ W
U1 through U4 = CDP1852D, 8-bit I/O port
U5 = CD4081BE, quad 2-input AND gates
U6 = CD4016AE, quad bilateral switch

Literature

Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216.

Technical Data for the CDP1852D, 8-Bit Input/Output Port.

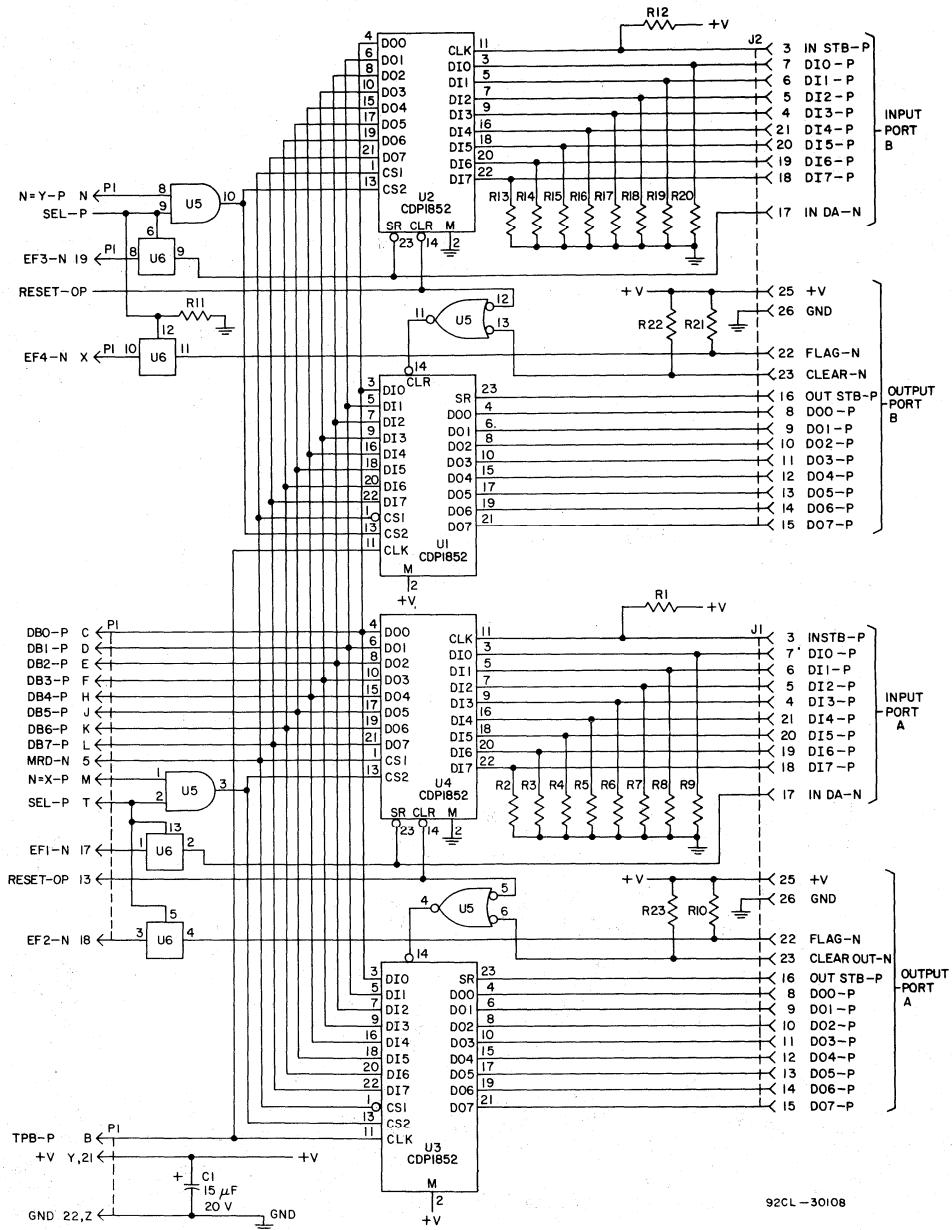


Fig. 2 – Byte I/O Module CDP18S510 Logic Diagram

CDP18S805V1, CDP18S805V3

COSMAC Floppy Disk System II

The COSMAC Floppy Disk System II (FDS) is a mass-memory storage unit designed to work with the CDP18S005 COSMAC Development System II (CDS II) to facilitate rapid program development. Use of the Floppy Disk System reduces program development time significantly in comparison with systems using other media. For example, assembly of a 1-kilobyte program takes approximately ten minutes when the FDS is used, as compared to approximately one hour with a 10-character-per-second paper-tape system.

The Floppy Disk System includes a dual-disk drive mechanism, interfacing hardware, special software for loading programs from the floppy diskette into memory, and special versions of the COSMAC Resident Editor, Assembler, and Utility programs. The two models are identical except that the CDP18S805V1 is designed for domestic use and operates on 115 V, 60 Hz, and the CDP18S805V3 is designed for international use and operates on 220 V, 50 Hz.

Features

The CDP18S805 Floppy Disk System consists of the following elements:

1. A dual-disk drive mechanism with cable (CDP18S801V1 or CDP18S801V3)
2. An interface module (CDP18S813)
3. A System diskette (CDP18S825) containing the following programs:
   a. **Level I, Level II, and MACRO assembler programs**
   b. Editor program
   c. Diagnostic program
   d. Tape-to-diskette transfer program
   e. Diskette copy program
   f. Memory save program
   g. ROM save program
   h. Printer program
   i. Diskette file examination program
   j. Change notice program
   k. Demonstration program
4. A blank diskette (CDP18S829)
5. Two instruction Manuals, MPM-217 and MPM-223

Installation of the Floppy Disk System CDP18S805 requires nothing more than plugging the interface module into the COSMAC Development System and the interfacing cable into the module. Disk loader and utility programs are already contained in the ROM in the CDS. System Diskette programs can reside in the RAM module supplied with the CDS II except for the Level II Assembler and the Macro Assembler which require an additional 4-kilobyte RAM module. A 12-kilobyte minimum RAM system is recommended for the Macro assembler.

Program Functions

The Disk Assembler and Editor programs are special versions of the standard COSMAC Resident Assembler and Editor programs optimized to work with the Floppy Disk System.

The Macro Assembler program extends the Level II Assembler facilities by providing macro and conditional assembly capabilities as well as several new logical features.

The diagnostic program is provided to verify diskette status. The tape-to-diskette transfer program provides a means for copying data stored on cassettes or paper tapes onto a diskette. The diskette copy program facilitates duplication of diskettes. The memory save program copies the CDS RAM data onto a diskette. The ROM save program does the same but puts data in ROM pattern format so that it may later be used as a basis for generation of ROM's. The printer program permits any diskette location to be output to a user-supplied printer. The diskette file examination program prints on the terminal the data bytes and the ASCII equivalents of any designated diskette location. The change notice program gives update information on the particular edition of software supplied.

A demonstration game program in assembly language is also provided on the diskette. The program may be assembled and loaded into the CDS by means of the software provided with the CDP18S005.

CDP18S805V1, CDP18S805V3

Specifications

CDP18S801 Dual-Disk Drive Mechanism

Power Requirements:
CDP18S801V1 – 115 V ac, 60 Hz, 250 W
CDP18S801V3 – 220 V ac, 50 Hz, 250 W

Dimensions:
Length 20-3/4 in., Width 19-1/4 in.,
Height 7-1/4 in.

Weight: 75 pounds, approx.

Cabling Supplied: AC power cord–5 feet;
CDS interface–4 feet

Number of Drives: 2

Total System Capacity: 512,512 bytes

Display Lights:
BUSY, CRC ERROR,
READY, DRIVE 0,
DRIVE 1

Operating Timing:
Seek
Track to track: 10 ms
Head Load and Settling Time: 40 ms max.
Max. Seek Time: 820 ms
Read/Write
Sector Read/Write Time: 6 ms
Average Latency: 83 ms

CDP18S813 Interface Module

Dimensions: 7.5 x 4.5 inches

Plugs into CDS II slot 24

CDP18S825 System Diskette

Programs Provided:
Assemblers, Editor, Diagnostic, Tape-to-Diskette Transfer, Diskette Copy, Memory Save, ROM Save, Printer, Diskette File Examination, Change Notice, Demonstration

Diskette Format:
IBM compatible
77 tracks per diskette
26 sectors per track
128 bytes per sector
256,256 bytes per diskette

Other Required System Components

COSMAC Development System II (CDP18S005)

Terminal: Serial ASCII 20-mA or EIA RS232C interface, 110-1200 baud

Blank Diskettes (CDP18S829) as required

Available Options

Binary Arithmetic Fixed-Point Subroutine Diskette CDP18S826.

Binary Arithmetic Floating–Point Subroutine Diskette CDP18S827.

Micromonitor Operating System (MOPS) CDP18S831.

microFORTH System CDP18S820. (microFORTH is a product of FORTH, Inc., 815 Manhattan Beach, Calif., This software is not compatible with standard RCA software for the CDS II. Technical support of microFORTH customers is provided by FORTH, Inc., (213) 372-8493).

Literature

A manual detailing the hardware and installation instructions for the Floppy Disk System II and describing the software and operating instructions is included with the system: **RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual, MPM-217.** Also included is the **Instruction Guide for the COSMAC Macro Assembler (CMAC), MPM-223.**

CDP18S820

microFORTH System for the CDP1802 COSMAC Microprocessor

The microFORTH System CDP18S820 is a complete self-contained software package for use with the RCA COSMAC Development System II (CDP18S005) having a minimum of 8 kilobytes of RAM and equipped with a Floppy Disk System (CDP18S805). Independent of all other RCA software, it provides its own I/O terminal interface software, a floppy-disk file-management system including an editor, and, most important, an interactive higher-level language environment for the design and implementation of application software.

Based on modern stack structures and an appropriate set of program flow concepts, the microFORTH System encourages structured programming—the best way to generate reliable code quickly. Its compiler/interpreter is optimized for code compactness and is designed to permit "line-at-a-time" compiling and execution, thereby providing immediate interactive debugging of each routine as it is conceived. This interactive feature makes it possible for even novice programmers to generate useful development system programs easily and quickly.

The microFORTH System includes its own **assembler**, making it easy to incorporate machine language inserts. The system is designed so that sophisticated users may extend the language and add data types where required. Every logical construct is easily redefinable. A **cross-compiler** is also provided to permit a more advanced programmer to convert operating programs to a form suitable for storage in the ROM of a COSMAC microprocessor-based controller.

The microFORTH system for the CDP1802 is compatible with microFORTH systems available from FORTH, Inc., for other microprocessors such as the 8080, 6800, and Z-80. Also, the microFORTH systems closely resemble the FORTH systems available on several minicomputers. The microFORTH system, however, uses different I/O and subroutine conventions than the standard software supplied with the COSMAC Development System CDP18S005.

Subsystems Provided

The following subsystems, written in microFORTH, are provided on the microFORTH diskette.

1. **On-line Compiler/Interpreter.** This subsystem accepts sequences of function names from the disk or from the keyboard. It uses a simplified syntax that encourages abundant nesting of definitions. New functions are easily expressed in terms of other previously defined high-level routines. Each name is either assembled into an on-line symbol table or executed, as appropriate. Unrecognized names are reported immediately. Families of names are linked into user-specified "vocabularies".

   The system maintains two stacks: one for program linkage and one for parameter passing. All built-in facilities communicate via the stacks so that user programs that behave similarly are easily accommodated. As a result, typical microFORTH program interfaces are logically direct and easy to describe.

2. **On-line Editor.** This subsystem is used to modify user source programs on diskettes.

3. **On-line Assembler.** This subsystem is used to code special routines such as unique I/O interfaces or subprograms for which execution time constraints are particularly stringent. It is normally used sparingly.

4. **On-line Utilities.** These subsystems are used for documentation purposes (printing listings or indexes) or for copying or error-checking diskette portions.

5. **Cross-compiler.** This subsystem is used to convert a working program on the development system, as well as microFORTH itself, into a compacted version (512 bytes minimum) suitable for storage in a ROM of a CDP1802-based controller. It requires, first, a development system having at least 12 kilobytes of RAM and, second, a user with substantial programming expertise.

CDP18S820

microFORTH Documentation

The microFORTH system diskette programs are supplied almost entirely in microFORTH source code. Simple instructions for loading the system are also provided. Two manuals are supplied to the user. The **microFORTH Primer** contains all introductory concepts and sufficient information to permit coding and running. The **microFORTH Technical Manual** contains further details on system structure and functions as well as additional explanations of the more sophisticated properties of the system. It also contains a detailed description of the Cross-compiler.

Technical Support

The microFORTH System converts the COSMAC Development System II into an extremely effective, highly interactive stand-alone operating system. Facilities are provided that permit the user to extend or modify the system, where desired. Use of the Cross-compiler requires a detailed knowledge of some of the more esoteric features of the system and should not be attempted by the novice user.

By agreement with RCA, the developers of the system (FORTH, Inc., 815 Manhattan Ave., Manhattan Beach, Calif. 90266) will directly support users by answering questions and providing supplementary documentation. Telephone number: (213) 372-8493.

Summary of microFORTH System Requirements

Hardware Requirements

CDP18S005 COSMAC Development System II
CDP18S805 COSMAC Floppy Disk System II

Minimum RAM Requirements

8 kilobytes for basic microFORTH subsystems
12 kilobytes for both Cross-compiler and basic subsystems

Terminal Requirements

Serial ASCII data terminal with baud rate of 300
Other speeds optional

CDP18S820 System Components

1. Diskette
2. Primer
3. Technical Manual
4. Loading Instructions

CDP18S826V1, CDP18S826V2

COSMAC Microprocessor Fixed-Point Binary Arithmetic Subroutines

The Binary Arithmetic Subroutine Package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines designed to be operated on COSMAC CDP-1802 Microprocessor systems. The subroutines are coded in Level I assembly language and require 1 kilobyte of memory space. A detailed description of these subroutines is given in the Manual **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206A.

The subroutines are available on a floppy diskette, paper tape, cassette, and on a ROM. In source language, they are available on floppy diskette CDP18S826 for use with RCA Floppy Disk System CDP18S805, a mass memory storage unit designed to work with the CDP18S005 COSMAC Development System (CDS II). The subroutines are also available on paper tape, CDP18S826V1, and on a magnetic-tape cassette, CDP18S826V2, for a TI Silent 700 Data Terminal*. In object code, the package is available in a single 1-kilobyte ROM, CDPR582CD (4- to 6.5-volt operation) or CDPR582D (4- to 10.5-volt operation). In addition to the binary arithmetic subroutines, the ROM contains the code for the Standard Call and Return Technique. The ROM contains its own address latch and is located in memory at hexadecimal locations C000 through C3FF.

Functions

The Binary Arithmetic Subroutine Package includes 31 subroutines. Fifteen of these are binary arithmetic subroutines, fourteen are utility subroutines, and two are for format conversion. Appropriate selections from the set of subroutines may be made for the calculations required in a specific application.

Arithmetic Functions. The arithmetic functions included in this package are:

1. 16-bit 2's-complement addition
2. 16-bit 2's-complement subtraction
3. 16-bit 2's-complement multiplication yielding 32-bit products
4. 32-bit 2's-complement division yielding 16-bit quotient and remainder.

Format Conversion. In addition to the arithmetic functions, two format-conversion subroutines are included for interfacing the system to binary-coded-decimal-oriented peripheral hardware. These subroutines provide BCD-to-binary and binary-to-BCD conversions.

Utility Subroutines. A set of special utility subroutines allows the user to save and restore a group of registers on a stack or at a user-defined RAM area. These registers are used by the arithmetic function subroutines to store an operand and to point to an operand in memory. Other utility subroutines compare 16-bit operands and give indication if a register is greater than or equal to an operand.

The Standard Call and Return Technique, described in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201, is used for all the subroutines.

Timing

Timing measurements at a 6.4-MHz clock rate for the best and worst cases of the various arithmetic and format conversion subroutines for the CDP1802 are given in the tabulations at the right. These times were determined by taking an ad hoc sample of large and small numbers and performing an operation upon them. Absolute best and worst case values may vary from the values listed here.

Arithmetic Function	Best (ms)	Worst (ms)	Format Conversion	Best (ms)	Worst (ms)
Add	0.041	0.068	Binary to BCD	1.33	2.82
Subtract	0.039	0.078			
Multiply	0.851	1.29	BCD to Binary	0.094	0.81
Divide	1.37	1.78			

Literature

Further information on the Fixed-Point Binary Arithmetic subroutines, including a complete listing for all the subroutines, is given in the Manual **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206A. General information on the RCA 1800 microprocessor series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

Another arithmetic software package is described in Product Description PD7 for the COSMAC Floating-Point Arithmetic Subroutine Diskette CDP18S827. Additional information on the Floating-Point Package is given in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207.

*Registered trademark, Texas Instruments Corporation.

CDP18S827

COSMAC Floating-Point Arithmetic Subroutine Diskette

The COSMAC Floating-Point Arithmetic Subroutine package on a floppy diskette CDP18S827 is a set of 32-bit arithmetic subroutines designed to be operated on COSMAC CDP1802 Microprocessor Systems including the COSMAC Development System (CDS) CDP18S005. The subroutines are coded in Level I assembly language and require approximately 2 kilobytes of memory space. The floating-point binary number is represented by eight exponent bits and 24 mantissa bits. The most significant bit of each indicates the sign. The range of decimal numbers that can be represented by the 32 bits is $0.294 \times 10^{-38} \leqslant \text{FPN} \leqslant 1.7014 \times 10^{38}$

A detailed description of these subroutines is given in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207. The subroutines are available in source language on a floppy diskette CDP18S827 for use with RCA Floppy Disk System CDP18S805, a mass memory storage unit designed to work with the CDP18S005 COSMAC Development System (CDS). The Floating-Point Arithmetic Subroutine Diskette can also be used with Floppy Disk System CDP18S800 and the CDP18S004 COSMAC Development System.

Functions

The Floating-Point Arithmetic Subroutine Diskette CDP18S827 includes 18 subroutines. Ten are arithmetic subroutines, six are utility subroutines, and two are for format conversion. Appropriate selections from the set of subroutines may be made for the calculations required in a specific application.

Floating-Point Arithmetic Subroutines. The arithmetic functions included in this floating-point arithmetic package are:

1. 32-bit addition
2. 32-bit subtraction
3. 32-bit multiplication yielding 32-bit products
4. 32-bit division yielding 32-bit quotient
5. Transcendental function: sine
6. Transcendental function: cosine
7. Transcendental function: arctan
8. Natural log
9. e^X
10. Square root

Utility Subroutines. A set of special utility subroutines allows the user to save and restore a group of registers on a stack. These registers are used by the arithmetic function subroutines to store an operand. Other utility subroutines allow constants to be pushed onto the stack.

Format Conversion Subroutines. Two format-conversion subroutines are included for interfacing the system to binary-coded-decimal-oriented peripheral hardware. These subroutines provide BCD-to-floating-point and floating-point-to-BCD conversions.

The Standard Call and Return Technique described in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201, can be used for all the subroutines.

Timing

Timing measurements at a 6.4-MHz clock rate for the best and worst cases of the various arithmetic and format conversion subroutines for the CDP1802 are given in the tabulation below. The timing, however, can be rescaled by a change in the system clock rate.

Arithmetic Function	Best (ms)	Worst (ms)	Format Conversion	Best (ms)	Worst (ms)
Add	0.53	7.8	Floating-Point-BCD	2.3	7.5
Subtract	0.81	8.1			
Multiply	43.8	47.5	BCD-Floating-Point	7.5	1600
Divide	30	32.5			
Sine	113	116			
Cosine	102	113			
Arctan	85.9	109			
Natural log	78.1	188			
e^X	71.9	125			
Square root	155	312			

Literature

Further information on the Floating-Point Arithmetic Subroutine Package CDP18S827, including data storage convention and register allocation, is provided in the Manual **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors** MPM-207. General information on the RCA1800 microprocessor series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor** MPM-201. Another software package encompassing 16-bit 2's-complement arithmetic is described in the manual **Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206.

CDP18S831
COSMAC
Micromonitor Operating System (MOPS)

The Micromonitor Operating System (MOPS) is a software package developed to enhance the capabilities of the RCA CDP18S030 Micromonitor. The Micromonitor is a self-contained, powerful debugging tool for use with any system based on the CDP1802 COSMAC Microprocessor. It permits in-circuit debugging in real time so that both hardware and software problems can be efficiently identified. The Micromonitor Operating System (MOPS) CDP18S831 enhances Micromonitor performance by providing user access to the processing and storage capabilities of the COSMAC Development System CDP18S005 equipped with the Floppy Disk System CDP18S805.

The Micromonitor Operating System CDP18S831 includes a MOPS Diskette CDP18S830, a UART Module CDP18S508, and a Connecting Cable CDP18S511.

System Functions

The Micromonitor Operating System CDP18S831 provides an extended Micromonitor-type command set with commands of the following types:

1. Commands that allow the user to conveniently switch Micromonitor commands and responses to and from a variety of system peripherals.
2. Single commands that allow a more complete interrogation of the CPU state.
3. Commands for saving the system-under-test memory, registers, etc., in a disk file or for loading the system-under-test from a disk file.
4. Commands that allow a degree of automation in system debugging and testing.

With MOPS, the debugging techniques available to the user range from simple terminal-Micromonitor dialog to fully automated hands-off system testing with commands coming from disk files.

System Operation

The user system configuration required for the utilization of MOPS is shown in Fig. 1. Depending on user directives, commands to the system are input at the terminal or are taken from command files on disk. Likewise, system responses can be directed to the terminal, to a disk file, or to both.

Standard Micromonitor commands entered to the system are directed to the Micromonitor through its serial interface, UART Module CDP18S508. Commands from the extended MOPS command set are "trapped" and processed by the operating system. In either case, the Micromonitor Operating System provides line-by-line command editing capability.

Support Systems

The **COSMAC Micromonitor CDP18S030** is a self-contained, real-time, in-circuit hardware and software debugging tool for use with any CDP1802 Microprocessor system. It has a built-in keyboard and display, status indicator lights, software debugging routines, and a 20-mA loop or EIA RS232C interface for auxiliary serial communication. Its primary use is for prototype-system software and hardware debugging. Because of its easy portability, however, it is also useful as a field service tool. In addition, it can be used as a versatile production tester. (Part number: CDP18S030; Product Description: PD18; Instruction Manual: MPM-218)

The **COSMAC Development System II** (CDS) CDP18S005 is an interactive software and hardware prototyping system for the development of products based on the RCA1800 family of microprocessor parts. It uses the CDP1802 Microprocessor as the CPU and includes a RAM-

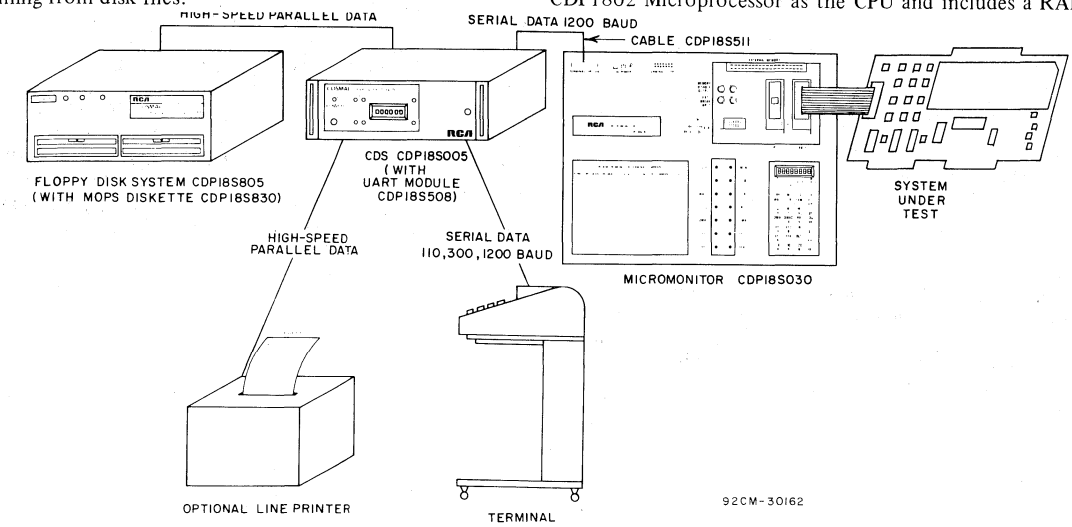


Fig. 1 — System configuration for utilization of MOPS software.

based resident Editor and Assembler. The CDS has space for additional I/O devices so that it can be used for hardware prototyping as well as program development. In small-volume applications it can be used as the major building block for dedicated microcomputers. (Part number: CDP18S005; Product Description: PD16; Instruction Manual: MPM-216)

The **COSMAC Floppy Disk System II** CDP18S805 is a mass-memory storage unit designed to work with the CDP18S005 COSMAC Development System II to facilitate rapid program development. In comparison with systems using other media, the Floppy Disk System reduces program development time significantly. It includes interfacing hardware and special versions of the COSMAC Resident Editor and Assembler and Utility programs. (Part number: CDP18S805; Product Description: PD17; Instruction Manual: MPM-217)

Literature

The **Micromonitor Operating System (MOPS) CDP18S831 Users' Guide** MPM-231, describing the installation, startup, and use of MOPS, is included with the unit.

System Components

Supplied as part of the Micromonitor Operating System (MOPS) CDP18S831 package are the following items:

MOPS Diskette CDP18S830 (Containing both 4- and 8-kilobyte RAM versions)
UART Module CDP18S508
Interconnecting Cable CDP18S511
Micromonitor Operating System (MOPS) CDP18S831 Users' Guide MPM-231

Summary of MOPS Commands

$TI	Set the terminal as the input device
$TO	Set the terminal as the output device
$DKI uutt	Set the disk as the input device
$DKO uutt	Set the disk as the output device
$DKC	Close a disk file
$O uutt	Set both terminal and disk as output devices
?CPU	Dump the CPU state to the output device(s)
?MRn h	Dump memory pointed to by register n for h bytes
$Hssss eeee uutt	Hold the state of the machine on disk
$L uutt	Load a disk file
$MSG	Type a message to the terminal
$WB	Wait for a break condition or the break key
$WT d	Wait for d seconds or the break key
!J d	Set the index J to d (a decimal number)
!J+	Increment the index J
!J–	Decrement the index J
?J	Question the current value of the index J
$GO TO %*label*	Search forward for %*label* and if found continue at that point, else end
$IF *v1 op v2* THEN GO TO %*label*	If the relation is true, execute "go to", else proceed
$DKW uutt	Write a command sequence to a disk file
$DKL uutt	List a disk file to the terminal
$DKP uutt	Print a disk file to the line printer
$U	Return to the utility program

CDP18S834

Basic 1 Compiler/Interpreter CDP18S834 for Use with COSMAC DOS Development System (CDS III)

The Basic 1 Compiler/Interpreter, provided on a diskette, is a high-level language software package designed to simplify program development on the COSMAC DOS Development System (CDS III) CDP18S007V1 and V3. An excellent language for the beginner, Basic 1 is easily learned and facilitates the rapid development of elementary application programs. A feature of Basic 1 is that it can form the core of a system whose facilities, limited only by the system memory, may be extended indefinitely by the addition of machine language routines.

The Basic Compiler/Interpreter gives the user the option of (1) developing and running programs in Basic 1 directly, or (2) converting these programs to executable object code capable of running at a greater speed.

The **interpreter** allows the user to write programs in Basic 1 with line numbers for later execution or without line numbers for immediate execution. The disk-related statements incorporated in the interpreter allow the programmer to save programs on a floppy disk for later recall.

The **compiler** enables the programmer to take any stored program written in Basic 1 and translate it into assembly language, giving the user the flexibility of specifying where in memory the program, variables, and stack are to reside. The output of the compiler is assembled by the COSMAC assembler (ASM2) to produce the executable object code. Programs compiled and assembled run at speeds much greater than those run directly through the interpreter.

Basic 1 Features

The Basic 1 Compiler/Interpreter can handle lines of up to 70 characters in length. Line numbers can range from 1 to 32767. Multiple statements per line are accepted. Numbers can be entered in decimal (−32767 to +32767) or hexadecimal (#0000 to #FFFF). Variables are designated by any single capital letter.

Basic 1 performs fixed-point arithmetic. Expressions are composed of one or more numbers, variables, and/or functions joined together by operators (+, −, /, *, @) and possibly grouped by parentheses. Expressions are evaluated modulo 2^{16}.

The functions Basic 1 has in its repertoire include MOD, AND, OR, XOR, MAX, MIN, SGN, ABS, HEX, RND, and USR. The USR function is important in that it allows the user to extend the features of Basic 1 by means of machine language subroutines.

The types of statements available to the programmer include the following:

Comments and Declarations: REM, !
Assignment: LET
Control: GOTO, GOSUB, RETURN, END
Conditional: IF
Input/Output: INPUT, PRINT, OUTPUT, INP
Disk Related: WFLN, RFLN, DOUT, DIN, CLOSE, WEOF, TIN, TOUT, NOUT
System Control: NEW, RUN, LIST, RDOS

Loading and Operating Basic 1

Loading and operating Basic 1 on the COSMAC DOS Development System is a simple procedure. To load the interpreter, the user places the disk in one of the disk drives and types BASIC1.INT:X where X is the drive (0 or 1) the disk has been placed in. This command loads the interpereter. The program initializes itself and then delivers its colon prompt ":" to indicate it is now in the enter mode and the user can begin entering a Basic 1 program.

To load the compiler, the user places the disk in one of the disk drives and types BASIC1.CMP:X, where X is the drive (0 or 1) the disk has been placed in. This command loads the compiler and begins execution. The compiler then issues its normal user prompts.

Error Messages and Program Debugging

Whenever the Basic 1 interpreter detects an error in a statement, it generates an error message consisting of an exclamation point "!" followed by a decimal number. The number signifies the type of error. If an error is detected during program execution, the line number of the offending statement is also given. Basic 1 lends itself to the use of dummy stop or print statements to reveal whether the flow within the program is proper or to permit the examination of variables at convenient points during program execution.

Literature

Further information on Basic 1 Compiler/Interpreter is given in the Manual **Use of Basic 1 Compiler/Interpreter CDP18S834 with the RCA COSMAC DOS Development System (CDS III)**, MPM-234.

Information on the RCA COSMAC DOS Development System CDP18S007V1 and V3 is given in the manuals **Operator Manual for the RCA COSMAC DOS**

Development System (CDS III) CDP18S007, MPM-232, and in the **Hardware Reference Manual for the RCA COSMAC DOS Development System (CDS III) CDP18S007**, MPM-233.

General information on the RCA 1800 Microprocessor Series, including software, programming techniques, and architecture, is given in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201.

Binary arithmetic software packages on disk are also available for use on the COSMAC DOS Development System CDS III. The COSMAC Microprocessor Fixed-Point Binary Arithmetic Subroutines (CDP18S826) are described in Product Description PD6 and the COSMAC Microprocessor Floating-Point Arithmetic Subroutines (CDP18S827) are described in Product Description PD7. Additional information on these arithmetic diskettes is given in the manuals **Fixed-Point Binary Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-206, and in **Floating-Point Arithmetic Subroutines for RCA COSMAC Microprocessors**, MPM-207.

CDP18S837
RCA COSMAC Disk Operating System Upgrade Package

This booklet discusses the components of RCA COSMAC Operating System Upgrade Package CDP18S837 and gives instructions for modification of the RCA COSMAC Development System (CDS II) CDP18S005 to incorporate and utilize the software for the COSMAC Disk Operating System (CDOS). These instructions apply to CDS II model CDP18S005 having a RAM complement expanded to 12 kilobytes and equipped with Floppy Disk System (CDP18S805 V1, V2, or V3).

Terminal Requirements

A data terminal having the following characteristics is required:

1. EIA RS232C or 20-mA loop interface.
2. Selectable baud rates (110, 300, 1200, 4800, 9600, or 19,200 baud).
3. Parity disable feature (parity is not generated or checked by CDS II).
4. ASCII code with eight data bits and one or more stop bits (CDS generates two stop bits).

NOTE: Item four is under software control and may be changed by the user program. For further information consult the **Operator Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007**, MPM-232.

The standard cables supplied with the CDS II and the Floppy Disk System are sufficient for the interconnections between the system components. No additional cabling changes are required.

Upgrade Package CDP18S837

The RCA COSMAC Disk Operating System Upgrade Package CDP18S837 includes the following items:

1 CDP18S621	RCA COSMAC Microboard 16-Kilobyte RAM,
or	
2 CDP18S623	RCA COSMAC Microboard 8-kilobyte RAM
1 CDP18S508	RCA COSMAC UART Interface Module
1 UT21	2708 PROM programmed with Utility Program UT21
1	CDOS System Diskette
1 MPM-232	**Operator Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007**
1 PD19	Product Description for UART Interface Module CDP18S508
1	Data Bulletin for UART CDP1854
1 MB-621	Product Description for Microboard 16-Kilobyte
or	RAM CDP18S621,
1 MB-623	Product Description for Microboard 8-Kilobyte RAM CDP18S623
1 PD37	RCA COSMAC Disk Operating System Upgrade Package CDP18S837
1	Warranty Card

Description of New Components

The modifications required to incorporate the CDOS Disk Operating System software with the CDS II include the installation of memory modules, the extraction of the Terminal Interface Module, the insertion of the UART Module, and the addition of PROM UT21, a programmed 2708 containing Utility Program UT21. A brief description of the functions of these new components follows.

Memory Modules

The minimum RAM required for CDOS operation includes 12 kilobytes in the address range 9000 - BFFF and 12 kilobytes in the address range 0000 - 2FFF. CDOS loads and runs in the upper memory area. Other system programs, such as the Macroassembler and Editor, load starting at address 0000. The CDP18S837

Upgrade Package includes 16-kilobytes of RAM but assumes that the system to be modified already has at least 8 kilobytes of additional RAM beyond the 4 kilobytes supplied with the basic CDS. If additional RAM is needed, extra RAM modules such as the CDP18S205V1 4-Kilobyte RAM, the CDP18S620 Microboard 4-Kilobyte RAM, or the CDP18S623 Microboard 8-Kilobyte RAM should be ordered and installed.

Fig. 1 shows a memory map of CDS III. The 16 kilobytes of RAM supplied with this Upgrade Package will be located in low memory and the existing 12 kilobytes of RAM, assumed to be in modules of 4 kilobytes each, will be moved to upper memory. Installation instructions for this changeover are given in the subsequent section **Installation and Assembly**.

Any additional memory in the area below address 8000 will be used by the Editor to expand its buffer area or by the Macroassembler as extra area for symbol tables and macro definitions. It is necessary, however, to keep RAM contiguous in the area below 8000.

Several different kinds of RAM modules in both the Microboard and the CDS series are available for memory expansion. Installation instructions for these modules are provided in the appropriate product description or instruction manual. For CDS memory modules not containing on-board bank-select decoding, the Bank Select Signals generated by the CDS Address Latch and Bank Select Module CDP18S206 can be used as board enables. Refer to the section "Memory Addressing and Expansion" in the **Operator Manual for the RCA COSMAC Development System II CDP18S005, MPM-216**, for more details on this subject. Table I gives a summary of the Memory Bank Select signals.

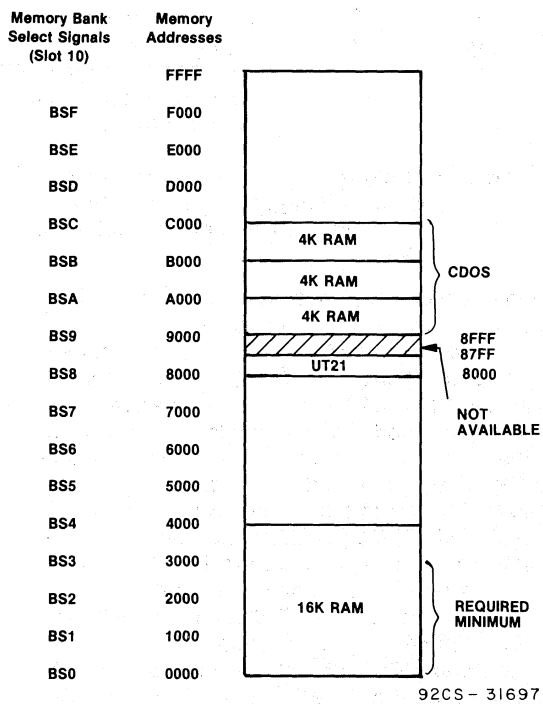


Fig. 1 - CDS III memory map.

Table I - Memory Bank Select Signals

Signal Name	Slot 10 Pin No.	Address Range Enabled	Notes
BS0-P	W	0000-0FFF	1
BS1-P	20	1000-1FFF	1
BS2-P	19	2000-2FFF	1
BS3-P	L	3000-3FFF	
BS4-P	K	4000-4FFF	
BS5-P	J	5000-5FFF	
BS6-P	H	6000-6FFF	
BS7-P	F	7000-7FFF	
BS8-P	E	8000-8FFF	2
BS9-P	C	9000-9FFF	3
BSA-P	5	A000-AFFF	3
BSB-P	4	B000-BFFF	3
BSC-P	3	C000-CFFF	
BSD-P	M	D000-DFFF	
BSE-P	A	E000-EFFF	
BSF-P	N	F000-FFFF	

Note: 1. Required minimum.
2. Do not use; assigned to Utility Program.
3. Required for CDOS.

CDP18S837

UART Module

Terminal communications for the upgraded CDS II are performed through the UART Interface Module CDP18S508. The Terminal Interface Module CDP18S507 must be removed from slot 14 to avoid conflict between the two interfaces. If more than one UART Module is used in the system, the one used as the terminal interface should be appropriately marked.

The UART Module will be under Group 1 control, just as the original Terminal Interface Module was, and will not interfere with any other modules under different Group Select numbers.

The following I/O assignments are made for the UART Module:

Instruction		Action
62	OUT 2	Writes data to the Transmitter Holding Register.
6A	IN 2	Reads data from the Receiver Holding Register.
63	OUT 3	Writes a Control byte to the UART.
6B	IN 3	Reads Status bytes from the UART.
67	OUT 7	Controls PT RDR output; not presently used.

Signals between the UART module and the terminal are given in Table II. Note that not all UART signals are actually sent through the standard cables.

Table II - Terminal Interface Cabling

CDS Side P1	Terminal Side P2	Signal
Teletypewriter Terminal (TTY)		
8	6	Data from TTY (Current Source)
7	8	Data to TTY (Current Source)
3	7	Data to TTY (Current Return)
4	5	Data from TTY (Current Return)
10	15	$+V_{DD}$
2	13	Paper Tape Control
EIA RS232C Terminal		
P1	**P2**	**Signal**
1	1	Ground
2	2	Data to CDS
3	3	Data to Terminal
10	7	Signal Ground
7	8	Clear to Send from CDS*
6	6,5	Data Set Ready - Held High by CDS

*Note: This signal can be permanently enabled (high) by changing link LK6 on the UART Module to connect C to A instead of C to B.

Utility Program UT21

To handle the data terminal interfacing via the UART module, a new Utility Program UT21 is provided in the UT21 PROM (a programmed 2708). Details of this new Utility Program are given in the **Operator Manual for the RCA COSMAC CDOS Operating System (CDS III) CDP18S007**, MPM-232. In summary, all old commands such as ?M and $U are identical. A new command, $C, causes CDOS to load automatically if the system diskette is in drive 0. It is equivalent to the $L command with unit 0 and track 01 used automatically.

A second difference is that a carriage return or line feed character is not necessary after the RESET, RUNU sequence to establish the terminal baud rate. That rate is established in hardware by switches on the UART module. The asterisk prompt character "*" will appear immediately after a RESET, RUNU sequence and the CDS will be ready for operation in the full-duplex mode. If half duplex is desired instead, the **first** character typed must be a Line Feed. Operation will then proceed in half duplex. Thus, the startup procedure for UT21 is identical to that of UT20 for half-duplex operation. For full-duplex operation, however, the initial Carriage Return can be omitted.

The routines in the UT20 concerned with terminal timing have been eliminated from the UT21, and READ operations may be immediately followed by TYPE's without a delay. Consequently, the routines TIMALC, DELAY, and

TYPE5D are not shown in the **Operator Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007**, MPM-232. The effects of calling DELAY (for example, from a previously written program) will simply be an immediate return to the caller without any delay being generated. Calling TYPE5D is the same as calling TYPE5. Register RC must still contain #80EF, as before, when UT21 routines are called. Programs using TIMALC will require modification to permit use with UT21.

Floppy Disk Interface

No change is required to the Floppy Disk interface. If the CDS is not already equipped with a Floppy Disk System, one should be ordered (CDP18S805V1 for 115 V, 60 Hz operation or CDP18S805V3 for 220 V, 50 Hz) and installed in accordance with the instructions given in the **RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual**, MPM-217.

Installation and Assembly

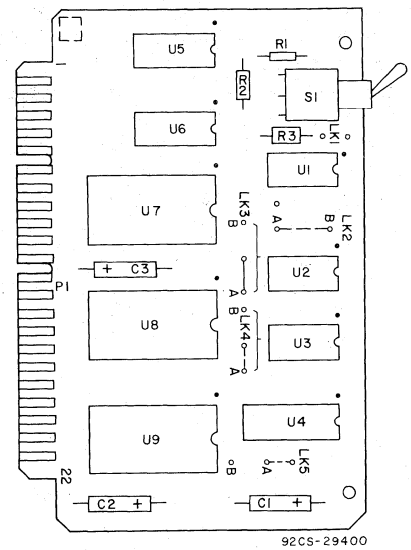
This section provides detailed installation and assembly instructions for modifying a CDS II equipped with Floppy Disk Option for operation with the COSMAC Disk Operating System (CDOS) software. Because many of the slots in the CDS backplane are keyed, it may be necessary to remove or adjust the keys to accommodate the new modules when the modifications described below are made.

Utilization of UT21 Utility Program

UT20 is contained in its entirety in two PROM's (U7 and U9) on the ROM/RAM module CDP18S401. Only one of these PROM's (U7), however, needs to be changed to upgrade to UT21. Two procedures are provided for modifying a CDS II to utilize the UT21 Utility Program. Procedure A substitutes the UT21 for the UT20 program and permits utilization of the Microterminal CDP18S021 option. Procedure B adds the UT21 capability and permits switching to either UT20 or UT21 by means of S1. Procedure B, however, does not permit use of the Microterminal CDP18S021.

Procedure A - Substitution of UT21 for UT20

1. Remove the ROM/RAM module CDP18S401 from slot 9 of the CDS II module nest.
2. Remove ROM U7 from its socket on the module. See Fig. 2.
3. Install the PROM UT21 provided with the Upgrade Package into socket U7. Be careful to observe polarity.
4. Make sure Switch S1 is in the down position.
5. Re-insert the modified ROM/RAM module CDP18S401 into slot 9.



C1, C2, C3 = 15 μF, ±20%, 20 volts
R1, R2, R3 = 22 kilohms, ±5%, ¼ watt
S1 = SPDT
U1 = CD4023BE U5, U6 = CDP1856D
U2 = CD4069BE U7, U9 = 2708
U3 = CD4012BE U8 = Socket for Microterminal
U4 = CDP1824D or UT21 ROM

Note:
S1 UP enables ROM in U8.
S1 DOWN enables ROM in U7.

Fig. 2 - ROM/RAM Module CDP18S401 layout diagram.

CDP18S837

Procedure B - Addition of UT21

1. Remove the ROM/RAM module CDP18S401 from slot 9 of the CDS II module nest.
2. Install PROM UT21 into socket U8. Be careful to observe polarity.
3. Re-insert the modified ROM/RAM module CDP18S401 into slot 9.
4. Switch S1 into the up position.

Installation of Memory Modules

The Upgrade Package contains either one CDP18S621 16-kilobyte RAM or two CDP18S623 8-kilobyte RAM's. The installation instructions for these components are given in Step B below. It is assumed that the RAM modules present in the CDS II are the CDP18S205V1 4-kilobyte RAM's. The instructions for the relocations of the addresses for the CDP18S205V1 RAM's are given in Step A below.

Step A - Module CDP18S205V1 (4 kilobytes)

1. Remove the three RAM modules from the CDS II module nest.
2. Perform the following CDS II backplane modifications:
   a. Connect slot 10, pin C to slot 8, pin X (BS9)
   b. Connect slot 10, pin 5 to slot 7, pin X (BSA)
   c. Connect slot 10, pin 4 to slot 6, pin X (BSB)
3. Insert CDP18S205 RAM modules into slots 6, 7, and 8.

Step B - Microboard CDP18S621 (16 kilobytes)

1. Connect pins 1 and 16 of link LK2A.
2. Set both rockers of switch S1 to "open".
3. Install Microboard CDP18S621 into any unused CDS II memory slot (1 to 5).
4. Add jumper wire on CDS II backplane from slot 10 pin D to pin 3 of any slot 1 through 9 (RNU-P signal).

Step B (alternate) - Two CDP18S623's (8 kilobytes each)

1. Connect pins 1 and 16 of link LK2A.
2. On one CDP18S623 RAM, set rockers 1, 2, and 3 of switch S1 to "open". On the other CDP18S623 RAM, set rockers 2 and 3 to "open" and 1 to "closed".
3. Install the two CDP18S623's into any unused CDS II memory slots (1 to 5).
4. Add jumper wire on CDS II backplane from slot 10 pin D to pin 3 of any slot 1 through 9 (RNU-P signal).

NOTE: For the installation of any additional RAM modules, refer to the section "Memory Addressing and Expansion" in the **Operator Manual for the RCA COSMAC Development System II CDP18S005**. Any additional RAM installed must start at #4000 (BS4) and may go up to address #7FFF (BS7). Memory in this region must be kept contiguous.

Installation of UART Interface Module CDP18S508

For the installation of the UART Interface Module CDP18S508 some simple modifications are required on the module and on the CDS II backplane. These modifications are described below.

Modifications to CDS II

1. Remove Terminal Interface Module CDP18S507 from slot 14.
2. On backplane add jumper wires as follows:

From Slot 14 Pin No.	To Slot 13 Pin No.	Signal Name
T	M	SEL0-P
M	3	N = 3-P
N	2	N = 2-P

Modifications to UART Module

1. Connect A and C of link LK2 together. See Fig. 3.
2. Set switch S1 to match baud rate of terminal to be used.

3. Insert the UART Module in CDS II I/O slot 14.

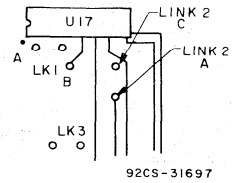


Fig. 3 - Location of A and C of link LK2 on UART Interface Module CDP18S508.

Startup Procedure

After the modifications and additions to the CDS II are made to enable it to utilize the software for the COSMAC Disk Operating System, the following startup procedure should be undertaken.

Connect the EIA or TTY (20 mA) cable between the newly installed UART Module CDP18S508 and the data terminal. Put the terminal in the line mode and check that the baud rate set by the UART Module switch and that of the terminal are matched. CAUTION: The maximum recommended baud rate for 20-mA operation is 1200 baud. Set the terminal for full-duplex operation. Connect the Floppy Disk Dual-Drive Mechanism CDP18S801 to the CDS II in accordance with the instructions given in the **RCA COSMAC Floppy Disk System II CDP18S805 Instruction Manual**, MPM-217.

Power on the CDS II, the data terminal, and the Floppy Disk Dual-Drive Mechanism, in that order. Press the RESET and then the RUNU switches on the CDS II. The asterisk prompt character "*" should appear immediately indicating that the Utility Program UT21 is running. Place the CDOS system diskette in Drive 0 and then type $C. The operating system should load and sign on with a ">" prompt in a few seconds. Follow the procedures given in the **Operation Manual for the RCA COSMAC CDOS Development System (CDS III) CDP18S007**, MPM-232, for using CDOS commands.

Upgrading Pre-CDOS Software

Programs developed for earlier CDS systems which do not use disk I/O routines can be upgraded to run under CDOS by use of a CDOS copy routine provided for this purpose. Versions of the software for the PROM Programmer CDP18S480 and for the Micromonitor Operating System (MOPS) CDP18S831 modified for use under CDOS are available from your local RCA sales or field engineering representative or from RCA Microprocessor Systems Marketing, Somerville, N.J.

User Options

Optional Accessories

COSMAC Micromonitor CDP18S030. The Micromonitor, a powerful self-contained debugging tool, may be used to considerable advantage with the COSMAC Development Systems. It permits in-circuit debugging in real time of both hardware and software. The Micromonitor includes a built-in 28-key keyboard with an 8-digit LED display, 14 status indicator lights, and software debugging routines. It significantly increases the speed with which hardware and software can be integrated and software debugged. It is specifically recommended for the development of programs of more than one kilobyte in length. (Part number: CDP18S030; product description: PD18; instruction manual: MPM-218)

PROM Programmer CDP18S480. This hardware/software package when installed in the CDS enables the user to program Intel 2704, 2708, 2758, 2716, or equivalent PROM's. In addition, it will read, but not program, 1702-type PROM's thereby providing a means of copying these PROM's onto other PROM's. The software is available on disk, paper tape, and magnetic tape in cassette. (Part number: CDP18S480 -disk version, CDP18S480V1 -paper-tape version, CDP18S480V2 - cassette version; product description: PD22; instruction manual: MPM-222)

CDP18S837

Optional Software

Basic 1 Compiler/Interpreter CDP18S834. This high-level language supplied on a diskette is designed to facilitate rapid program development with the COSMAC CDOS Development Systems (CDS III) CDP18S007 V1 and V3. Basic 1 is an easily learned language for the beginning programmer and may be extended indefinitely by the addition of machine language routines. (Part number: CDP18S834; product description: PD34; instruction manual: MPM-234)

Binary Fixed-Point Arithmetic Subroutines CDP18S826. This software package is a set of 16-bit 2's-complement fixed-point arithmetic subroutines including addition, subtraction, multiplication, and division. Also included are binary-to-BCD and BCD-to-binary conversion subroutines plus various utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number: CDP18S826 - disk version, CDP18S826V1 -paper-tape version, CDP18S826V2 - cassette version; product description: PD6; instruction manual: MPM-206)

Binary Floating-Point Arithmetic Subroutines CDP18S827. This software package is a set of 32-bit floating-point arithmetic subroutines including addition, subtraction, multiplication, division, sine, cosine, arctan, natural log, e^x, and square root. Also included are binary-to-BCD and BCD-to-binary conversion plus other utility routines. These subroutines are available on disk, paper tape, or magnetic tape on cassettes. (Part number: CDP18S827 - disk version, CDP18S827V1 -paper-tape version, CDP18S827V2 - cassette version; product description: PD7; instruction manual: MPM-207)

COSMAC Micromonitor Operating System (MOPS) CDP18S831. This software package enhances the capabilities of the Micromonitor by providing inter-facing to disk files. MOPS provides the user with such options as saving the state of the CPU for subsequent reloading and driving the Micromonitor with commands from a disk file to perform automated testing. (Part number: CDP18S831; product description: PD31; instruction manual: MPM-231)

Application Notes

ICAN-6416

An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor

by H. Tweddle

The advent of LSI technology has not as yet brought about the revolution in digital circuit design of which it is, in principle, capable. An LSI circuit, in comparison to its hardwired SSI/MSI equivalent, is more reliable, more compact, and less expensive; however it is less expensive only in high volume, and because of its complexity it tends to be a specialized device with a limited range of applications. As a result of these two factors, LSI has rarely been suitable for standard parts and has found outlets mainly in the custom parts area, which is only economically viable for a large-volume user.

The problem, then, is to produce an LSI circuit which is versatile enough to be made available economically as a standard part. One solution would be to design it with logic elements separately accessible to the user, to be wired in whatever way suited a particular application, but this would result in an impractical pin count. So another approach is taken, that of an LSI circuit whose function is defined by the state of a number of control inputs. This approach has the added advantage that the control inputs need not necessarily be hardwired to a particular function, but may be set by other devices when the system is actually in operation.

Consider, as an example, the CD4057 COS/MOS 4-bit arithmetic logic unit.[1] It has four "function select" inputs on which four bits (the instruction) may be placed to select one of sixteen different arithmetic and logical functions. By supplying it with a series of instructions (which might be described as an elementary program), it can be made to perform more complex functions, such as multiplication and division.

A microprocessor takes this idea several stages further in that, as well as performing arithmetic and logical functions, it can address memory, input, output, and store data, and make program branch decisions. This Note is an introduction to the fundamentals of microprocessors and to the specific capabilities of the RCA COSMAC microprocessor.

AN ELEMENTARY MICROPROCESSOR SYSTEM

Fig. 1 shows a generalized block diagram of a microprocessor together with the three additional functions usually required in a system: program memory, data memory and I/O electronics. It is instructive to divide the microprocessor itself into three main areas: the arithmetic and logic unit (ALU), the registers and the control logic.

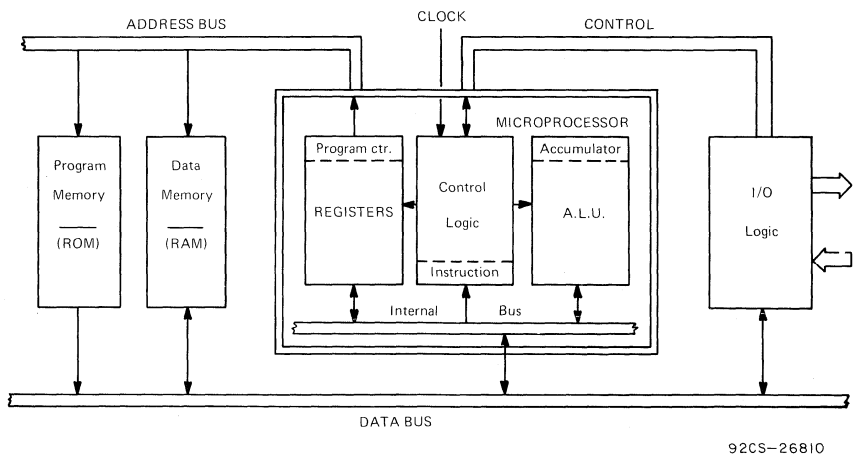


Fig. 1—An elementary microprocessor system.

The Arithmetic and Logic Unit

The ALU, shown in Fig. 2, performs arithmetic and logical functions on words presented to it via the internal data bus. This bus comprises a number of lines (usually 4, 8, 12, or 16) on which data words may be placed. The word length upon which the ALU operates is an important characteristic of a microprocessor: a longer word, by allowing more data to be processed at one time, provides potentially higher speed but results in a more complex, and thus more expensive, machine. The number of different ALU functions available to the user is again a characteristic of a particular microprocessor.

Associated with the ALU is the accumulator, which is a register for temporary storage of operands and results of ALU operations. Some microprocessor architectures employ several accumulators; in the simplest case, however, one operand is loaded into the accumulator and the other is presented on the data bus, while the result appears in the accumulator, overwriting the first operand. An overflow of the accumulator sets a flip-flop called a flag. There may be a number of other flags, both to indicate overflow or underflow of registers and to show certain internal- and external-state information.

Registers

A microprocessor stores memory addresses and data in a number of registers, as shown in Table I. One register holds the current program counter, which addresses a location in program memory. A group of registers is usually provided for temporary data storage; these registers are referred to as scratchpad memory. In most applications, some additional read/write data memory is required; this memory is addressed by a register containing the data pointer.

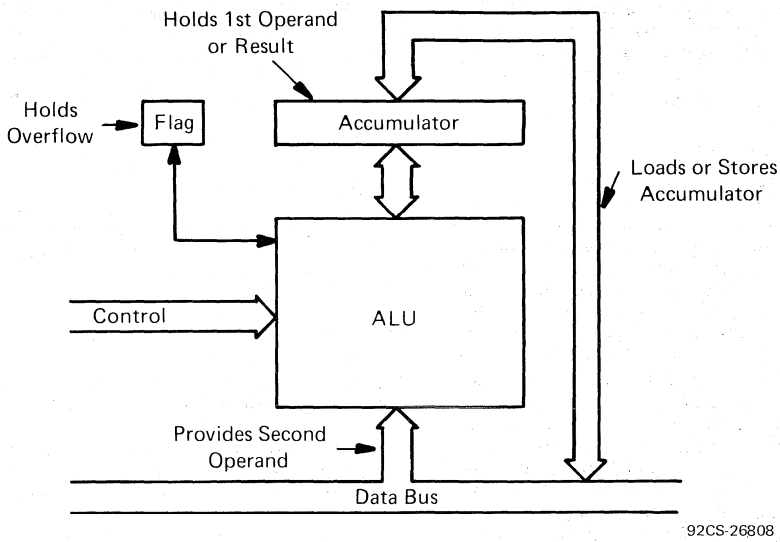


Fig. 2—The arithmetic and logic unit, the ALU.

Table I – Typical Microprocessor Register Usage

PROGRAM COUNTER	Addresses current instruction in program memory
DATA POINTER	Addresses current location of interest in data memory
STACK POINTER	Addresses next vacant location in external stack
DMA POINTER	Addresses location in data memory for DMA transfer
(INTERNAL) STACK	LIFO data/address storage
SCRATCHPAD	Random access data/address storage

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A register block may also be set aside as a "stack", which provides last-in first-out storage of return addresses and data. A stack is needed when the program includes subroutines. A limited stack size, however, limits the subroutine nesting capability of a microprocessor. A more versatile approach is to form a stack in external memory, in locations addressed by the stack pointer.

The word length of the address registers is important as it defines the number of memory locations that may be directly addressed. The word length of the data registers is usually defined by the word length of the machine.

The Control Logic

The control logic is responsible for defining the operation of the ALU, data movements within the microprocessor and data transfer to and from external devices. It also provides control signals to help external logic to interface with the microprocessor, and can be instructed to change the program counter, and thus the microprocessor operation sequence, in response to the state of control inputs, flags or internal registers. The control logic derives its timing from one or more clock inputs; its function is defined by the instruction, a word presented to it from program memory and stored in the instruction register.

Program Execution

The sequence of operations that the microprocessor is required to perform is stored as a string of instructions, called a program, in the program memory. The first of these instructions is addressed by the program counter and fetched into the instruction register. The control logic then acts upon this instruction to execute the operation it specifies. The program counter is then incremented, the next instruction is fetched, and another fetch-and-execute sequence is carried out. In this way, the microprocessor steps through the instructions to perform the task defined in the program.

Certain instructions, usually called branch instructions, change the program counter to a location other than the immediately subsequent one, allowing program jumps and the use of subroutines. Subroutines are frequently used groups of instructions, which may be stored away from the main program stream and called into use whenever needed by the main program. They help conserve memory space, since a subroutine which may be used several times in the course of a program need be stored only once.

Conditional branch instructions test the state of a particular register or flag and implement the branch if the required condition is met. If the condition is not met, the microprocessor continues with the next instruction in the main program. In this way, the microprocessor may be made to respond differently to different external or internal conditions.

Memory Requirements

Several different types of semiconductor memories are commonly used with microprocessors, as shown in Table II. Data memory is written into in the course of a program; therefore, it is implemented in a random access memory (RAM), a read/write memory that is volatile (i.e., it loses its data when the power supply is removed). Program memory, on the other hand, must usually be non-volatile and is not altered during normal microprocessor operation, so that program storage, in a production system, is normally a read-only memory (ROM). However, if the application allows or requires reloading of the program, the program may be stored in a RAM. This memory may also be used during initial development of a system, where frequent program changes are required. Another possible form of program storage is the programmable ROM (PROM), which may be used in prototype systems or in small-quantity production systems where a mask-programmed ROM is not economical. It may be found convenient in a prototype system to use an erasable PROM (EPROM) for program storage since, although non-volatile, an EPROM may be reprogrammed as the system is modified.

Input/Output

The input/output[2], or I/O, portion of the microprocessor provides information as words on the data bus with additional controls available separately. The I/O electronics is responsible for interfacing these signals with whatever input/output devices the system uses. Broadly, the functions of the I/O electronics include synchronization of data transfer, selection and activation of one of a number of I/O devices, and the formatting of data so that it is compatible with the device selected. The functions available on the control lines have a marked effect on the complexity of the I/O electronics. The I/O electronics may also be required to do logic-level conversion as part of the interfacing function if this facility is not provided within the microprocessor itself.

Table II – Types of Memory Commonly Used with Microprocessors

RAM	Random Access Memory	Volatile	Data storage, and program storage in some applications
ROM	Read Only Memory	Non-Volatile	Program storage in production systems
PROM	Programmable ROM	"	Program storage in small quantity production and prototypes
EPROM	Erasable PROM	"	"

An I/O data transfer may be initiated either by the microprocessor in the course of its program execution (programmed mode I/O), or by one of the I/O devices. In the latter case, the I/O device requests an interrupt by raising the interrupt input of the microprocessor. The current program execution is then halted, data and addresses required for eventual resumption of the program are stored in the stack as for a normal subroutine, and the microprocessor starts performing the interrupt service routine defined by the user. The interrupt service routine first establishes which I/O device has requested the interrupt and then performs the appropriate instructions to deal with the request.

The input or output of data may also be performed directly between the I/O device and data memory; this mode is called direct memory access (DMA). DMA may be externally or internally controlled. In the first case, raising the DMA request pin causes the microprocessor, after completing its current instruction, to detach itself from the data and address buses. The I/O device is then permitted to communicate with data memory at a speed limited only by the access time of the memory, rather than by the cycle time of the microprocessor. This form of DMA can be made very fast by using fast memory, but in this form the I/O electronics is required to provide address and control as well as data inputs to the memory, thereby increasing interface complexity. In the second form of DMA, the microprocessor itself provides address and control signals in response to a DMA request; the I/O electronics need only present the data to the I/O bus. This second form is the more convenient form of DMA, and is considerably faster than a standard programmed or interrupt mode I/O. However, the speed of data transfer is a function of the cycle time of the microprocessor, and therefore no advantage is gained from using a very fast memory.

SOFTWARE

The preceding text has established broadly what a microprocessor is and what it can do. Its associated software[3] (its instructions and their manipulation) and software support (the computer assistance which may be called upon to assist in software handling) must now be considered.

Hexadecimal Code

An instruction word as understood by the microprocessor is, of course, composed of a number of binary digits or bits, which can only take one of the two values 0 or 1. However, it would be very laborious for the user to write his programs in this form, so a shorthand notation is used.

Decimal, or base 10, notation is not a convenient form of shorthand for binary numbers since 10 is not an integral power of 2 and hence conversion from decimal to binary notation is awkward. A more practical shorthand is hexadecimal, or base 16, notation, which uses the 16 symbols 0 to 9 and A to F to represent the binary numbers 0000 to 1111. An eight-bit instruction is therefore represented by two hexadecimal or hex digits, which is considerably more convenient. Conversion from binary to hex notation is straightforward and involves direct translation of each block of four bits into a hex digit, as shown in Table III. The only points to remember are that the division into blocks must start from the "least significant" end of the binary number, and that leading zeros must be added to fill up the "most significant" block if necessary. Conversion from hex to binary is simply a reversal of this process. For example, hex 2A represents binary 101010.

Table III – Binary/Octal/Decimal/Hex Conversion Table

Binary	Octal	Decimal	Hex
0000	0	0	0
0001	1	1	1
0010	2	2	2
0011	3	3	3
0100	4	4	4
0101	5	5	5
0110	6	6	6
0111	7	7	7
1000	10	8	8
1001	11	9	9
1010	12	10	A
1011	13	11	B
1100	14	12	C
1101	15	13	D
1110	16	14	E
1111	17	15	F

Assembly Language

Although hex notation is convenient for converting instructions to binary code for the microprocessor, it is not very easy for the user to read. For this reason an assembly language is used in which instructions are represented by mnemonic names which bear some relation to the instruction in plain English and which can, therefore, be read easily. In addition, it is convenient to label branch destinations with mnemonic names as an alternative to keeping track of the actual addresses of such destinations in program memory (which may change as the program is modified and instructions are inserted or deleted). It should be noted that assembly-language instructions bear a one-to-one correspondence to machine-code instructions, so the designer still has close control of his instruction usage, and is, therefore, in a position to optimize his program for minimum program storage space and execution time. Conversion to machine code, or assembly, may be done on a computer using a program called an assembler. The assembler is

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usually accessible through computer time-share companies as one of a microprocessor manufacturer's software support programs.

On assembly, certain diagnostic messages will be output indicating "grammatical" errors in the program. For instance, a branch to a non-existent label will be objected to by the assembler. Any changes to the program may be made by using another program resident in the computer, the editor.

Higher-Level Languages

It is sometimes convenient to write programs in a higher-level language (e.g., PL/M), in which case a support program called a compiler is required to convert the high-level instructions to machine code. One high-level instruction gives rise to a number of machine-code instructions on compilation: this feature distinguishes it from an assembly language instruction. The many-for-one transformation means that the programmer is no longer in direct control of his machine code and cannot easily optimize his program for minimum storage space and execution time. However, higher-level languages are useful since they represent a quick and convenient way of writing microprocessor programs. A well-written compiler will minimize the inefficiency of the many-for-one transformation.

Simulation

Once a grammatically correct program has been written, it is necessary to ascertain whether it performs the desired function. For this purpose, a simulated version of the microprocessor may be set up within the host computer by calling the simulator program. The simulated machine is put through its paces by applying inputs and observing outputs on the keyboard of the host computer.

Debugging

If the program run on the simulated machine has bugs (i.e., errors) it is necessary to trace the exact nature of these bugs in order to make the appropriate modifications to the program. A program called the debugger facilitates this process by allowing the designer to observe or alter registers, memory locations, and flags in the simulated machine. After removal of a bug by use of the editor, the simulator is called back and the simulate/debug/edit sequence continues until program operation is satisfactory.

Fig. 3 compares the method of programming by hand with that of using software support programs.

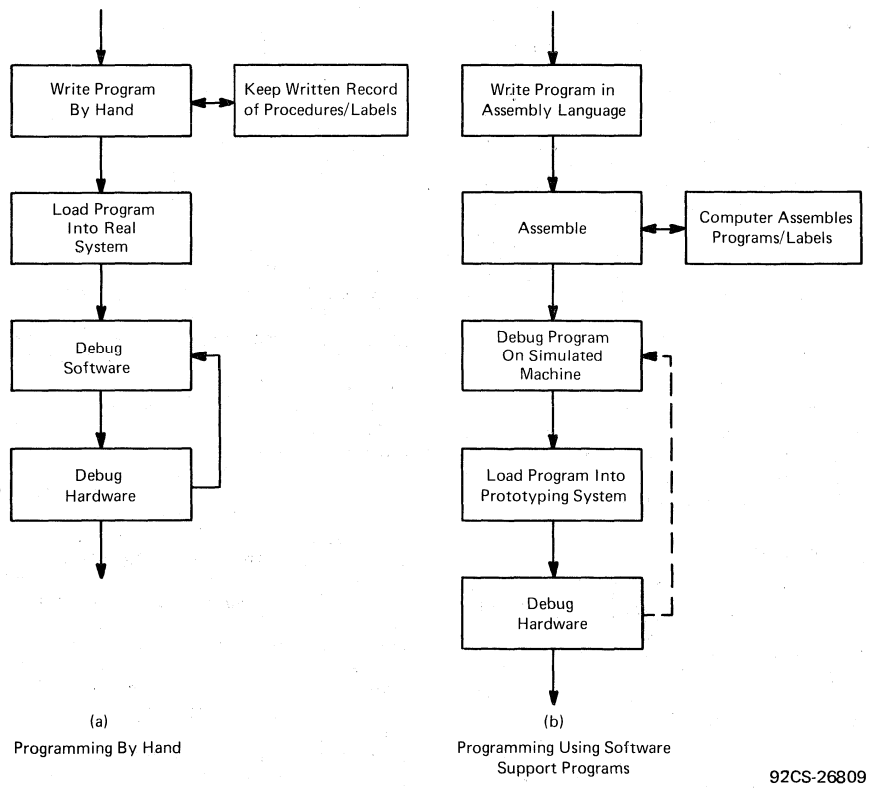

Fig. 3—Two ways of writing a program.

HARDWARE

The program produced as previously described must now be put through its paces in a real system, and for two main reasons it may still contain bugs. First, the simulated machine does not, of course, operate in real time, so that certain timing problems may not be apparent at the simulation stage. Second, the simulation does not include the I/O devices and their associated electronics, and therefore these too must be checked out in actual hardware.

Part of the applications backup provided for microprocessors is the hardware support kit. This kit contains the bare essentials of a microprocessor system including the microprocessor itself, some memory, and some interface and control electronics. It is intended as an aid to prototyping microprocessor designs. The designer builds his prototype system using this kit as a basis, and can therefore prove its operation before embarking upon his production design. The kit may then be reused to prototype the next system.

To further aid interfacing and memory expansion, standard cards implementing commonly used functions may be made available for use in the prototyping systems; support chips provide similar support for production systems.

COSMAC

The first commercially available RCA microprocessor, COSMAC, is, at the time of writing, a two-chip machine consisting of the CDP1801U microprocessor control IC and the CDP1801R microprocessor register IC. The COSMAC microprocessor is described in detail elsewhere[4,5,6], but it is instructive to draw attention to some of its main features here.

Technology

The COSMAC microprocessor makes use of COS/MOS devices, with their well-known advantages of low power consumption, high noise immunity and wide power supply tolerance. Only one clock input is required, and all registers employ static memory cells, so that there is no minimum clock frequency. Therefore, the user can choose slow-speed operation for ultra-low power consumption or implementation of inexpensive slow memory. The clock may, in fact, be stopped at any time without any loss of information, which is a useful feature for synchronization with other system components.

The COSMAC microprocessor operates over the full military temperature range (−55 to 125°C) and can be run from a single power supply anywhere in the range of 4 to 12 volts. It can also supply the output buffers independently of the main supply voltage if required, making external logic level conversion unnecessary.

Architecture

The COSMAC microprocessor is an eight-bit machine: its I/O bus has eight lines and the ALU acts upon eight-bit words. The architecture[7], shown in Fig. 4, is based on a 16-word by 16-bit register matrix that can be used to store multiple program counters, data pointers, etc. This register matrix can also be used as scratch-pad memory because the high- and low-order eight bits of each register may be accessed separately by means of the data bus. This register-based architecture is extremely flexible; the designer is allowed free choice of the way in which he uses the registers to suit his particular application. The 16-bit program counters and data pointers allow direct addressing of up to 64K bytes of memory.

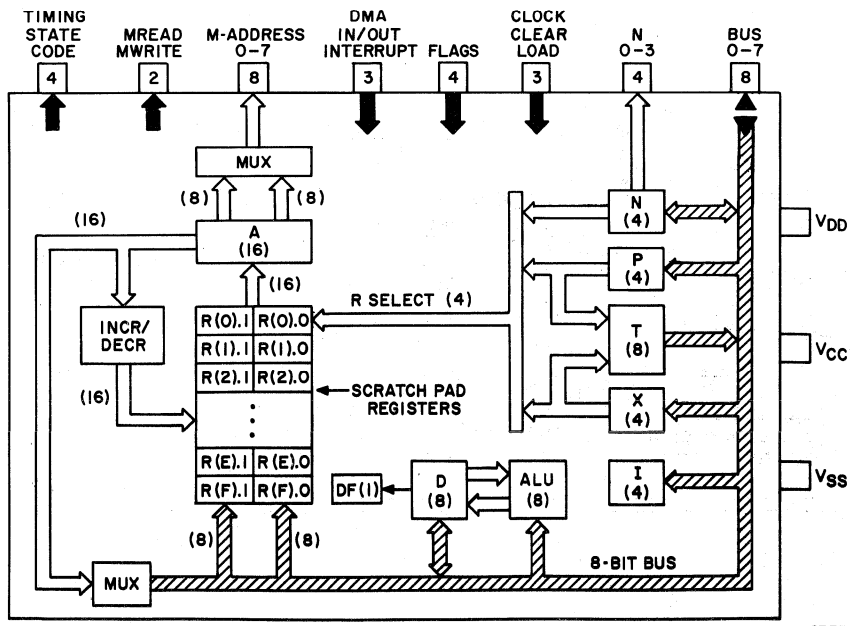

Fig. 4—Architecture of the COSMAC microprocessor. 92CS-26557

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Instruction Set

The instruction set is a simple but powerful one and, again, flexible. It contains ALU, branch, register transfer, memory transfer, interrupt handling, and I/O instructions. Each instruction is eight bits long and has the same instruction cycle time (i.e., two machine cycles, or 16 clock periods). This uniformity of format and speed is significant in making the COSMAC microprocessor easy to use, especially in real-time applications. The total number of instructions recognized by the microprocessor is 208, but this total subdivides into 59 easily understood generic instructions.

Input/Output Structure

The cost of the microprocessor itself is, of course, only a small part of the total system cost; memory, input, output, power supply, system control, and programming costs are all major considerations. The advantages of the COSMAC microprocessor in some of these areas have already been described. The I/O structure especially has been evolved with a view to minimizing system cost and complexity, as shown in Fig. 5.

In addition to the eight-bit bidirectional data bus, there are four external flags (i.e., inputs which may be tested by branch instructions) and a four-bit I/O command bus which is set by the programmer as part of each I/O instruction. Two timing-pulse outputs further aid interface design.

There is an interrupt request line and two lines to request DMA input and output. The COSMAC microprocessor provides its own addressing for DMA transfers ("on-chip DMA"), again reducing I/O interface complexity. The built-in program load facility takes advantage of this on-chip DMA capability, allowing loading of a program starting at memory location number 1 by simply setting the "load" input; no external addressing is required to load a program.

Software Development Package

Although the register-based architecture makes machine-code programming particularly easy, software support programs[8] are available on timeshare or on tape for running on an in-house computer to speed up program development. These programs include an assembler, a simulator, and a debugger, as shown in Fig. 6. At the time of writing, a compiler is in preparation.

A batch assembler for use on an IBM 360/370 is also available. A "stand-alone" editor/assembler will fulfill the needs of those users who do not wish to depend upon either in-house or timeshare computing.

COSMAC Microkit

The COSMAC microkit[9] is a prototyping system for the development of systems based on the COSMAC microprocessor. A teletype or similar terminal can be attached to the microkit to form an elementary but complete microcomputer system. Physically, the microkit comprises a 19-inch rack-mountable card nest with power supply and basic controls with a COSMAC CPU, control and interface circuitry, 512 bytes of PROM containing utility programs, and 1,000 bytes of RAM into which the user can load his own programs. Spare positions are provided into which the user can plug cards carrying extra memory, I/O electronics, or whatever circuitry is required to build his prototype system. Another function of the microkit will be as a vehicle for the "stand-alone" software support described above.

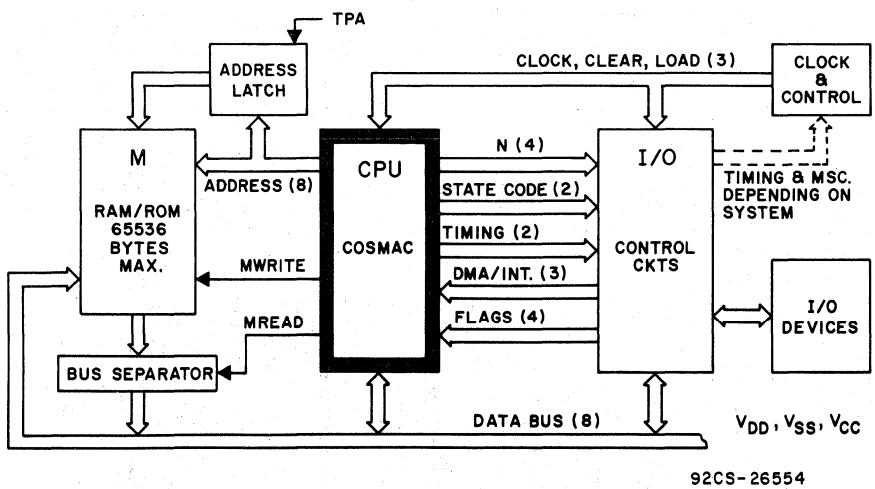

Fig. 5—System block diagram of the COSMAC microprocessor.

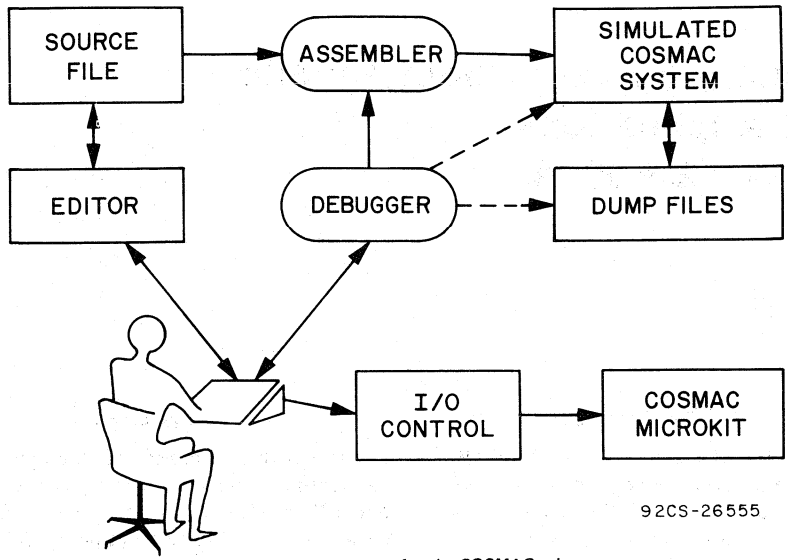

Fig. 6—Software support system for the COSMAC microprocessor.

APPLICATIONS

The range of applications of the microprocessor is extremely wide and includes most data-handling and control applications, where it provides an attractive alternative not only to hardwired logic, but also to custom LSI and in some cases minicomputers. Such applications include instrumentation, computer peripherals, automobile electronics, process and traffic control, home entertainment[10], and educational and business systems.

The COSMAC microprocessor finds applications in areas where microprocessors using other technologies may not be suitable. For example, its low power consumption and wide power-supply tolerance reduce power-supply costs and allow its use in battery-operated systems or systems with standby battery supplies. The wide operating-temperature range opens up applications in the military field and in automotive and harsh industrial environments, where high noise immunity is an added advantage. In addition, since the COSMAC microprocessor has been specifically designed to reduce system cost and complexity, it promises to be economically viable in a very wide spectrum of applications.

CONCLUSION

This Note has discussed some of the characteristics of microprocessors with the intention of providing a basic introduction and definition of terms; a more detailed treatment of the subject may be found in references 11 through 14. A very brief description of the COSMAC microprocessor has been provided. It is suggested that this machine, because of its unusually simple and symmetrical architecture, provides an ideal introduction to microprocessors as well as, for both economic and technical reasons, representing new and interesting aspects of microprocessor technology.

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Memory-System Characteristics and Applications of the CD4061A

by

J. Paradise

INTRODUCTION

The CD4061A 256-word by 1-bit RAM, by virtue of its low power, simplicity of use, and its standard COS/MOS features, is a versatile building block in medium-scale memory systems. This Note describes circuit and system applications concepts of the CD4061A, and includes details on practical memory-system design, timing, performance, and testing.

CIRCUIT CONCEPTS

The CD4061A consists of three major components: the 256-bit memory array, the X and Y decoders used to access a particular bit in the array, and an input/output interface between the external package pins and the memory array. The memory array consists of 256 six-transistor static memory cells organized into 16 columns and 16 rows, Fig. 1. The static memory cell is designed to

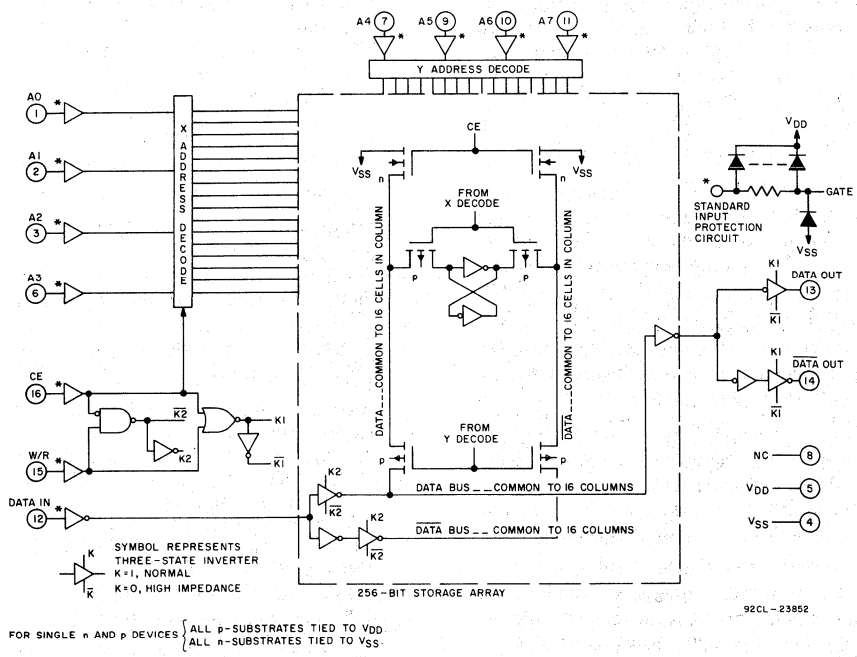

Fig. 1 – CD4061A logic diagram.

provide efficient and reliable read and write operation; the requirements for small area, low power, insensitivity to process variations, speed, and reliability over the full, expected voltage and temperature ranges were considered in the design.

The write operation takes advantage of a push-pull driving configuration; data is written into one side of the flip-flop and $\overline{\text{data}}$ into the other side. This arrangement provides the advantages of high speed and successful writing without restricting voltage range or incurring unusually tight layout or processing problems. For the read operation, current is sourced from a flip-flop p-unit and a p-transmission gate from the data side to provide a stored 1. The ratios of the p transistors to the n transistors in the cell are selected to provide adequate drive capability for speed, dc stability, and nondestructive read and write operations.

The memory is addressed by means of two 4-to-16 address decoders per column (Y decoder) and row (X decoder). The X decoder turns on the p transmission gates of a selected row of memory cells, and the y decoder turns on the p transmission gates in series with the data and $\overline{\text{data}}$ lines of a selected column, connecting that column to the common data and $\overline{\text{data}}$ bus.

The input/output circuitry enables data to be transmitted into and out of the memory array through the external package pins. Data input is connected to the data and $\overline{\text{data}}$ bus through the interface circuitry shown in Fig. 1 only when writing is being performed with the chip enabled. A sense amplifier used for reading is permanently connected to the data line bus, but the output circuitry is turned on only when reading is being accomplished with the chip enabled. For any other condition, the output is at a high-impedance level with n and p output transistors turned off.

The read sense amplifier senses source current from a memory cell with a stored 1 and converts it to a logic 1 voltage level. If the memory cell contains a stored 0, the sense amplifier retains a logic 0 output-voltage level because the data line is initialized to a 0 level before the chip is enabled. This 0 level appears on the output as soon as the output circuitry is turned on (typically 50 nanoseconds after the chip is enabled at 10 volts) independent of the previous level of the high-impedance line. The level will change only if a 1 is sensed from the memory, and then before the maximum access time specified for the device.

Because of the internal structure of the circuit it is necessary to raise and lower the chip enable voltage level for each read or write cycle, which maintains the chip enable voltage at a high level during an address transition. The explanation for this is as follows: Residual charge is present on the data and $\overline{\text{data}}$ lines after a read or write operation. When new information is being read, this charge may destroy a stored 0 already present in the newly selected cell. In addition, the address decoder, while settling, may instantaneously select an undesired cell, which may have its information destroyed by this charge. To prevent this, n-channel clamping transistors, turned on when the chip-enable level is high, are provided on each data and $\overline{\text{data}}$ line to discharge these lines. The X decoder is also disabled when chip enable is high to allow time for the decoder to settle before accessing and to prevent "half-select" current from flowing from a selected row cell in the array containing a 1 through the clamp to ground. Thus, there is a minimum setup time to allow for data lines to discharge and a minimum hold time to allow the address decoders to settle.

SYSTEM CONCEPTS

The CD4061A package can be used as a building block in the construction of medium-scale memory systems. For bit expansion, the address lines, the write/read control, and the chip enable line of each package can be tied together; separate data in and data out lines are maintained. For word expansion, the chip enable function can be utilized by accessing blocks of 256 words with external decoding. As an expansion feature, all outputs are disabled except when reading is being performed with the chip enable function at a low level. Thus, outputs can be tied to a common bus, and data in and data out lines can be tied together in a common data-line system (with data-in drivers disabled when necessary).

Consider the performance characteristics of an expanded memory system. Loading is increased when multipackage wiring is used; thus the fan-out of the buffers driving the address and control lines must be considered as must the equivalent output capacitance of the common data-out buses (with approximately 10 picofarads of output capacitance for each package with the output in the high-impedance state). The read access time of a single memory package increases as a function of this bus and wiring capacitance,

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Fig. 2. Note that the access time of a memory system is the worst-case access time of the slowest package in the system.

In considering the power dissipation of such a system, standby power is approximately equal to the typical value specified on the data sheet multiplied by the total package count, since typical data reflects a distribution mean of units. Standby power can be reduced considerably if a standby battery system is used, as illustrated in

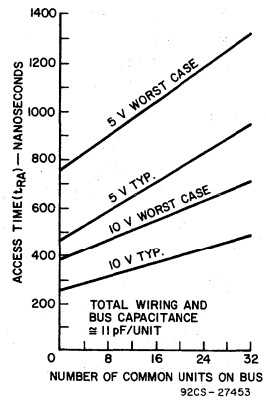


Fig. 2 – Typical and expected worst-case access time of single CD4061 as a function of number of common CD4061 outputs per bus.

Fig. 3. Any battery voltage above 3 volts can be used to power the memory while it is in an inactive state. The battery also serves as a back-up during power interruptions, and eliminates concern about the volatility of the system. Note that the forward diode drop of the diode in series with the battery and the voltage levels at both inputs and outputs with external power removed must be considered.

The dynamic dissipation of the system is additive, but only for those memory devices being utilized at any instant. Dynamic dissipation can be decreased by lowering operating voltage, but there are performance tradeoffs. Operation at 5 volts yields low power and the possibility of direct TTL interfacing to inputs and outputs. Operation at a higher voltage increases power dissipation and interface complexity but provides the advantage of higher speed. The choice is a function of the requirements of the system being designed.

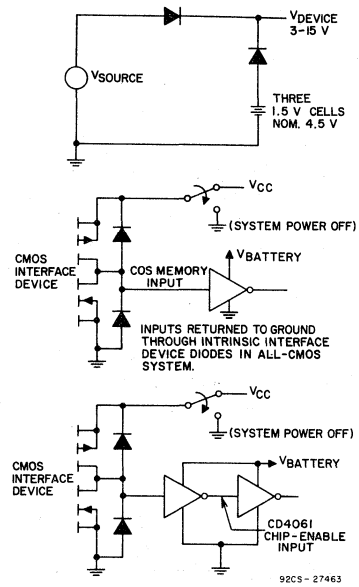


Fig. 3 – Battery back-up system: (a) power-supply configuration, (b) configuration for CD4061 inputs when system power is shut off, (c) recommended addition of inverter for chip-enable input to keep chip disabled when system power is off.

PRACTICAL MEMORY SYSTEM

Fig. 4 illustrates the use of the CD4061A in a memory system. The system shown consists of 32 memory packages organized as 1024 words by 8 bits plus address, write/read, and input and output data latches. Such a system can be modified to suit system memory capacity requirements by adding or deleting memory or latch chips. Three methods of control timing are explained; others may be used if the timing requirements of the memory chip are not violated. These methods provide ways of generating the basic system clocks needed; namely, the data-in latch clock, data-out latch clock, address latch clock, write/read latch clock, and chip-enable clock. An additional clock refinement can be generated to force the data-out latches to a high-impedance condition for any desired portion of the memory cycle. The clocks must be generated such that all address transitions at the chip take place before the chip experiences a low chip-enable signal.

Control-Timing Methods

Method 1 - Single Clock - The single-clock method, Fig. 5, utilizes a single clock signal

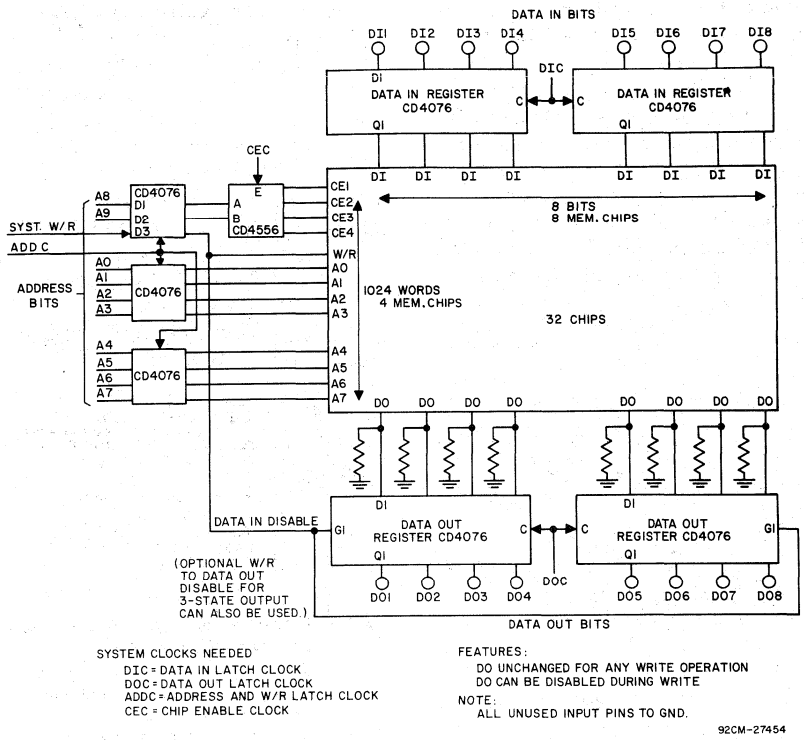


Fig. 4 – Basic 8K memory system.

to generate all of the timing for the system. This method assumes that all address, write/read, and data-in signals to the system are stable by the time that the clock signal has a positive-going edge. At this time, these signals are latched into the appropriate CD4076 latches for cycle N. On the negative

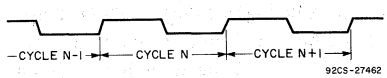


Fig. 5 – Single-clock method timing diagram.

transition, the chip is enabled (the CD4556 decoder allows the selected chip-enable input to go low). This transition cannot take place until the latches settle and the minimum chip-enable width is observed.

For a read cycle at the next positive transition, where the time between negative and positive transitions must be greater than the minimum chip-enable width, the valid output data is latched into the data-out latches; for a write cycle, valid data is written into the memory during the chip-enable low interval; output data latches hold their previous states. At the same transition, information for cycle N+1 is latched into the memory. Thus, in this method, new address and data signals must be generated before the previous data appears at the output. However, for systems in which this generation of signals is not a problem, this method is simple and fast.

Method 2 - Multiclock - The multiclock method enables a decision to be made on output data before new address and data information is presented to the memory. In this method, input signals are latched after data out is present, as shown in the timing diagram in Fig. 6. Note that the master clock frequency is four times greater than

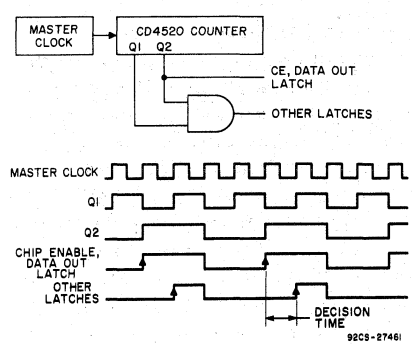


Fig. 6 – Multiclock-method logic and timing diagram.

the system frequency, as necessitated by the decoding scheme used. The decision time is half the chip-enable width. If the decision time must be longer, an alternative scheme may be used, as shown in Fig. 7. The decision time is twice the chip enable width with the scheme of Fig. 7.

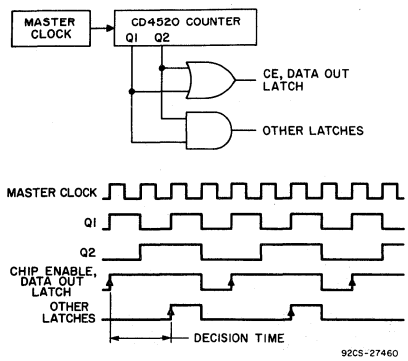


Fig. 7 – Multiclock-method logic and timing diagrams when decision time must be longer than with the circuit of Fig. 6.

Method 3 - Read/Modify/Write Cycle - The previous methods showed examples of either read- or write-cycle system approaches. Method 3 increases system speed by allowing a read and write cycle for the same address to be combined, Fig. 8.

The chip-enable signal is generated as before. The address latch is designed to occur while the chip-enable level is high, as in the previous examples. The major difference is that the write/read function switches while the chip-enable level is low to allow both a read and a write operation; data-out latches just before the write operation. If a write only or a read only cycle is desired, the appropriate read/modify/write and write/read signals must be generated, as shown in the truth table.

If the valid data-out must be latched before new information is written, the alternative scheme shown in Fig. 9 may be used. Note that many other arrangements for system timing are possible, but as decoding complexity is increased, the speed limitations of such decoding arrangements may offset any speed gained by generating a multitude of signals.

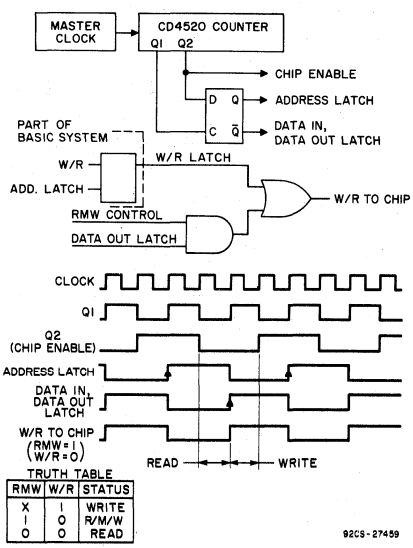


Fig. 8 – Read/Modify/Write logic and timing diagrams.

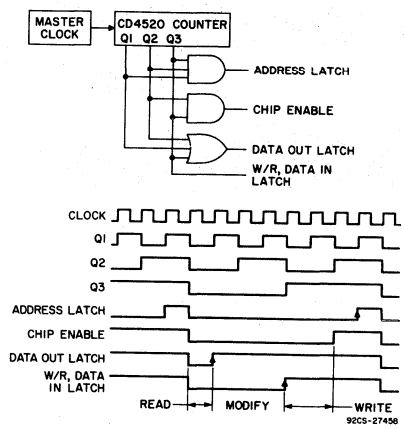


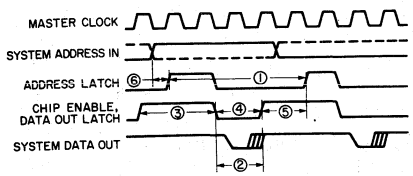
Fig. 9 – Read/Modify/Write logic and timing diagrams when valid data-out must be latched before new information is written.

MEMORY SYSTEM PERFORMANCE

The memory system described in connection with Fig. 6 was built and dynamically exercised on a CMOS memory exerciser (described below) to judge system performance. Typical units chosen at random were used for the memory chips and the peripheral circuitry. The timing diagram and numbers presented in Fig. 10 describe the minimun time allowable for reliable memory performance using a "walking 1 and 0" test pattern.

CMOS PATTERN GENERATOR

A practical system, a programmable CMOS pattern generator that utilizes the method of memory system timing control of Fig. 6, is



PARAMETER	MEASURED DELAY (MINIMUM) 5V	10V	15V
① CYCLE TIME	2000	800	600
② ACCESS TIME	600	300	240
③ CHIP ENABLE OFF TIME	1000	370	280
④ CHIP ENABLE ON TIME	1000	430	320
⑤ DATA OUT LATCH TO NEW ADDRESS LATCH TIME	600	400	300
⑥ SYSTEM ADDRESS SETUP TIME	600	200	150

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Fig. 10 – Memory system performance.

described in Fig. 11. The pattern generator can be expanded to N independent channels of 256 bits each; each channel uses one CD4061A memory chip with peripheral circuitry common to all channels.

that is selected by means of an external switch will have data written into it when the write/read control is high. When the write/read control is low, data is read from all chips. The data is latched on the leading edge of the chip-enable signal and output from the system.

The system is versatile because it is CMOS compatible and uses the same power supply as the device under test. The circuitry can be refined to increase this versatility. As an example, the eight-channel pulse generator pictured in Fig. 12 was built for 8 independent channels with one channel programmed to stop or reset the system at a desired time slot. (Time slots shorter than 1 microsecond are readily achieved with V_{DD} = 10 V). The pattern generator can be expanded into a laboratory bench tester if expected output waveforms are programmed on the necessary channels and compared with the waveforms of the device under test

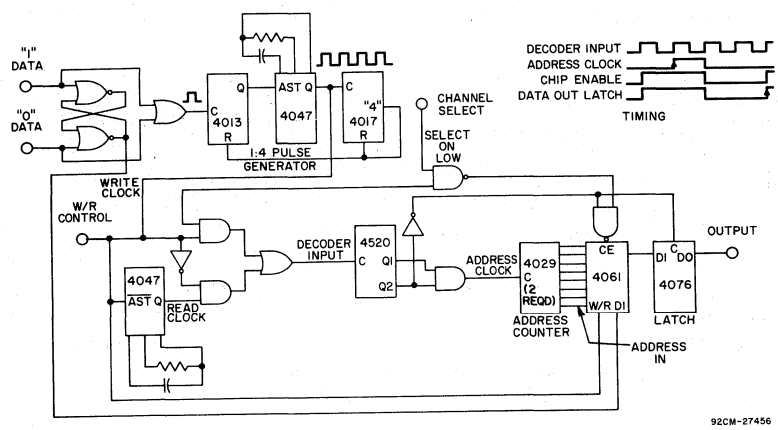

Fig. 11 – Basic CMOS pattern-generator schematic diagram.

Data is input to the system by means of separate pushbuttons designated for 1 or 0 data. The data is latched and input to the memory chips. The data pulse is detected and converted to a four-pulse burst. The external write/read control selects this burst for writing into the memory or selects a free-running oscillator for reading. Decoding circuitry converts each series of four pulses into an address-clock and chip enable signal; the address-clock edge is generated while chip enable is high. An address counter advances on each address-clock edge and is input to the memory address lines. The chip

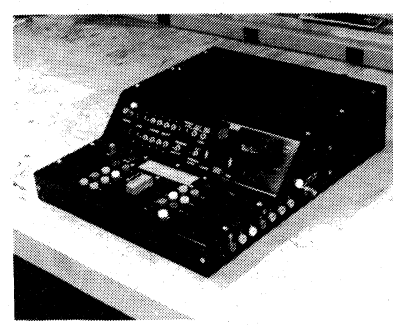

Fig. 12 – Eight-channel pulse generator.

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by means of exclusive-OR gates. The gate outputs can stop the tester, indicating which time slots failed. Note the speed limitations of such a system as a result of the delays added by extra circuitry and the propagation delay of the tested device.

MEMORY TESTING CONSIDERATIONS

Semiconductor memories can be tested to a wide variety of test patterns to guarantee their functionality. These methods range from a simple 4N test (where N is the number of words) where the memory is written into with all 1 data or all 0 data and then sequentially read back, to a 2^N test, which covers every possible data storage pattern. The simple test does not detect address or data interaction; the complex test is impractical–$1.157920892 \times 10^{77}$ tests are needed to exercise the CD4061 memory of 256 words.

Compromise patterns are used to factory test the CD4061. One is a "marching 1 and 0" pattern (MARCH), a 10N test used for initial functional testing; the other is a "galloping 1 and 0" pattern (GALPAT), an $8N^2$ test used to exercise the memory to the limits specified on the data sheet.

In MARCH, a background field of 0 data is written into the memory. At address 0, the 0 is read and a 1 is written. The address is sequentially advanced until 0 data has been read from and 1 data has been written into each cell. The address is then decremented, with 1 data read and 0 data written. The entire procedure is then repeated, this time with a background 1 data field. This pattern effectively checks for adjacent data disturb, and has been found to be a reliable test for the CD4061.

In GALPAT, the same background field of 0 data is written into the memory. A 1 is written into test-word address 0. Then address 1 is read, address 0, address 2, address 0, etc., until all addresses are read. A 0 is written into address 0, and the test-word is moved to address 1. The sequence is repeated until the test-word has been moved to all locations. The procedure outlined is then repeated for a background of 1 data. GALPAT, which represents one of the most complex of all practical data patterns, is used on the CD4061, although excellent correlation has been achieved between GALPAT and the simpler MARCH pattern. GALPAT does have the advantage of testing all possible address and data transitions, instead of adjacent data only.

For the memory user, the most efficient test is one that exercises the memory with the same data-pattern possibilities that will be input in actual use. As an alternative, this Note describes a "black box" tester, a WALKPAT memory exerciser, that can be used. The tester uses a "walking 1 and 0" pattern ($2N^2$ tests), a pattern similar to that used by GALPAT with the exception that address locations are sequentially read during the read operation instead of addressing the test word between each incremental address change. This pattern is fairly easy to generate with available CMOS circuitry and remains simple enough so that the memory can be exercised to the minimum cycle time limits specified in the data sheet. The WALKPAT exerciser is described in detail below.

WALKPAT MEMORY EXERCISER

The details of the exerciser are shown in the block diagram of Fig. 13 and the logic diagram of Fig. 14. The exerciser is divided into three basic parts, as shown in the block diagram.

With the operation of the start switch, the system is automatically reset to initial conditions by means of a short, master reset pulse. The external clock is gated on, and signals for advancing the address, chip enable, and data strobe are generated. When either an error or end-of-test signal is generated, the clock is gated off, enabling the user to detect the failing bit if there is an error.

The counter select logic initially allows 0 data to be written into each cell in the memory under test. A test-word of 1 is selected for the starting address and is written into that location. The sequential address counter then cycles through all bits in the memory, and memory data is read from the device under test. After all bits are read, the test-word is moved to the next bit. The test-word address counter stores the test-word while the sequential address counter cycles through all bits. After each complete cycle, the test-word is incremented, until it has been moved through all bits. The procedure is then repeated, with a test-word of 0 "walked" through a field of 1 data.

The address-comparator circuitry compares the contents of the sequential address register with the test-word address register. A 1 output is generated only when both registers contain the same address. This signal is compared with the memory under

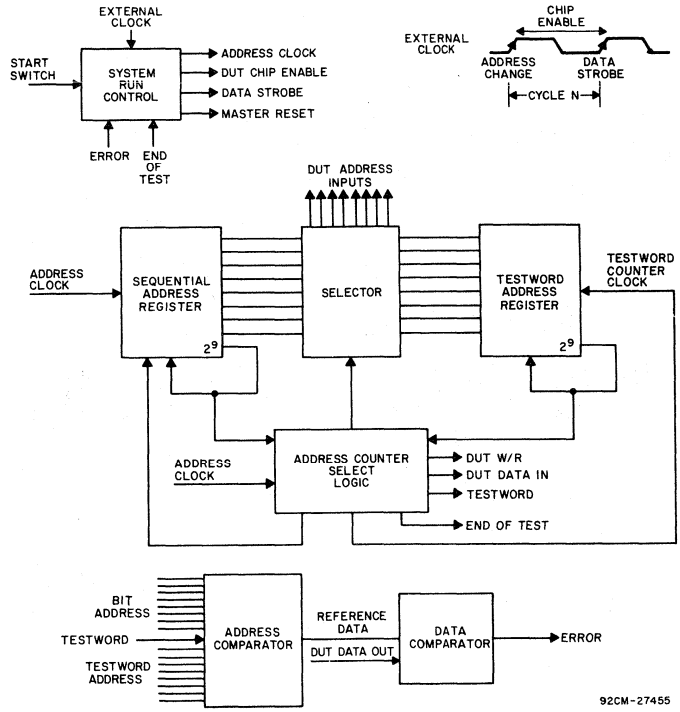

Fig. 13 – WALKPAT Memory Exerciser block diagram.

test, which should output 1 data only at the test-word location (the opposite occurs for a test-word 0). An error signal is generated whenever the two data patterns do not match. Since the counter is stopped at the failing address, this information becomes readily available to the user.

Circuit refinements are shown in the logic diagram of Fig. 14. An error override switch is included to allow the tester to complete its cycle. Continuous or one-shot operation can also be selected. A green light can be connected to the end-of-test output and a red light to the error output to signal whether the tested device is good or bad.

Maximum speed is obtained by adjusting the external clock to give the appropriate chip-enable on and off times as specified in the data sheet and by delaying chip enable from the address clock to allow enough time for the address outputs from the exerciser to settle.

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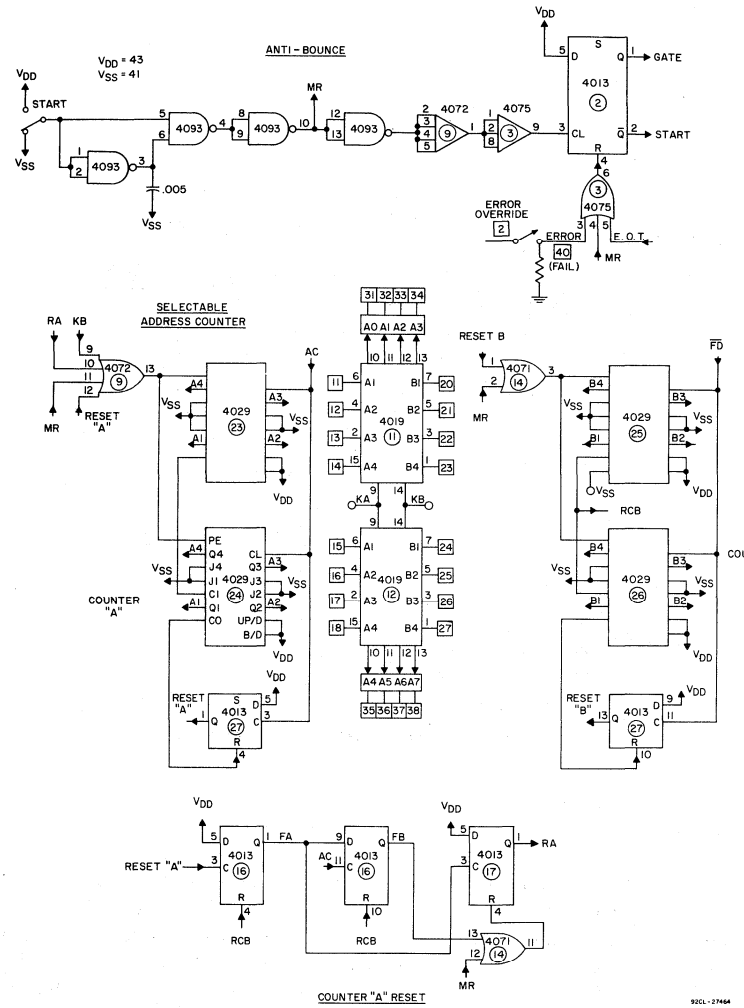
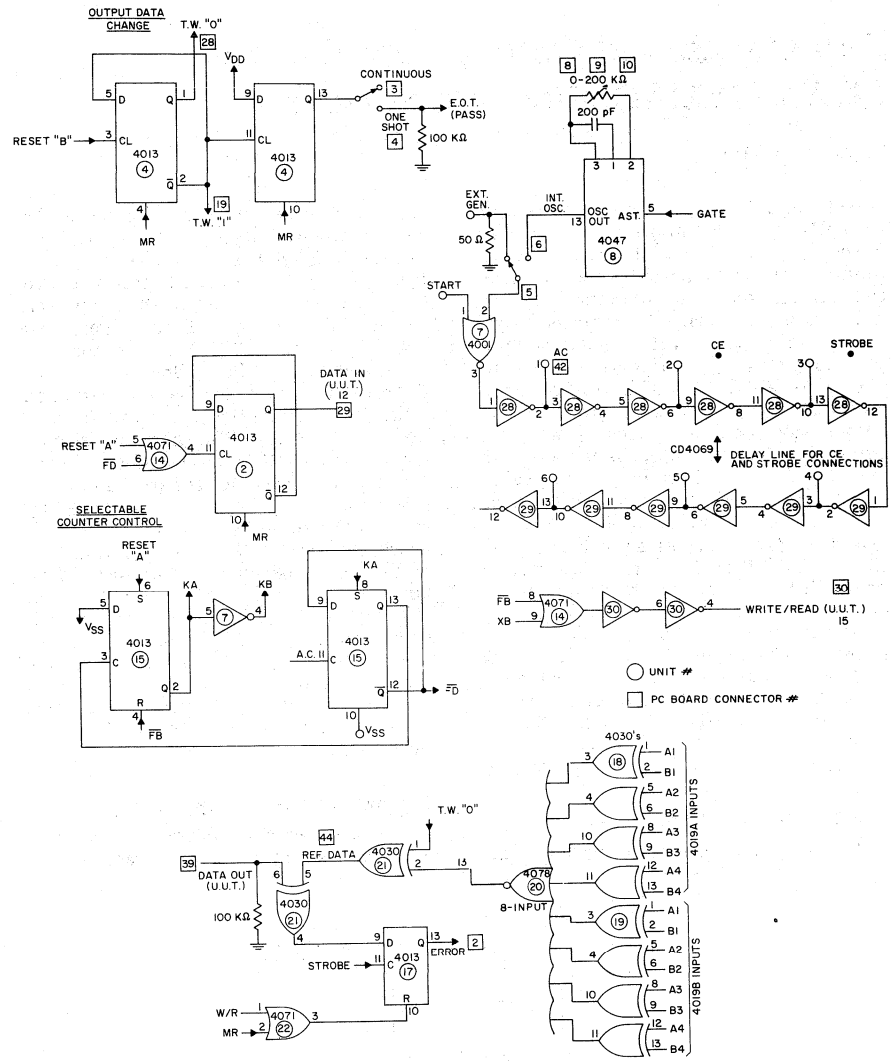


Fig. 14 — WALKPAT Memory Exerciser logic diagram. (Part 1)



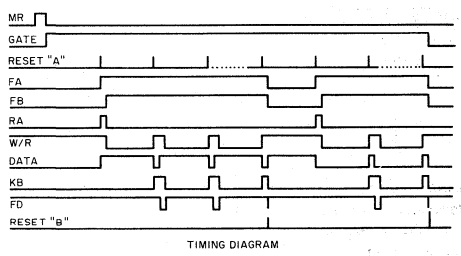


Fig. 14 – WALKPAT Memory Exerciser logic diagram. (Part 2)

ACKNOWLEDGMENTS

The assistance of J. Donnelly, O. Harasymowych, H. Riehman, and R. Vaccarella in the construction and testing of the circuits presented in this Note is acknowledged.

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1. "COS/MOS 256-Word-By-1-Bit Static Random-Access Memory," RCA Data Bulletin, File No. 768.
2. "Common Problem Areas and Pitfalls of Testing Semiconductor Memories," Macrodata Co., MD-100 Field Application Note No. 7.

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Register-Based Output Function for RCA COSMAC Microprocessors

by N. P. Swales

This Note describes a circuit for use with RCA COSMAC Microprocessors; the circuit provides the capability to output information from any of the 16 general-purpose scratch-pad registers contained within the CPU. This circuit is of particular interest to users constrained to operating with memory systems containing only ROM, or to users wishing to transfer 16 bits of data with a single Output instruction. The information given and the terminology used are presented with the assumption that the reader is familiar with the COSMAC architecture and manuals.[1]

Although other logic implementations of the functions described in this Note are realizable, the examples given employ the CDP1852 I/O Port. For further information on the CDP1852, the user should refer to the data sheet.[2]

The circuit in this Note provides a mechanism for transferring data from one of the 16 general-purpose registers contained in the COSMAC CPU to an I/O device. The data is transferred to the I/O device via the Memory Address Bus from the CPU rather than via the Bidirectional Data Bus from the Memory System.

One-Byte Transfer Configuration

Fig. 1 shows a simple configuration designed to transfer the data contained in the low-order byte of one of the 16 CPU registers to a CDP1852 I/O port. The I/O port is configured in a manner similar to that described in the data sheet for the CDP1852; however, instead of connecting the Data In lines of the CDP1852 to the CPU Data Bus, they are connected to the CPU Address Bus. During the execute cycle of the Output instruction which is to transfer the data to the I/O port, the contents of the CPU register specified by the X register (R(X)) are transferred to the memory system via the Memory Address Bus (the most significant byte first followed by the least significant byte). At the time during which TPB occurs, the least significant byte of R(X) is available on the memory address bus lines and is therefore transferred into the I/O port. It should be noted that the output data contained in the CPU register is incremented by one, and that this operation causes a read from the memory system. However, the memory data byte resulting from this operation is ignored by the rest of the system.

Two-Byte Transfer Configuration

Fig. 2 shows a configuration similar to Fig. 1 which may be used to transfer both

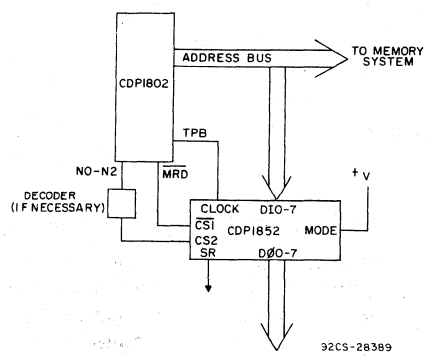

Fig. 1 — Circuit configuration for transferring data from the least significant byte of one of the CDP1802's 16 general-purpose registers to an I/O device.

bytes of one of the CPU's general-purpose registers to an I/O device. TPA is used to transfer the high-order byte of the register into the CDP1852 on the left, and TPB transfers the low-order byte into the CDP-1852 on the right. In this configuration, care should be taken to meet the timing requirements of the CDP1852 and the CDP1802 for the transfer of the most significant byte of data.

References

1. User Manual for the CDP1802 COSMAC Microprocessor, MPM-201A.
2. CDP1852 Series, 8-Bit Input/Output Port; Preliminary Data Sheet.

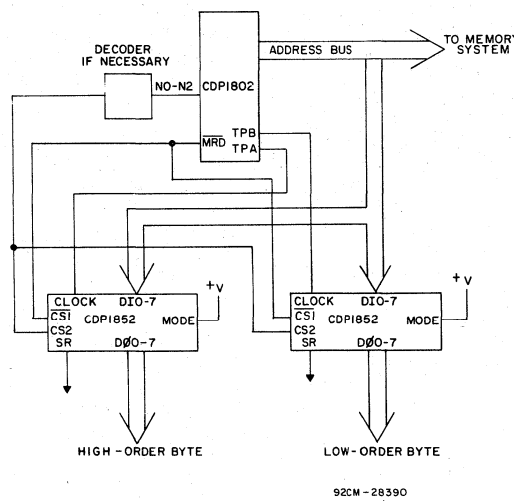

Fig. 2 – Circuit configuration for transferring the full contents (two bytes) of one of the CDP1802's 16 general-purpose registers to an I/O device.

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Design of Clock Generators for Use with RCA COSMAC Microprocessor CDP1802

by D. Hillman

Clock signal generation for the CDP1802 COSMAC Microprocessor is simple and straightforward. The CDP1802 features of static operation, single-phase clock input, and the on-chip oscillator amplifier make practical the use of a low-cost, highly stable, crystal-controlled oscillator as its clock generator. The design of external oscillators for this purpose, crystal or RC controlled, is equally straightforward and they require only minimal circuitry. In addition to the oscillator amplifier, the CDP1802 incorporates all necessary start/stop logic on-chip. This application note describes clock generator designs suitable for various applications.

Crystal Oscillator Design

The basic oscillator circuit for the CDP-1802 consists of the on-chip amplifier and an external feedback network as illustrated in Fig. 1. For oscillation to occur, the gain of

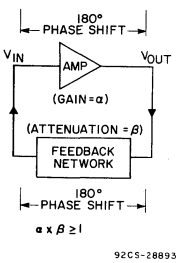

Fig. 1 – Basic oscillator circuit.

the amplifier (α) times the attenuation (β) of the feedback network must be greater than or equal to one. In addition, the total phase shift through the amplifier and feedback network must be equal to N times 360 degrees, where N is an integer. Oscillations occur in any system in which the amplified signal is returned in phase to the amplifier after being attenuated less than it was originally amplified.

The frequency stability of an oscillator is primarily dependent upon the phase-changing properties of the feedback network. Because of their high Q and inherent frequency stability, quartz crystals are commonly used in the feedback network.

A parallel resonant oscillator circuit is shown in Fig. 2. The phase angle for the type

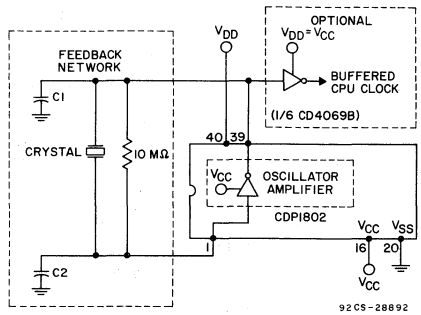

Fig. 2 – Parallel resonant oscillator circuit.

of feedback network shown in this figure is extremely sensitive to a change in frequency, a condition necessary for stable oscillation. If the equivalent resistance of the crystal is in fact zero (infinite Q), a change in phase angle of the feedback circuit would not cause any change in oscillator frequency. Therefore, for an oscillator of highest stability, the Q of the crystal should be as high as possible. In general, Q increases with increasing frequency.

The crystal load capacitance, C_L, is defined as the series sum of C_1 and C_2. Higher values of crystal load capacitance generally improve frequency stability, but also increase power consumption. The choice of equivalent load capacitance (usually specified to the crystal suppliers) only fixes the series sum of the two capacitors C_1 and C_2. The value of the amplifier output capacitance C_1 should not be fixed. A trimmer should be connected in parallel with, or used in place of, a fixed output capacitor to permit compensation for variation in stray capacitance and circuit component values.

The required capacitance range for the oscillator trimmer capacitor is determined by the variation in oscillation frequency with load capacitance. The total trimming range is mainly a function of the crystal characteristics. For a more detailed analysis, see Reference 4.

Practical Oscillator Circuits

The amplifier, feedback network, and crystal considerations discussed in the preceding paragraphs can be combined for the design of a crystal-controlled oscillator for the CDP1802. The majority of microprocessor applications do not require the frequency of oscillation to be so exact as to require oscillator trimming. An "untrimmed" crystal oscillator will be within 1% of its specified crystal frequency. For most microprocessor applications the following simple guidelines can be used.

1. The crystal should be connected between terminals 1 and 39 of the CDP1802.
2. For crystal frequencies between 100 kHz and 6.4 MHz, a 10- to 22-megohm feedback resistor should be used in parallel with the crystal.
3. Capacitors C_1 and C_2 are not required but a value of between 20 and 30 pF for each is recommended to improve stability.

It should be noted that the on-chip oscillator and timing generator are capable of operating at frequencies higher than the microprocessor maximum operating frequency. For reliable operation, the crystal frequency must always be less than or equal to the maximum operating frequency specified in the CDP1802 data sheet.

A practical example, the CDP18S020 Evaluation Kit oscillator, consists of a 10-megohm feedback resistor and a 2-MHz AT-cut crystal, both connected in parallel across terminals 1 and 39 of the CDP1802. (Crystal: Part No. X023303; C_L=15 pF; Series M1; holder, series HC330; made by Turotel, Inc., 13402 S. 71 Highway, Grandview, Missouri 68030.) Provisions for oscillator capacitors are made in the Evaluation Kit, but their use is not required. The increase in oscillator stability with respect to supply voltage that can be obtained by adding the capacitors is shown in Fig. 3.

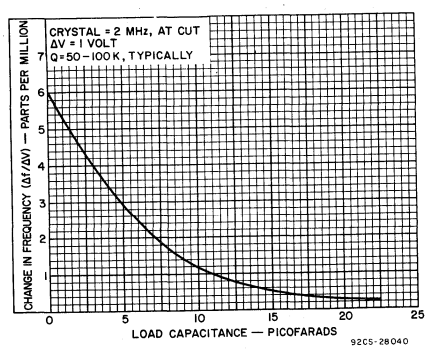

Fig. 3 – Stability of CDP1802 crystal oscillator as a function of load capacitance value.

The amplifier stability also depends upon the value of the resistor in the feedback network. Fig. 4 shows the relationship between the feedback resistor value and oscillator stability. The curve indicates that 10 megohms is an adequate value for the feedback resistor.

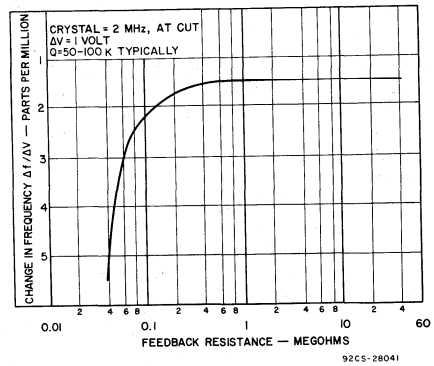

Fig. 4 – Stability of CDP1802 crystal oscillator as a function of feedback resistance value.

External Clock Generators

For low-frequency applications (less than 500 kHz) a cost-effective approach may be to use external RC-controlled oscillators. Three simple RC-controlled oscillators that may be used to clock the CDP1802 are shown in Fig. 5. When an external clock is used in

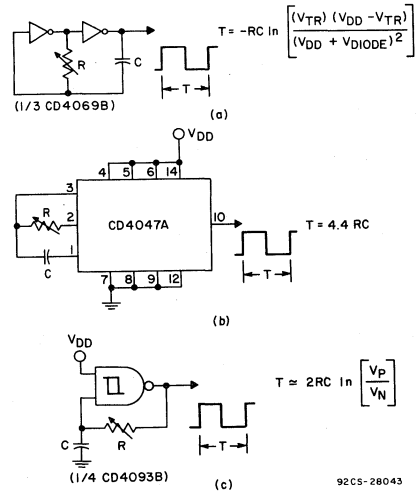

Fig. 5 – Three simple RC-controlled oscillator circuits suitable for use as external clock for CDP1802 microprocessor (output connected to pin 1 through Evaluation Kit P2-W).
(a) Inverter type oscillator (see References 5 and 6).
(b) RC oscillator using digital IC CD4047A (see References 5 and 6).
(c) Schmitt-trigger-type RC oscillator (see CD4093B data sheet).

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high-noise environments, a 20- to 30-pF capacitor between terminal 39 (XTAL) of the CDP1802 and ground may be used to increase the microprocessor noise immunity.

The selection of the R and C should be compatible with system requirements. The capacitor should be non-polarized and have low leakage. There is no upper limit for either R or C values to maintain oscillation. However, C should be larger than the inherent stray capacitance. R must be larger than the output impedance of the COS/MOS device, which is typically hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted. Based on these considerations recommended values for these components are:

C - greater than 100 pF, up to any practical value

R - greater than 10 kilohms, but less than one megohm

With large values of R and C, the circuit in Fig. 5(c) can be used. This circuit, because of its hysteresis, eliminates multiple output pulses caused by noise on the input RC waveform. For a more detailed analysis, see References 5 and 6.

Clock Buffering

In some applications it may be desirable to supply the CPU clock signal to other system components. In such cases the loading on the oscillator circuit should be minimized by buffering the clock through a COS/MOS inverter, as shown in Fig. 2. The loading presented by the inverter will be mainly capacitive, about 5 picofarads, and can usually be neglected in non-critical designs. The buffer should be located close to the crystal in order to minimize stray capacitance.

When the crystal oscillator is being trimmed to its desired frequency, the buffered clock technique should also be used to prevent the oscillator from being loaded by the frequency counter.

References

1. CDP1802 data sheet.
2. CD4047A data sheet, File No. 623.
3. CD4093B data sheet, File No. 836.
4. "Timekeeping Advances Through COS/MOS Technology", ICAN-6086.
5. "Using the CD4047A in COS/MOS Timing Applications", ICAN-6230.
6. "Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits", ICAN-6267.
7. User Manual for the RCA CDP1802 COSMAC Microprocessor, MPM-201.

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Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor

by W. F. Clark

This Note describes several circuits which enable a power-on reset/run capability for COSMAC microprocessor systems. It is assumed that the user is familiar with the hardware considerations for the CDP1802 as explained in the **User Manual for the CDP1802 COSMAC Microprocessor**, MPM-201A.

The power-on reset/run facility is useful in systems which periodically incorporate a power-down phase during system operation. During this power-down phase, care should be taken to prevent signals from reaching any of the microprocessor inputs or outputs because these signals could be coupled through the substrate protection diodes to the V_{DD} line and repower the system.

Clock Input Considerations

The waveforms in Fig.1 show the behavior of the supply lines and CLEAR line for resetting the microprocessor using two different modes of clock inputs, the on-chip crystal oscillator and an external clock source. The required reset pulse phasing is determined by the type of clock used in the system. When the on-chip oscillator is used, the delay in oscillator start-up depends on the loading on the CLOCK input. With 5-picofarad decoupling capacitors on the CLOCK and XTAL lines, a delay of 10 milliseconds is typical for oscillator start up at 25°C. To assure proper operation, the reset pulse should be active until the oscillator has stabilized.

When an external clock is used, it should be gated with the power-on signal. The reset pulse should allow for the V_{DD}, V_{CC} time constant and can be terminated when the clock is in a valid state or, typically, 20 microseconds following power-on. If the reset pulse terminates before the clock is running, internal registers I and N and the Q output will reset. Registers X, P, and R(0) will not reset, however, until the initialization cycle is completed.

Typical Reset Circuits

Some typical reset circuits are shown in Fig.2. The basic one-shot circuit is shown in Fig.2(a). The circuit in Fig.2(b) permits manual reset and allows access to the LOAD mode. The circuits in Figs.2(c) and 2(d) eliminate feedback resistors by using the CD4093 Quad 2-Input NAND Schmitt Triggers. Other variations of these circuits are possible following the above constraints.

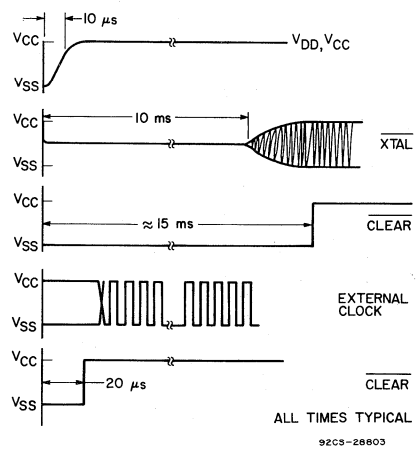

Fig.1 – Typical start-up waveforms.

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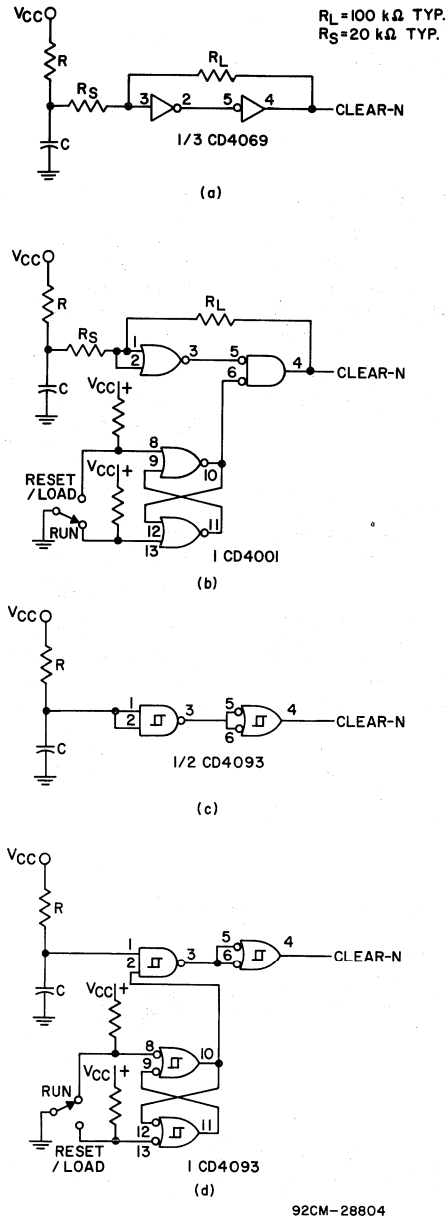

Fig.2 – Typical power-on reset/run circuits. IC supply leads are V_{CC} and V_{SS} or ground.

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Keyboard Scan Routine for Use with the RCA COSMAC Microterminal CDP18S021

by D. Block

The RCA COSMAC Microterminal CDP18S021 provides general-purpose subroutines in a utility program UT5 so that the Microterminal can be used as an output display device by the user program. In particular, the REGDIS subroutine sends the contents of registers RA and RB to the display, and the LEDD subroutine provides independent control of all eight display digits and decimal points. Refer to the **Instruction Manual for the RCA COSMAC Microterminal MPM-211** for details of their use. UT5, however, does not contain a general-purpose keyboard read routine that a user program can call. This Note contains the code for such a keyboard reading routine which can be added as a subroutine to the user program thereby making the Microterminal useful as a general-purpose input as well as output device.

Microterminal Operation

The following discussion assumes that the Microterminal is being used with the RCA Evaluation Kit CDP18S020. When one of the scanned keys of the Microterminal (0 through F, CA, $P, INC, or ←) is pressed, the $\overline{EF3}$ flag input to the CPU is set low. This line is then the basic signal indicating that the keyboard should be read. In the READ routine given in this Note, the keyboard is read by the 6C input instruction (INP 4) and decoded by comparing the byte against a look-up table occupying locations 8122-8135 in UT5. Register RA is used as a pointer to the table. Because of the special coding scheme used with the keyboard, keybounce produces invalid codes. The keyboard reading program described here will signal an invalid read by setting RA.0 equal to zero. The main program would then normally attempt another read operation until a valid code is found.

Microterminal Keyboard READ Routine

A flow chart for the Microterminal READ routine is given in Fig. 1 and the code listing in Table I. The READ routine assumes that the standard

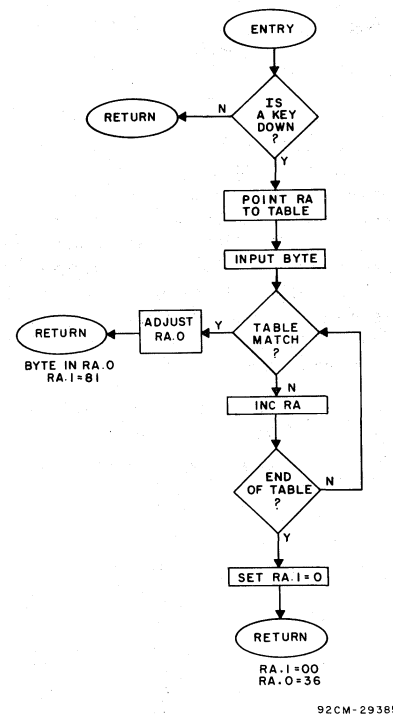

Fig. 1 - Microterminal Keyboard READ Routine Flowchart.

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Table I — Code Listing for Microterminal Keyboard Read Routine

```
READ:   BN3   END   ..IF NO KEY DEPRESSED, RETURN
        GHI   R4    ..POINT RA AT LOOKUP TABLE
        PHI   RA
        LDI   #22   ..TABLE AT 8122 FOR #13 BYTES
        PLO   RA
        INP   4     ..READ IN KEY TO STACK
FCOM:   LDA   RA    ..COMPARE AGAINST TABLE
        XOR
        BZ    FMAT  ..IF MATCH, GO TO FMAT
        GLO   RA    ..CHECK FOR END OF TABLE
        SMI   #36
        BDF   ERROR ..IF SO, GO TO ERROR ROUTINE
        BR    FCOM  ..IF NOT, TRY NEXT TABLE ENTRY

FMAT:   GLO   RA    ..ADJUST RA.0 TO EQUAL
        SMI   #23   ..KEY VALUE
        PLO   RA
END:    SEP   R5    ..RETURN WITH BYTE IN RA.0
                    ..AND RA.1 = 81

ERROR:  LDI   #00   ..SET RA.1 = 0 AND RETURN
        PHI   RA
        SEP   R5
```

COSMAC Call and Return subroutine convention is being used, and it uses RA for byte-transfer operations. Upon a successful read, the key code is entered into RA.0, and RA.1 = 81. An unsuccessful read is denoted by RA.1 = 0 (and RA.0 = 36). Table II gives the keyboard code assignments. If a key is not pressed, the READ routine executes an immediate return without altering RA.

Table II — Microterminal Keyboard Code Assignments

Key Depressed	Table Entry	RA.0 =
0	0A	0
1	8E	1
2	80	2
3	81	3
4	4E	4
5	40	5
6	41	6
7	2E	7
8	20	8
9	21	9
A	1E	A
B	10	B
C	11	C
D	06	D
E	08	E
F	04	F
↔	02	10
$P	09	11
INC	01	12
CA	0C	13

Note: The keys R, RU, and RP are not scanned inputs.

To distinguish among no key read, key invalid, or key valid, the following calling sequence for the READ routine could be used. First, set RA.1 = 1, call READ, and then examine RA.1. If RA.1 = 1, no key was read; if RA = 00 an invalid read occurred (due to key bounce); if RA = 81, a valid read occurred. These conditions are summarized in Table III. The calling sequence is given in Table IV.

Table III — Conditions on Exit from Read Routine

Condition	RA.1	RA.0
No key depressed	(no change)	
Key read invalid	00	36
Valid key read	81	(key value)

Alternative ways of signaling the main program via the READ routine can be developed. For instance, to distinguish between a read operation in which no key is pressed and one in which an invalid read occurs, the ERROR routine could be modified to set the Q flip-flop or DF. Typically, on an invalid read or a no-key-pressed operation one would simply re-read until a valid key was found. To assure that only one byte is read per key press, the user program should wait for EF3 = 1 before proceeding. In a system with a multiplexed display, the program would loop refreshing the display during this wait period.

Table IV — Code Listing for Calling Sequence

```
KEYSCN:  LDI    #01        ..Set RA.1 = 1.
         PHI    RA
         SEP    R4         ..Call the read routine
         ,A(READ)
         GHI    RA         ..Examine RA.1 for valid
                           ..Read operation
         BZ     KEYSCN     ..Invalid read, try again
         SHR
         BZ     NOKEY      ..No key read, go to no key
         GLO    RA         ..Key read: get value
```

References:

MPM-201A User Manual for the RCA COSMAC Microprocessor
MPM-203A Evaluation Kit Manual for the RCA CDP1802 COSMAC Microprocessor
MPM-211 Instruction Manual for the RCA COSMAC Microterminal

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Use of the CDP1856 and CDP1857 Buffer/Separator In CDP1802 Microprocessor Systems

by J. Oberman

The RCA CDP1856 and CDP1857 are four-bit bus buffers or separators intended for those applications that require interface with the CDP1802 bidirectional three-state data bus. They can be used to buffer the bidirectional data bus, for increased driving capability, or to separate the data bus into two unidirectional data buses. This Note describes the uses of the CDP1856 and CDP1857 and, more specifically, how they may be utilized in the RCA Evaluation Kit, CDP18S020, and the E-K/Assembler-Editor Design Kit, CDP18S024.

DESCRIPTION

The functional logic diagram for both the CDP1856 and CDP1857 is shown in Fig. 1. Both parts require a positive chip-select input signal to enable their outputs. They differ only in the polarity of the MRD input signal required to transfer data to the bidirectional data bus. The CDP1856 requires a negative polarity MRD signal, and can be used to buffer or separate data transfers between memory and microprocessor. The CDP1857 requires a positive MRD input signal and

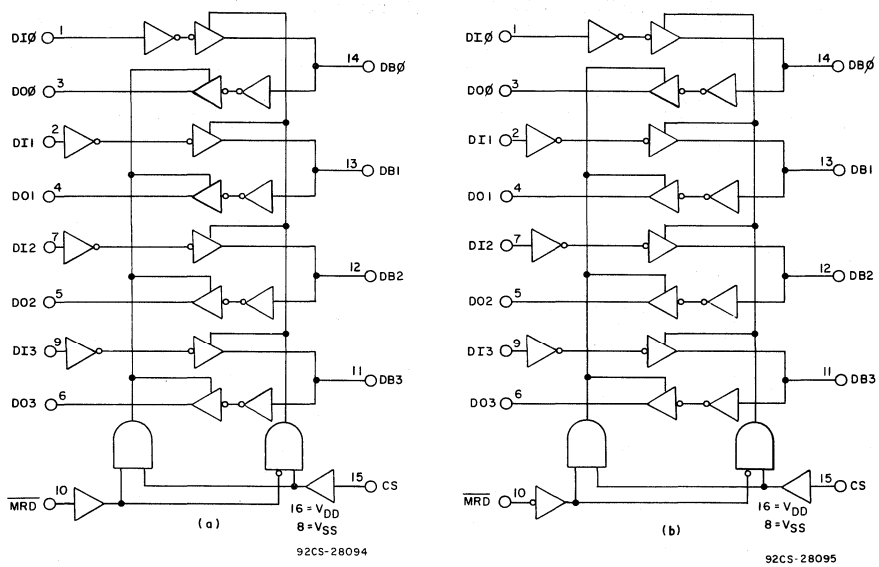

Fig. 1 - Functional diagrams (a) CDP1856, (b) CDP1857.

can be used for data transfers between the bus and various I/O devices.

As shown in Fig. 1, a typical buffer consists of two three-state drivers. On the bus side, the input of one driver is connected to the output of the other driver; they share a common terminal. However, their respective output and input are connected to separate terminals. When the chip is selected, only one output will be enabled, depending upon the polarity of the MRD input signal and the particular part.

APPLICATION INFORMATION

The CDP1856 may be used as a bus separator or bus buffer on the memory side of the bidirectional data bus. Similarly, the CDP1857 can be used for the same functions on the I/O side of the data bus. If an I/O command (N-bits) is present, the data transfer is from I/O to memory and microprocessor, otherwise the transfer is between microprocessor and memory. The MRD command, pin 7 of the CDP1802, determines the direction of the transfer.

If an I/O command is present, and MRD is high, the data transfer is from I/O device to memory and microprocessor, I/O M(R(X)), D. The MWR command will be asserted by the microprocessor. If MRD is low, the transfer is directly from the memory to the I/O device, M(R(X)) I/O. The microprocessor will ignore the data placed on the bus.

For a non-I/O instruction, I/O command lines low, a low level on the CDP1802 MRD output terminal indicates a data transfer from memory to microprocessor. If MRD is high, a data transfer from microprocessor to memory may occur; the output of data from the microprocessor to the bus and the presence of an MWR command later in the cycle will be the only indication of this occurrence.

The CDP1856 or CDP1857 may be used in conjunction with the RCA COSMAC Kits, CDP18S020 and CDP18S024 when large amounts of logic will be added to the microprocessor's data bus. The components may be mounted in the user area provided on the card with connections made directly to the user I/O connector if the additional logic is to be breadboarded externally. The points for connections to the data bus and MRD command are available along the left-hand side of the user area. Decoded I/O commands, I/O - 1 to I/O - 7, are available at the system connector, P-1.

Fig. 2 illustrates two techniques for using the CDP1856 either as a bus buffer or a bus separator to reduce the loading effects of large memory systems on the data bus. If the memory employs common I/O pins, the buffer configuration should be used. The bus separator configuration is useful if the memory does not have an output disable input or if it is desirable to maintain separate inputs and output connections to the memory devices.

The use of the CDP1857 is illustrated in Fig. 3. It is used on the I/O side of the data bus; its chip enable input may be connected to an I/O command output. Therefore, the CDP1857 can be used to gate information to a particular I/O device under control of the microprocessor. As discussed above, the use of the buffer or bus separator configuration will depend upon the needs of the particular application.

The CDP1856 and CDP1857 provide an efficient low-cost solution to the problem of interfacing with the CDP1802 bidirectional data bus.

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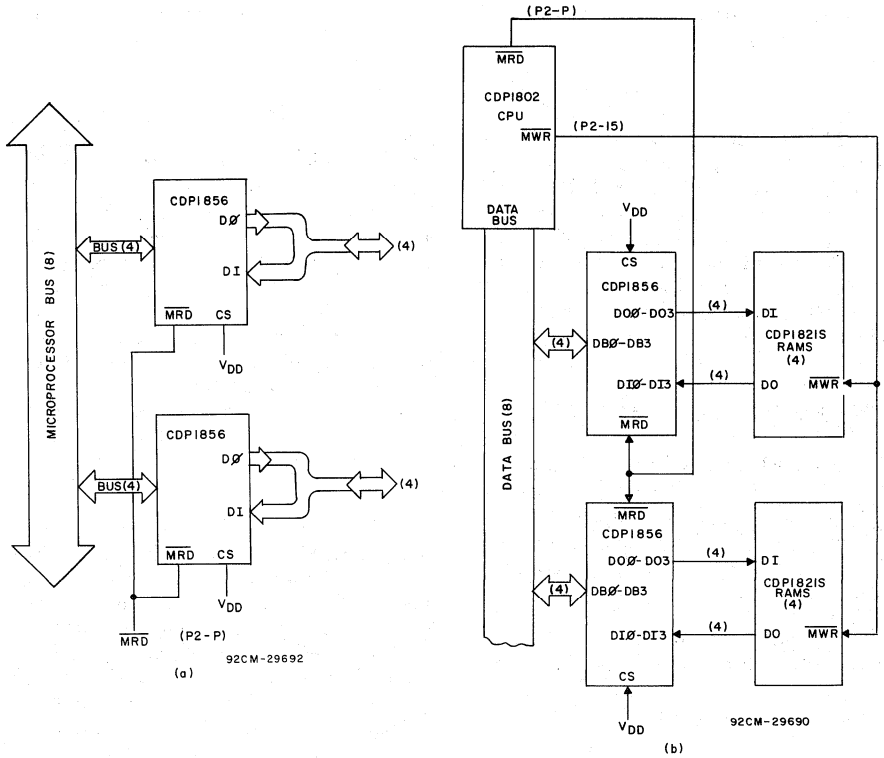

Fig. 2 - (a) Memory bus buffer, (b) memory-data bus separator.

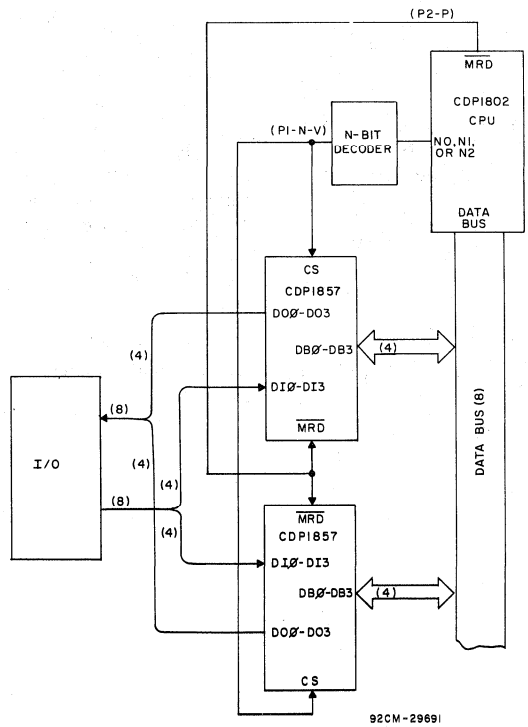

Fig. 3 - I/O bus separator.

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Software Control of Microprocessor-Based Realtime Clock

by Kaare Karstad

In many microcomputer applications, a precision time display such as a realtime clock or an accurate time delay must be generated to sequence program flow or to supervise assigned programming tasks. For example, in a data acquisition system, numerous measuring stations producing different physical quantities must be polled for data at predetermined rates to obtain a sufficient number of samples per unit time for each quantity; thus, this system would require a multicycle timer. Also, each sampled value must be associated with its realtime position. Another system example is where multistage processing cycles are programmed and executed sequentially, requiring a clock and a count-down timer.

In microprocessor-based systems, three timing options are usually available. The central processing unit (CPU) may have an on-chip timer or an interface with an external timer, or it may have to generate time bases under software control. Either a hardware or a software design may be implemented for measuring and monitoring real time, and each approach should be evaluated according to the specific application for cost-performance effectiveness.

A microprocessor-based clock system can generate a time base entirely in software. In this design, a 12-h clock, 4-yr calendar, and 12-h elapsed-time indicator are implemented and displayed on a 3½-digit multiplexed readout unit. The system is programmed with priority for the 12-h clock, and the other two timing functions are displayed for a predetermined time upon demand. The CDP1802 microprocessor[1] is a large-scale integration (LSI), complementary metal-oxide semiconductor (CMOS) 8-bit register-oriented CPU designed for use as a general-purpose computing or control element in a wide range of stored program systems.[1,2,3,4] It includes a dedicated direct-memory access (DMA) pointer on chip, which is used to generate timing functions with accuracies limited only by the crystal-clock oscillator tolerance. Designers can build a dedicated multifunction time display or simply incorporate the clock functions in specific applications. Advantages of the described system design are low cost, no external parts, high accuracy, and minimal software overhead. Inherent CMOS benefits include minimum power-supply requirements, completely static circuitry (no refreshing needed), wide temperature range, high noise immunity, and CMOS, transistor-transistor logic, and n-channel MOS interface compatibility.

Time Measurements

For a hardware design, timing can be done by external logic, in which a clock signal interrupts the microprocessor and updates a counter at a fixed time interval. For a software design, the microprocessor performs timing by monitoring its instruction flow, since each section of the program executes within a specific time. While the software ap-

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proach does not require external hardware, it does require skilled programming. To adjust a time-base interval for a constant value requires careful structuring, particularly with microprocessors having variable length instruction times. Interrupt and subroutine effects must also be thoughtfully evaluated.

For most microprocessors, the instruction time varies considerably within a given instruction repertoire according to which instruction is being executed. If the program also branches to a subroutine, which may call other subroutines to several levels deep, the task of generating a constant time-base period in software becomes complex. However, by utilizing the DMA function integrated into the CDP1802, an accurate software time base can be generated easily, regardless of the instruction sequence.

DMA Technique

Generally, DMA is a mechanism that allows an input/output (I/O) device to take control of the CPU for one or more memory cycles, in order to write into or read from memory. However, a different DMA technique in the CDP1802 generates a steady time base. For example, a register in this microprocessor is preloaded with an address to a specific memory location. When a DMA-IN request is generated by a peripheral, an 8-bit byte on the data bus is written into the addressed location. This write cycle takes place without CPU intervention, as a cycle is stolen from the instruction sequence. CPU execution then continues where it left off. Also, the address pointer is incremented to the next memory location, ready for the succeeding DMA cycle.

The CDP1802 microprocessor has 16 16-bit scratchpad registers—R(0) to R(F)—available to the programmer. For DMA operation, the first register, R(0), is automatically activated as a DMA address pointer, and is incremented once for every byte read from or written to random-access memory (RAM) as follows.

DMA-IN: BUS→M(R(0)); R(0) + 1 (1)
DMA-OUT: M(R(0))→BUS; R(0) + 1 (2)

In the DMA-IN mode, a byte on the data bus is written into memory location M(R(0)), addressed by the content of register R(0). Then, register R(0) is incremented to the next address.

If DMA-OUT is asserted, the microprocessor first completes its current instruction cycle and then executes a DMA cycle. When the DMA request is removed, the microprocessor returns to the next instruction; otherwise, it continues to execute DMA cycles as long as DMA-OUT is true. The microprocessor generates its own DMA request by hardwiring state code line SC1 to DMA-OUT (Fig. 1(a)). State code lines SC0 and SC1 are always interpreting one of the four CPU states—fetch, execute, DMA, or interrupt.

A normal CPU instruction sequence consists of two cycles—fetch and execute with SC1 low. When the microprocessor samples a DMA-OUT request (SC1 goes high), it responds with an added—or third—DMA cycle (Fig. 1(a)). When SC1 returns low, it effectively resets the DMA cycle so that the microprocessor reverts to the next fetch-and-execute pair. In this manner the normal 2-cycle sequence of fetch-execute is modified to a 3-cycle sequence: fetch-execute-DMA.

Since every DMA cycle increments register R(0), a mechanism exists for incrementing a counter automatically at a fixed known rate as the program is run, regardless of instruction type and program structure. The only restriction is to avoid CDP1802 3-machine cycle instructions (op codes C(N)), which require a fetch followed by two execute cycles; this involves not using the long branch, long skip, and no operation instructions, 17 of the available 91 basic instructions.

Measuring time is now reduced to monitoring B_{15}—the most significant bit (MSB) of R(0). During the time that R(0) counts to 2^{16}, bit B_{15} changes from 0 to 1 half way through the count (Fig. 1(b)). Thus, the designer can choose a convenient time increment to fill the register (e.g., 1 s) and then calculate the required crystal-controlled oscillator frequency.

$$T = \frac{1}{F} \times N \times M \times 2^{16}$$

where
N = number of clock pulses per machine cycle (eight for CDP1802)
M = number of machine cycles in modified (fetch-execute-DMA) instruction (three)

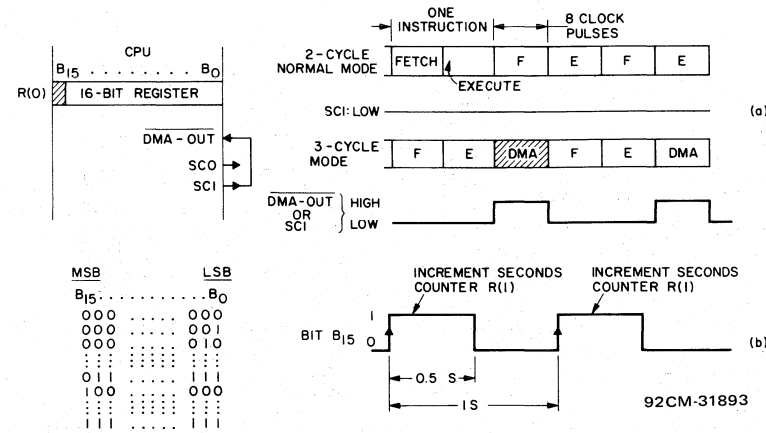

Fig. 1 — DMA technique. Normal Fetch-Execute instruction sequence (a) is modified to include DMA cycle by hardwiring state code line SC1 to DMA-OUT. Each time instruction is executed, 16-bit register is incremented. Monitoring MSB B_{15} state transitions from 0 to 1 (b) reveals when 1 s has elapsed.

Therefore, for T = 1 s, F = 1.572864 MHz.

Four bytes in RAM are assigned to store the four digits (two for hours and two for minutes) for the 12-h clock display. The lower order byte of scratchpad register R(1) in the microprocessor is allocated as a counter for seconds. Consequently, updating the clock buffers in RAM becomes a matter of incrementing the right digit(s) once every 60 s to count minutes.

The required main program (see Fig. 2) is short and consists of calls to various subroutines, such as updating, display, and setting the clock time. However, each pass through the main program varies in length according to branch conditions. For instance, if the test for 60 s is not met, no updating of the four RAM buffers is required, and the updating section of the program is bypassed. The important point is that the microprocessor must check the 0 to 1 transition of B_{15} in R(0) at least once every 0.5 s, and then increment the R(1) seconds counter if a transition takes place (Fig. 1(b)).

With the microprocessor multiplexing the four display digits at a 100-Hz refresh rate (well above the flicker rate of about 50 Hz), 10 ms is the longest time that the CPU is tied up in timing loops. A complete pass after each update takes only 1 to 2 ms in the full program under discussion. Hence, the critical transition test of R(0), at least once every 0.5 s, can easily be met.

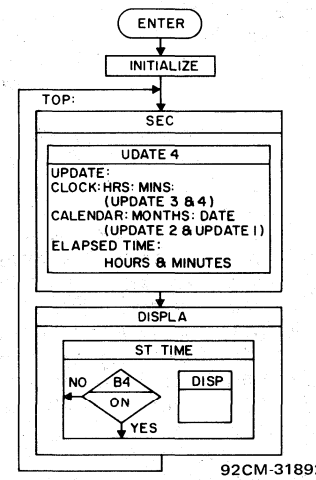

Fig. 2 — Program flowchart. Main program calls only two major subroutines—SEC and DISPLA. SEC calls UDATE for updating RAM buffers. If clock is being set, DISPLA calls STTIME, which again calls part of DISPLA and debounces pushbutton. SEC counts seconds, generates minutes, updates clock, elapsed time, and calendar. Updating takes place when SEC calls subroutine UDATE4.

System Description

The microprocessor-based clock system (Fig. 3) can output 8-bit bytes of information from any of its 16 scratchpad registers with only one output instruction, causing the 16 bits to go out over the memory address (MA) bus. Since this bus is only eight bits wide, the higher order byte appears first and is latched in the CD1852 input/output (I/O) port by

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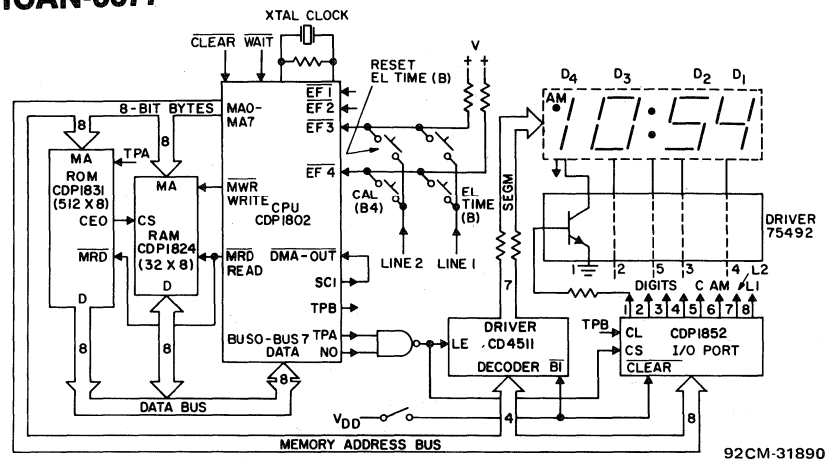

Fig. 3 — Microprocessor-based clock system. Timing functions include multiplexing and outputting to 3½-digit display, accurate timekeeping in software, and monitoring four request pushbuttons. Software gives priority to 12-h clock display; upon request, elapsed time or 4-yr calendar display stays on for predetermined time.

timing pulse A (TPA). The lower order byte follows later in the same machine cycle and is latched by timing pulse B (TPB) in another I/O port.

In the microprocessor, a 16-bit scratchpad register, R(F), stores the current content of a memory location for the multiplexed 3½-digit display (Fig. 4). Four binary-coded decimal (BCD) data bits of the higher order byte are decoded by the CD4511 interface device, which drives the seven segments of each light-emitting diode (LED) display digit. Eight bits of the lower order byte, via the CDP1852 I/O port, specify the digit address for multiplexing the four LED displays, as well as additional information for enabling the colon and am time-period displays. When the program executes an output instruction, this 12-bit word travels over the memory address bus in two bytes to the output ports selected by I/O command N0 and provides complete display information for each multiplexed digit. Upon completion of each machine cycle after data are latched, the I/O ports are deselected by N0. Register R(F) bit assignments for the required 12-bit output of the memory address bus are shown in Fig. 4. For example, when the least significant bit (B0) is set to 1, display digit D1 is selected. In the 12-h clock mode, colon bit B4 is also 1, and period bit B5 is 1 during am. Content of the first location in clock buffer D1 (minutes) is next stored as BCD data (bits B_8 to B_{11}) in the higher order byte of R(F). An output instruction then outputs the 12 bits, thereby turning on display digit D1. A timing loop in software keeps this digit on for 2.5 ms, after which a test is made to determine whether all four digits have been handled.

In the primary or clock mode of operation, the system displays hours and minutes continuously, and calendar (month and date for up to 4 yr) or elapsed time (hours and minutes) upon pushbutton request. The latter two displays stay on for a preprogrammed time (for example, 5 s), and program control then automatically reverts to the 12-h clock display. The implemented system has four operator-activated pushbuttons—calendar (B4), elapsed time, reset elapsed time, and one spare. Two external flag lines ($\overline{EF3}$ and $\overline{EF4}$) and two scan lines (L1 and L2) form a 2 by 2 matrix (Fig. 3) from the I/O port to test pushbutton status. In the programmed I/O mode, data transfers are controlled and timed by the program. The flag lines sense external events, i.e., whether the logic levels on the flag lines are high or low. At a certain point in the program sequence, one scan line at a time is made active low. If one of the two pushbuttons (Fig. 3) connected between this scan line and either flag line ($\overline{EF3}$ or $\overline{EF4}$) is depressed, the activated pushbutton is identified by branch instructions that test the two flag lines. If no pushbutton is depressed, the program proceeds to output hours and minutes data, which is the normal 12-h display mode. If, for instance, the elapsed-

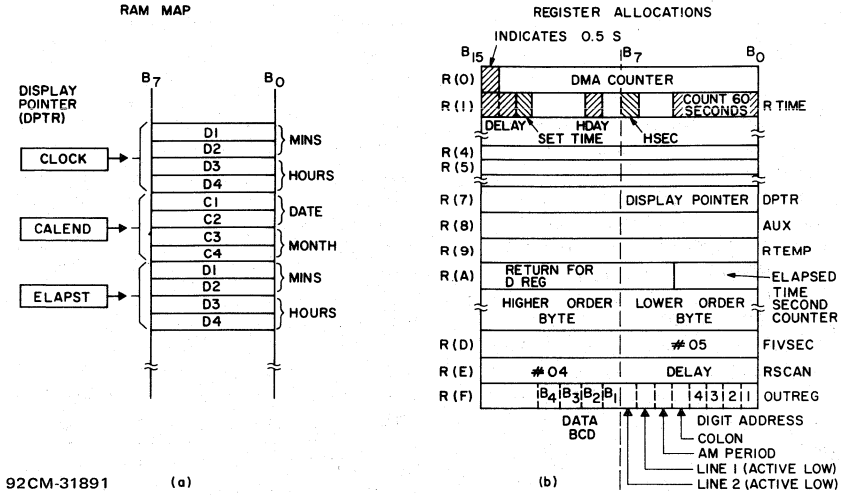

Fig. 4 — CPU registers. Memory map (a) shows RAM buffers for clock, calendar, and elapsed time. Register and bit allocations (b) are contained in CPU for programming. DMA pointer R(0) keeps track of time; register R(F) contains output data for LED displays.

time pushbutton is activated, the RAM pointer moves to the four elapsed-time buffers, and the system displays elapsed time for a predetermined period.

Updating of RAM Buffers for Time Displays

A memory map of the RAM buffers to be updated is shown in Fig. 4(a), and major register allocations and bit assignments are defined in Fig. 4(b). In RAM, three buffer areas, with four bytes in each, are reserved as display buffers for clock (CLOCK), calendar (CALEND), and elapsed time (ELAPST).

A 0.5-s flag bit (HSEC)—B_7 in R(1)— is assigned to monitor bit B_{15} in the DMA counter, R(0). Assume that the HSEC bit is 0; thus, when B_{15} is 0, 0.5 s has not elapsed, and software control returns to the main program. However, when B_{15} goes to 1, the 0.5-s transition has occurred, and the HSEC bit is updated to 1. The lower five bits of register R(1), assigned as a counter for 60 s, are next incremented, and the program checks whether the count is 60 or greater. If the answer is yes, a minute has passed. Therefore, the 60-s counter (five low order bits of R(1)) is reset to 0, and the four RAM locations (D1 to D4) storing the clock hour and minute values are updated. The next step is to check whether the lower order byte of register R(A)—allocated as an elapsed-time seconds computer—has overflowed. If the answer is yes, the four elapsed-time RAM buffers are updated.

Register R(7) is loaded and points to the least significant digit (D1) of MINS (minutes) in the RAM clock buffer. The addressed memory byte is incremented and examined for updating. If the value is less than nine, a 0 is stored in the buffer, and the minutes D2 digit is incremented and examined. If D2 is greater than five, a 0 is stored in the location for D2. For a 12-h clock, it is necessary to examine only D4 for 0 to 1. If D4 is 0, D3 is incremented and tested for the nine limit. If D3 is greater than nine, a 1 is loaded into D4 and a 0 into D3. If D4 is 1, then D3 is incremented and examined. When D3 is greater than 2, a 1 is loaded into D3 and a 0 into D4, since the clock changes from 12:59 to 01:00. Note that while the clock makes this change, the elapsed-time display proceeds from 12:00 to 00:01. Consequently, minute digits D1 and D2 are handled differently by the program according to whether the clock or elapsed-time buffers are being updated. Therefore, a test is made by the program to determine which buffer area is being updated. This information is provided by comparing the current address of the display pointer (DPTR) with the known fixed address for that location in the elapsed-time buffer.

With the clock and calendar displays, am and pm must be tracked for 24-h monitoring. Flag bit (HDAY)—Bg in R(1)—is defined as 0 for pm. Once every 12 h, when D3 is 2 at noon and midnight, the HDAY flag is complemented and examined. For

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pm, the stored HDAY bit reads 0; no action is needed and software control returns to main. When the HDAY flag reads 1 (am), the 24-h transition point has been passed, and the program proceeds to update calendar month and date.

This system implements a 4-yr calendar, in which the correct number of days for each month is indicated automatically by pointing the value of the current month to a table stored in read-only memory (ROM). If the current date is less than the table entry, no action is required; otherwise, 01 goes into the two calendar-date buffers (C1 and C2).

Setting Clock and Keyboard Debouncing

A series of manual B4 (calendar) pushbutton depressions sequentially updates the contents of all 8 RAM buffers to the correct readout by incrementing the four LED display values.

Pushbutton Depression	Result
1. B4 and reset elapsed time (simultaneously)	Enter set clock mode; circulate month display
2. B4	Stop month display; circulate date display
3. B4	Stop date display; circulate hours display
4. B4	Stop hours display; circulate minutes display
5. B4	Stop minutes display; blink colon display
6. B4	Stop colon display; reset seconds display; run clock time

Flag bit B_{13} (set time) is allocated in R(1) to indicate this mode. It is tested during all update routines, and essentially permits exits at appropriate program points; hence, the calendar-month value, for instance, is updated without affecting the other RAM buffers.

Entering the set clock module requires that both the calendar and reset elapsed-time pushbutton be depressed simultaneously. The program then points to the RAM buffers for calendar month and date and calls the display routine after a 0.5-s delay. As long as calendar pushbutton B4 is not activated, the third and fourth display digits will indicate the current content of the two month locations (C3 and C4) in the calendar buffer for 0.5 s. Next, the update routine for calendar month is called, and the contents in the two buffers are incremented and updated. Then, the sequence is repeated. The new buffer content is displayed for 0.5 s, the buffers incremented, and the procedure repeated until pushbutton B4 is once more manually depressed. Pushing B4 again freezes the calendar-month value, and the program exits to the next loop, which starts updating the calendar date in a similar manner at a 2-Hz rate.

Loops for date, hours, and minutes are functionally similar to the loop described for month. They all use the update subroutine; only entry and exit points change according to which RAM buffer is being updated. At the end of this sequence, when all 12 RAM buffers have been updated, the colon starts blinking at a rapid rate (10 Hz) to indicate that the clock is set but not yet running. A final manual depression of B4 resets the seconds counter, R(1), and starts the clock.

When pushbutton B4 is depressed to set the clock, a second test is made after a time delay determined by the execution time of routine DISP to debounce the leading edge of the pushbutton depression, the only critical edge for operation. If pushbutton B4 is still held down, the program locks up in a loop for the duration of the depression. During this period, the contents of the selected RAM buffer are being displayed. Upon release of the pushbutton, the program exits from the debounce routine to the set time (STTIME) routine.

Main Program

With the assembly program structured in a number of interrelated subroutines, the main program (see panel of Realtime Clock Software Programs) contains only four instructions after initialization. These call two major subroutines—SEC (seconds) and DISPLA (display)—and one minor display subroutine (DISP). Instruction SEP R4 changes the current program counter to register R(4), and starting address A(SEC) for the SEC subroutine is loaded during the call. The SEC subroutine counts DMA requests (time base) and increments the 60-s counter, R(1). After each minute elapses, the SEC subroutine calls another subroutine (UPDATE 4) for updating the 12 RAM buffers. The 12-h clock is updated first, then elapsed time. Next, the main program

Realtime Clock Software Programs

Main Program

```
TOP:    SEP R4, A(SEC)          Count seconds,
                                generate minutes,
                                update clock,
                                elapsed time, and
                                calendar
        SEP R4, A(DISPLA)       Display content of
        SEP R4, A(DISP)         relevant buffer
        BR TOP                  Go around again
```

SEC Routine

```
SEC:    GLO RTIME               Get HSEC bit
        SHL
        BNF HSEC0               BR if HSEC = 0
        GHI R0                  Else,test for 1 to 0
        SHL                     Transition
        BNF LABEL1              BR if transition
                                  made
        SEP R5                  Else, return
        Continue
        - - -
HSEC0:  GHI R0                  Test for 0 to 1
        SHL
        BDF LABEL2              BR if made
        SEP R5                  Else, return
        Continue
        - - -
LABEL2: GLO RTIME               Set
        ORI #80                 HSEC = 1
        PLO RTIME               Replace
        GLO DPTR                Hold DPTR
        PLO AUX                 During update
        INC RTIME               Increment
                                  seconds
        INC ETIME               Increment
                                  elapsed
                                  seconds
        GLO RTIME               Test for 60
        SMI B'10111100'         Seconds
        BNF LABEL3              No, branch
        LDI #80                 Zero seconds
        PLO RTIME               Leave HSEC = 1
        LDI A.0(CLOCK)          Point to
        PLO DPTR                Clock buffer
        SEP R4,                 Update clock
          A(UDATE4)             and calendar
        Continue
        - - -
```

UDATE 4 Routine

```
UDATE4: LDN DPTR                Get digit one
        ADI #01                 Increment it
        STR DPTR                Replace it
        SDI #09                 Test if > 9
        BM DIG10                BR if D1 > 9
        SEP R5                  Return
DIG10:  LDI #00                 Load 0
        STR DPTR                Into D1
        INC DPTR                Point to D2
        LDN DPTR                Get D2
        ADI #01                 Increment it
        STR DPTR                Replace D2
        SDI #05                 Test second digit
        BM DIG20                BR if D2 > 5
        SEP R5                  Else, return
        Continue
        - - -
```

DISPLAY Routine

```
DISPLA: LDI A.0(CLOCK)          Display pointer
        PLO DPTR                To clock
        GLO OUTREG              Turn off
        ORI B'10000000'         Line 2
        ANI B'10111111'         Turn on
        PLO OUTREG              Line 1
        SEX OUTREG              Line 1
        OUR 1                   Active low
        DEC OUTREG
        B4 ETBUFF               BR if ETIME
                                Button on
        B3 FUBUFF               BR if function X
                                Buffer on
        Continue
        - - -
DISP:   GLO OUTREG              Turn on
        ANI #F0                 First digit
        ORI #01                 Address
        PLO OUTREG
        LDI 04                  Assign
        PHI RSCAN               Digit count
        Continue
        - - -
```

STTIME Routine

```
STTIME: GHI RTIME               Turn on
        ORI B'00100000'         Set time bit
        PHI RTIME
        LDI A.0(CALEND)         Point to calendar
        PLO DPTR                Buffer
        LDI 50                  Load half second
        PLO RTEMP               Delay constant
        SEP R4, A(DISP)         Display calendar
        SEP R4,                 Button 4 on?
          A(BUTTN4)
        BNZ (LABEL4)            Yes
        DEC RTEMP               Else, no
        Continue
        - - -
```

calls the display routine, with the address given by A(DISPLA).

STTIME, used for setting the clock, is called from the DISPLA routine. When the operator sets the clock and watches the display, only the lower part of the DISPLA routine is needed. This part is called from the STTIME routine by loading the program pointer with address A(DISP).

A Standard Call and Return Technique[3] (SCRT) uses two linking subroutines: one when the call operation is to be performed and the other when the return from the subroutine is to be done. Registers R(4) and R(5) must be initialized once in the program to point to the linking call subroutine and the linking return subroutine, respectively. A call to a subroutine is performed by executing a SEP R4 instruction. The two bytes following this SEP instruction must

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contain the address of the subroutine to be called. Once a subroutine has been called and has completed its function, control should be returned to the caller by executing a SEP R5 instruction.

Seconds Subroutine

The SEC subroutine contained in the Realtime Clock Software Programs counts seconds, generates minutes, and updates clock, elapsed time, and calendar. Updating takes place when SEC calls subroutine UPDATE 4.

Bit B7 is stored in RTIME register R(1) as an HSEC flag. The first instruction fetches the lower order byte of register RTIME to the D register (CPU accumulator). The shift left instruction moves the bit into a 1-bit data flag (DF) register, where it can be tested. If the HSEC bit is 1, execution continues with the next instruction. The higher order byte of R(0) is fetched in order to test bit B_{15}; B_{15} is then shifted left into DF and its content tested. If this bit is 0, the routine executes a branch to address LABEL 1 (routine not listed) and resets HSEC bit to 0. If B_{15} is 1, the program returns to main. Register R(5) is a dedicated program counter for the return routine. If the first test of the HSEC bit reads 0, the program branches to an address given by HSEC 0. Again, the higher order byte of R(0) is read in order to test B_{15}, and the procedure is repeated.

Update 4 Subroutine

This routine updates the 12 RAM buffers pointed at by a display pointer whose address is either clock, calendar, or elapsed time (see Realtime Clock Software Programs). UDATE 2—part of UDATE 4—updates calendar month and date; UDATE 1 is the entry point in the STTIME mode when month values are being updated. The lower order byte of register R(7) is allocated as a display pointer (DPTR). In the display routine, it is initialized to point at the first location in the clock buffer.

Instruction "Load via N (LDN)" places the byte addressed by register DPTR in the D (CPU) register. Instruction ADI adds the constant 01 to the content in the D register, and the next store (STR) instruction stores the addition result within the D register into the memory location addressed by register DPTR.

Current content of the D register is tested for limit nine by subtracting the constant 09, instruction SDI #09. If the result is negative, the program branches to address DIG10. If the result is less than nine, a return to main is executed by SEP R5, which calls the return routine.

At the address given by DIG10, the load immediate (LDI) instruction loads a constant 00 into the D register. The next store instruction puts the value into the first (D1) location of the clock buffer. Register DPTR is then incremented so it points to the next byte in RAM (D2). This byte is loaded into the D register and a 1 is added to it, after which the result is stored back into D2 and the procedure is repeated for D3 and D4. After setting clock minutes D1 and D2, UDATE 3 is the entry point within UDATE 4 for updating the clock hours (D3 and D4) for both clock and elapsed-time buffers.

Display Subroutine

The display routine tests the status of the four pushbuttons and outputs data to the 3½-digit, multiplexed display. If a pushbutton is depressed, a new address is loaded into the display pointer, and data are output from the appropriate buffers for 5 s.

When the routine contained in the Realtime Clock Software Programs is called, the first instruction loads the address for the display pointer. Address A.0 (CLOCK) is the lower order byte for the clock buffer, and LDI puts it into the D register. Instruction PLO (put low) loads the content of D into the lower order byte of DPTR. The lower order byte of OUTREG —R(F)—is fetched to the D register, and its content is ORed with byte 80_{16} ($1000\ 0000_2$). Since scan line 2 is active low, ANDing the current content of D with hexadecimal constant BF ($1011\ 1111_2$) turns on scan line 1 and leaves line 2 unchanged, i.e., off. PLO puts this information back into OUTREG, and OUT 1 puts the content of OUTREG on the data bus. Scan line 1 is now active low. Since the output instruction incremented the data pointer, a decrement is done to reset the pointer.

Instruction B4 tests input flag $\overline{EF4}$ on the CPU. If the line is low and the elapsed-time pushbutton is depressed. then the program branches to address ETBUFF and sets the pointer to the elapsed-time buffer. If the test is not met, the program next tests the status of flag line $\overline{EF3}$, and the procedure is repeated.

Set Time Routine

Called only when setting the clock, the STTIME routine (see listing of Software Programs) calls debounce routine BUTTN4 and four update routines at various entry points, according to the values being updated: month, date, hours, or minutes. While the operator watches the LED displays during the STTIME mode, the entry to the display routine is at DISP.

Bit B13 in the RTIME register (R1) is allocated as a set time flag. The first instruction puts the higher order byte into the D register. Its content is ORed with hexadecimal constant 20 ($0010\ 0000_2$). When the result is put back into RTIME by PHI, the set time bit is set.

Address A.0 (CALEND) is the lower order address byte for the calendar buffer. The LDI instruction puts this value into the D register, after which PLO loads the address into DPTR. Delay constant 50, equivalent to 0.5 s, is loaded by LDI into the D register and is next stored in the lower order byte of RTEMP—R(9). Instruction SEP R4 calls the display routine starting at address DISP; the procedure is then repeated.

Summary

Hardware and software aspects of a microprocessor-based realtime clock application are covered, with priority given to a 3½-digit, 12-h clock display. Upon request, the same digits can display either a 4-yr calendar in months and days, or elapsed time in hours and minutes for a preprogrammed period. After this, the display automatically returns to the 12-h clock mode.

A timer or realtime clock is frequently needed in many microcomputer systems. Unless hardware is provided on chip, or added externally, timing must be implemented entirely in software. This task often requires carefully structured programs. The described software controlled clock design overcomes these difficulties by taking advantage of the inherent architectural capabilities in the CDP1802 microprocessor, such as DMA. Running any random program sequence automatically provides a known accurate time interval (for example, 1 s). The microcomputer system can be dedicated to various timing functions, and can easily be incorporated into another system where various time displays are required, such as adding a seconds display or an accumulated elapsed time. With a CMOS microprocessor and associated circuitry, this system design can be battery operated and requires less than 2 mA at 5 V, exclusive of the LEDs, for a typical program of 512 bytes.

Acknowledgment

The author wishes to acknowledge the contributions of Larry A. Solomon to this project.

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Optimizing Hardware/Software Trade-Offs In RCA CDP1802 Microprocessor Applications

By L.A. Solomon and D. Block

One of the chief reasons for choosing to design with a microprocessor rather than standard IC's is to reduce a system's parts count. To make the best choice requires a careful analysis of hardware/software trade-offs. This analysis usually narrows down to the ratio of ROM to I/O devices in the system. Economics indicates that the more functions handled in software, the less expensive and more flexible the system will be. Thus, a good design practice is to attempt to do everything in software initially and then relegate functions to hardware only as the speed/processing capability of the CPU becomes taxed. This Note will develop some examples of processor interfaces that not only minimize external hardware but, through judicious programming techniques, also minimize speed requirements on the CPU.

The RCA CDP1802 microprocessor is particularly well suited to minimum-cost interfacing because it has a significant number of terminal connections dedicated to I/O operations and an extensive set of I/O instructions. It has three I/O selection lines, called the "N" lines, that are controlled by I/O instructions plus four general-purpose flag input lines testable with branch instructions. There are also DMA-in, DMA-out, and Interrupt Request line inputs as well as two state code and two timing pulse outputs to synchronize I/O devices to the CPU. A single bit output (Q) which can be set or reset under program control is also provided. In all, 15 of the CDP1802 terminal connections are dedicated exclusively to I/O control. In addition, the CDP1802 has other unique architectural features, such as built-in DMA, that can be used to advantage. These features will also be discussed.

A CLASSICAL SYSTEM

A simple system having a keyboard input and a digital display output is shown in Fig. 1. The specific functions are

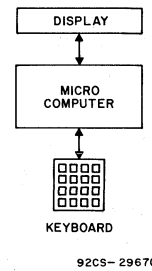

Fig. 1 - Simple microcomputer system.

omitted because the immediate concerns are only the microprocessor and I/O interfaces. These interfaces will be constrained by the programming technique choosen for the system. In the classical software control flowchart for this system, shown in Fig. 2, the standard

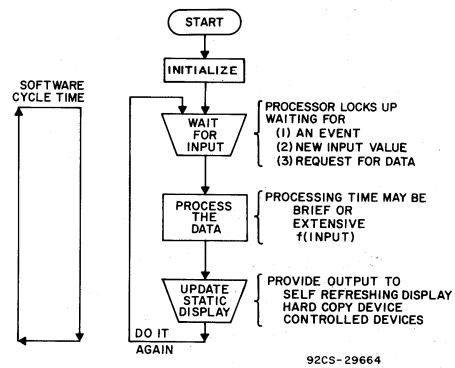

Fig. 2 - Classical software control flowchart for the system of Fig. 1.

initialization block is followed by an input, processing, and output procedure with a final loop back to repeat the action. Even without the details of the hardware or software design or the specific application, certain predictions can be made about this system.

First, consider the software cycle time, that is the time to go completely through one loop of the procedure. The cycle time is the sum of the time spent in each portion of the software, including input, processing, and output. Because the program apparently waits for an input, the time spent in the input block is indeterminate. The system cycle time, therefore, is indeterminate. This parameter has immediate impact on the selection of both input and output devices used in the system. The output device, for instance, must be capable of operating for prolonged periods without processor attention. Therefore, it must be a device that is self-refreshing or contains a latch. It certainly cannot be dynamic because no provision for refreshing is apparent in the simple software structure shown thus far. Because dynamically refreshed displays have the potential for lower cost, the static requirement is a serious drawback.

Next, consider an input device. A keyboard, being human operated, will present data to the processor at an uneven rate. The time between keystrokes may vary from a few milliseconds to several seconds or minutes. With the flowchart given, the processor must complete its processing before the next input can be received. If each keystroke requires some analysis by the microprocessor, a choice between using a very fast (and expensive) processor or lengthening the minimum time between keystrokes must be made. The first alternative would be very wasteful since the processor's very fast speed would only be needed in short bursts; most of the time it would be idling waiting for an input. The second alternative leads to an unresponsive system, one in which the operator will have to adjust to the system rather than the other way around. A third alternative is to design in an "intelligent" keyboard controller or buffering device to smooth out the input rate as depicted in Fig. 3. This alternative, however, is not ideal either because it requires additional hardware expense.

Resorting to additional hardware, however, may not be necessary if the flowchart of Fig. 3 is restructured. By doing the controller functions in the

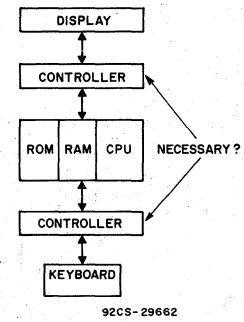

Fig. 3 - Addition of controllers to smooth out input rate.

software the controllers can be eliminated at only the cost of enlarging the system ROM. Moreover, because ROM's come in fixed increments, it may be no more expensive to have a program that is 1024 bytes long than one that is 527 bytes, even though one is nearly twice as long as the other. In fact, if there is unused space in the system ROM, the controller function may be had for "free". Even if an additional ROM is required, it may cost less than the MSI or LSI controller being replaced.

To take advantage of software control, the approach is changed, so that instead of waiting for an input to take place, the system simply looks at the input periodically. If no input is present, it skips the input operation and goes on to something else. That something else could be the refreshing of a dynamic display, for example, or some processing required as the result of the last input. If an input is present, then it is accepted and acted on. There are several options available for handling the processing associated with this input. If the input is small and can be handled immediately, the system will do so. If not, it can be saved for later when there will be time to handle it, or it can be broken up into small computational blocks interspersed among other tasks such as display refresh. These approaches are flowcharted in Fig. 4. The latter approach is the idea behind a powerful technique called interpretive programming in which functions such as display refresh and keyboard scan are written as modular subroutines. Calls to these subroutines, which pass or pick up parameters from the main program, can be interspersed throughout the main program wherever required by the system timing considerations.

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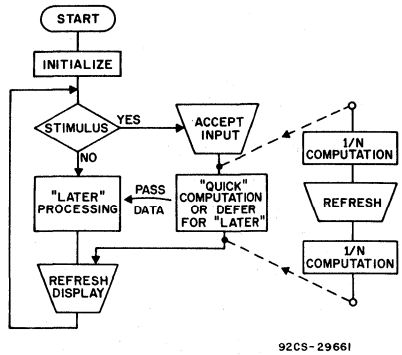

Fig. 4 - Controller function transferred to software and input loads interspersed.

HANDLING A DYNAMIC DISPLAY

Fig. 5 shows a typical multiplexed display system and Fig. 6 gives the details on the display refresh rate. The minimum refresh rate for any digit should be 100 Hz, which is fast enough to prevent flicker under most stationary display conditions.

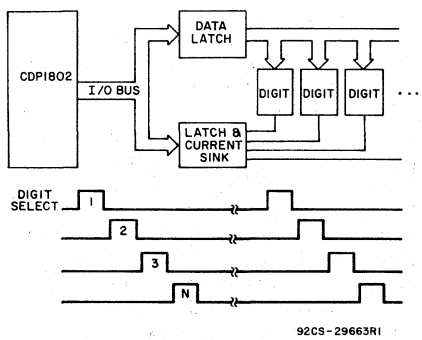

Fig. 5 - Typical multiplexed display system.

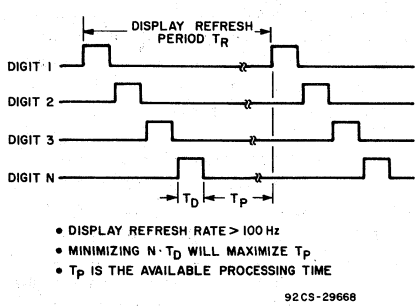

Fig. 6 - Details of the display refresh rate.

The actual ON time (T_D) of any digit is a trade-off between the intensity of the display and the time remaining within the 100-Hz refresh period for the processor to do some other work. It is desirable to minimize T_D so that a maximum of processing time (T_P) is left for the rest of the processing load.

It is customary to "overdrive" multiplexed LED displays to increase their apparent brightness. The extent to which overdrive is practical is a function of the duty cycle

$$\frac{T_D}{T_R}$$

of the display. This technique, however, is not without risk. Should the program crash or hang up (because of a program bug or noise injected into the system, or component failure, etc.), it is quite probable that a digit driver will be incinerated. Because of this hazard appropriate precautions, particularly when debugging a system, should be taken.

The segment information for a 7-segment display can be handled in either of two ways. If the data is in BCD, a device such as the CD4511 which contains a latch, BCD-to-7-segment decoder, and drivers can be used as shown in Fig. 7. Or,

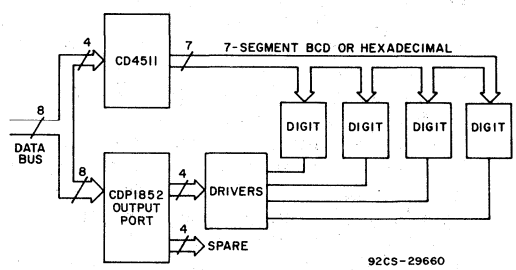

Fig. 7 - Handling segment information in hardware by means of a CD4511 BCD-to-7-segment latch decoder driver.

instead of the CD4511 that does code conversion in hardware, a software conversion via a look-up table can be used along with a simple output port as shown in Fig. 8. Hexadecimal or other codes are also easily accommodated in the table look-up method. But, because the output ports may not have sufficient drive to directly handle LED's, an intermediate stage of buffering may be necessary. No clear-cut recommendation can be made because variables such as the number of devices and the type of display chosen are significant.

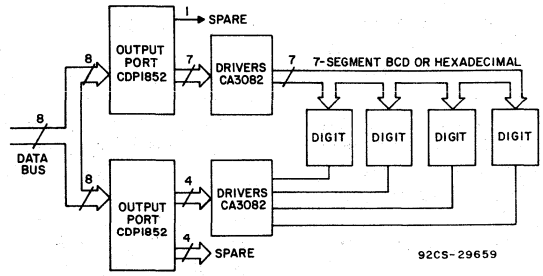

Fig. 8 - Handling segment information in software by means of an output port and lookup table.

SINGLE-SIGNAL INPUTS

The CDP1802 has four flag input lines that can be tested with branch instructions. These inputs are general purpose and can be used for such functions as interrupt vectoring, status indicators, or as single-bit inputs for slowly varying signals such as that of an ASCII terminal having a moderate baud rate. As an example, one of the flag lines is used as an input for a switch in Fig. 9. To signal

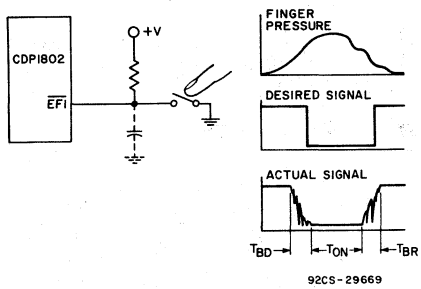

Fig. 9 - Basic switch circuit using microprocessor flag line.

the processor, a change on the flag line from a logic 1 to logic 0 level is used. However, the tendency of mechanical switches to "bounce" prevents this simplistic solution. The actual signal presented to the microprocessor consists of three parts - an initial bounce, a stable ON period, and a release bounce. A program looking only for a simple 1 to 0 to 1 transition may sense many switch closures because of the bounce noise. Although there are hardware solutions to this problem, software techniques may prove more cost-effective. Fig. 10 is a flowchart of a subroutine to debounce a mechanical switch. A test is made on the input signal to test for a switch closure. If none is found, a "switch down" software flag is

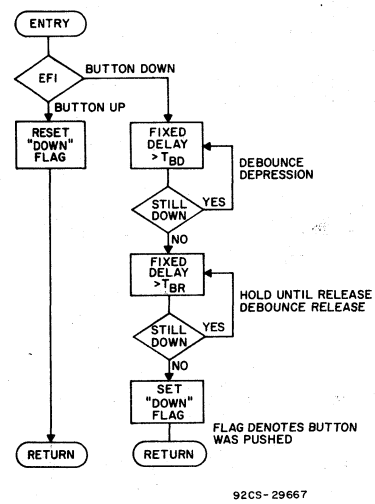

Fig. 10 - Flowchart of subroutine for debouncing a mechanical switch.

reset. This flag may be some convenient bit in one of the CDP1802's sixteen general purpose CPU registers or a bit in a RAM status word. If the switch is down, then the software will loop, waiting for the button to be released. The wait is performed to insure that the switch is not "seen" again for the current depression and to allow for the initial bounce period T_{BD}. Once the switch is released, the switch is again interrogated until it reaches a stable OFF condition. The software flag indicating a "switch down" condition is set, and the program returns to the caller. Although this program is easy to understand, it is, like the earlier simple solutions, not without its problems. For instance, the processor again wastes valuable time. The execution time (see Fig. 9) for this subroutine is at least

$$T_{BD} + T_{BR}$$

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and does, in fact, last as long as the button is depressed. Thus, it is obviously not suitable for systems having dynamically refreshed displays. A further drawback, from the human-engineering standpoint, is that a response is made on the release of the switch rather than on its depression, the opposite of what one would normally expect.

Fig. 11 shows a flowchart for an improved method that overcomes both of these drawbacks. Here, the subroutine that looks at the input signal has the capability of remembering what that signal was the last time it looked. This information is saved in a software flag called the "down flag". The routine operates as follows. If the button is now down and was also down the last time, then it is assumed that the system sees the same button depression seen earlier. A return is made to the caller with an indication of no new activity. If the button is not now down, but was the last time, then the switch has been released. In this case, the "down flag" is reset and a return made to the caller indicating no new activity (it is assumed that the processor is interested only in switch depressions and not their duration). But, if the switch is down now and was not down the last time, then there is a new depression. The switch must be debounced, the "down flag" set, and a message returned to the caller. Notice in the flowchart that a second test was made after the delay generated in the "busy work" block. This delayed second test is a debouncing technique to determine that the switch has been in the same state for two successive samplings before a decision is made on the true state of the switch. This method is still not optimal because the program is waiting (and therefore wasting time) during the debounce period. If some additional constraints are placed on the software cycle time, however, the program can be further optimized. For example, if the cycle time is greater than the bounce time (T_{BD}) but less than the switch ON time (T_{ON}), then the flowchart can be simplified to Fig. 12. Here there are no timewasting loops because switch bounce, in effect, will not be seen within the given timing restraints.

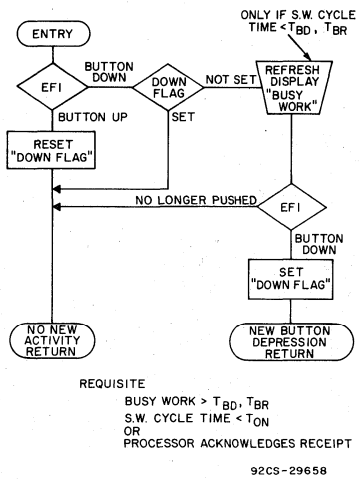

Fig. 11 - Flowchart of improved subroutine for debouncing a mechanical switch.

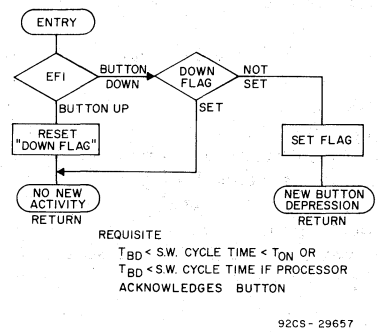

Fig. 12 - Flowchart of simplified debouncing subroutine benefitting from additional constraints.

MULTIPLE INPUTS

Up to four inputs can be handled as described above with each switch connected to a separate flag line of the CDP1802. Another technique is a multiplexing scheme in which the four switches are connected to one flag input, as shown in Fig. 13, and sequentially scanned as described in the flowchart of Fig. 14. This technique is readily expandable to additional scanned functions and, therefore, is discussed in detail. The

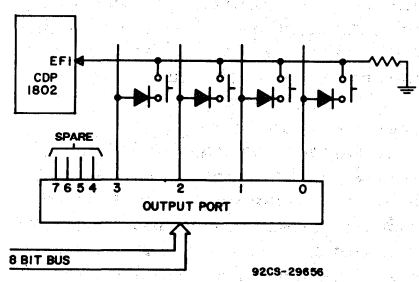

Fig. 13 - Hardware for handling four switch inputs on one flag line by means of a scanning routine.

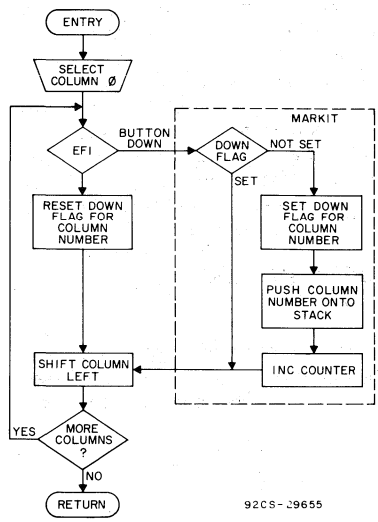

Fig. 14 - Flowchart of scanning routine for handling four switch inputs.

subroutine is designed to look for new switch closures and report them to the main program by "pushing" the switch number of a newly closed switch onto a stack and incrementing a counter. The main program will "pop" switch numbers off the stack and decrement the counter whenever the count is greater than zero. In the CDP1802 any one of the 16 general-purpose registers can be conveniently used as a counter because each has its own increment and decrement instruction.

The auxiliary functions for the subroutine are shown in Fig. 15. It is

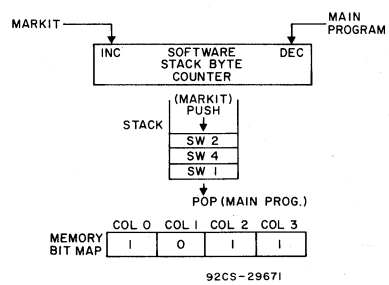

Fig. 15 - Auxiliary functions for the scanning subroutine of Fig. 14.

assumed that the timing constraints of Fig. 12 are met by this routine also, so that Fig. 14 is an extension of the basic flowchart previously developed. Upon entry into the subroutine, the first switch column is selected by outputting a 1 in bit position 0 of the data bus and examining the switch associated with that position. If a new depression is detected, the "down flag" is set for that switch in the memory bit map, the column number is pushed onto the stack, and the counter incremented. Next, the column is shifted and, if more columns remain to be scanned, the process is repeated. No switch closure or no new switch closure simply results in a column shift and continuation. When all columns have been scanned, a return to the main program is executed. The main program detects if any new switch closures have occurred by seeing if the counter has a value greater than zero. If so, the main program successively "pops" a switch number from the stack and decrements the counter until it reaches zero.

A section of the flowchart in Fig. 14 has been partitioned off and labeled "MARKIT". This routine is a common one that can be used as an expanded keyboard scan rountine discussed in the next section. It should be noted that the approach taken above lends itself well to a multi-processor system in which one processor handles the keyboard scanning and puts key numbers in a stack accessible to the other processors as well.

KEYBOARD SCANNING TECHNIQUES

Fig. 16 shows an arrangement for

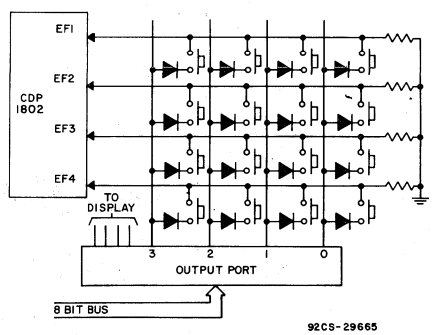

Fig. 16 - Hardware arrangement for handling a 16-key matrix using a scanning routine.

scanning a 16-key matrix. It is a simple extension of the arrangement just discussed. The horizontal lines can go directly into the four flag inputs of the CDP1802 as shown. Fig. 17 gives a flowchart of the software in which "MARKIT" is now responsible for handling row as well as column information. The basic interface between

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the main program and the keyboard scan subroutine remains the same; the subroutine place new key depressions on the stack and from there they are passed to the main program. Note that a key number's position on the stack does not necessarily represent when a given key was depressed with respect to the other keys on the stack, but merely indicates the order in which the keys were scanned. Because the stack is emptied on each cycle by the main program and only new key depressions are entered, the presence of two key numbers on the stack tells only that both keys were down when the scan took place. To discriminate in time between rapid key depressions, a short software cycle time is necessary. But, remember that this time must be kept within the constraints of T_{BR}, T_{BD}, and T_{ON}. There is a limitation to the technique discussed in that the software does not indicate to the main program when a key has been released. Thus, it can not be used in a system requiring lockout of other keys when any one key is down.

COMBINED DISPLAY AND KEYBOARD

The whole system of Fig. 1 is shown with its component blocks filled in on Fig. 18. The original objective to minimize

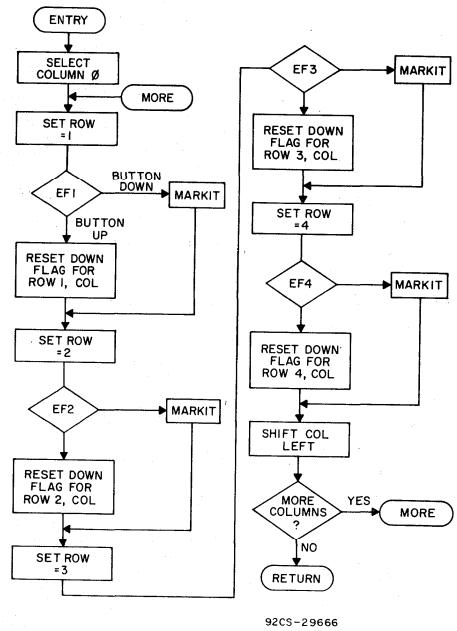

Fig. 17 - Flow chart of software for handling row and column information utilizing "MARKIT" routine.

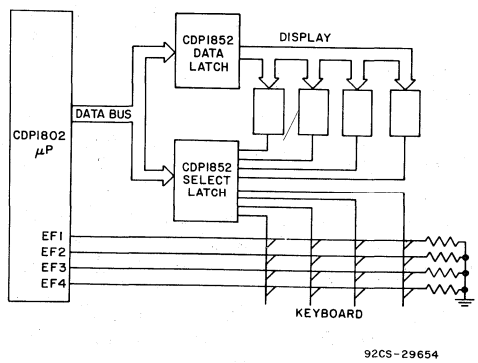

Fig. 18 - Simple microcomputer system of Fig. 1 with component blocks expanded.

hardware has been realized in that only two 8-bit output ports are required in this design besides digit drivers (not shown).

A further improvement can be made in the system by combining the keyboard scan and display multiplexing signals as shown in Fig. 19. Here, a single-byte

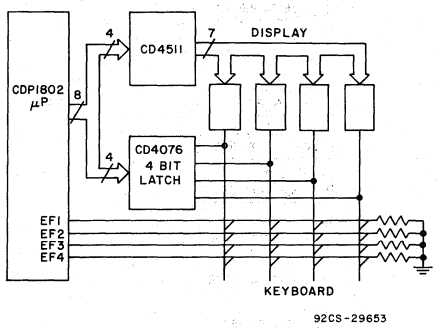

Fig. 19 - System improvement made by combining keyboard scan and display multiplexing signals.

output is used with the upper-order 4-bits being BCD data for the display and the lower-order 4 bits used to simultaneously select a display digit and keyboard column. This arrangement does not reduce the parts count, but does give smaller packages if space is a consideration and cuts down on the number of output operations and output bytes stored. A ready expansion of the system shown in Fig. 20 still uses only two IC's but permits scanning two 16-key keyboards and an 8-digit display.

TIMING GENERATION

In many applications it may be necessary to have some time-keeping ability in the microprocessor system. The requirements may range from having a time-of-day or elapsed-time clock to microsecond timing resolution for generating precision pulse widths. Here again, of the many approaches possible to timekeeping, a cost/performance-optimized one can be found.

Consider an example, shown in Fig. 21, for generating an output pulse of width T_1 each time switch S_1 is closed. The CD-

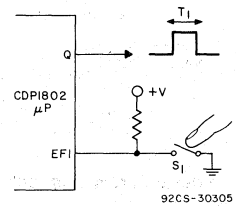

Fig. 21 - System for generating an output pulse for each switch closure.

P1802 has a single-bit output called the Q flip-flop that can be set or reset under program control to perform this function. The simplest technique for generating a fixed delay is by executing a series of "no-ops" in the program as illustrated in Fig. 22. If each "no-op" takes 5 microseconds to execute, for example, and T_1 is 50 microseconds long, then ten "no-ops" would do the job. This technique is obviously not a realistic one for long timing intervals because it is extremely wasteful of memory and fully occupies the processor with a non-productive task.

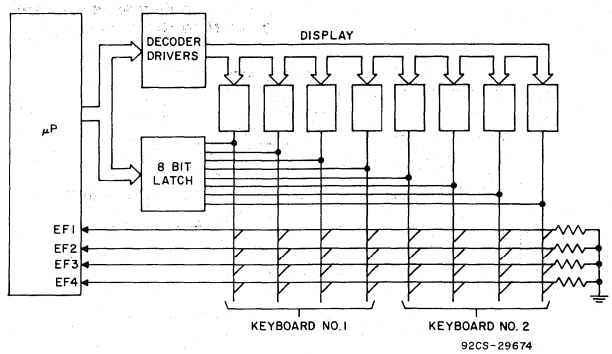

Fig. 20 - An expanded system with 8-digit display and two 16-key keyboards.

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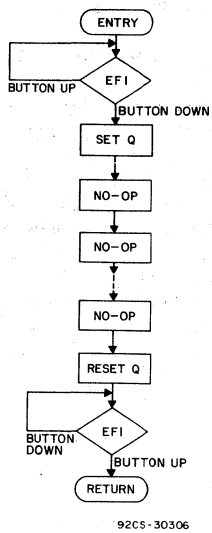


Fig. 22 - Primitive programming technique for pulse generation.

A better technique is shown in Fig. 23(a). Here a counter is preset with a given value and continually decremented until it reaches zero. In the CDP1802 one of the 16-bit general-purpose registers can be used for this function. Fig. 23(b) shows the specific instruction sequence. This technique saves a lot of memory bytes but still ties up the processor. For maximum processor efficiency it would be best to load an external counter that would count at some preset rate and generate an interrupt to the processor when it reaches zero. Meanwhile, the processor could be doing some useful work. Such a system is shown in Fig. 24, but it does not minimize system hardware.

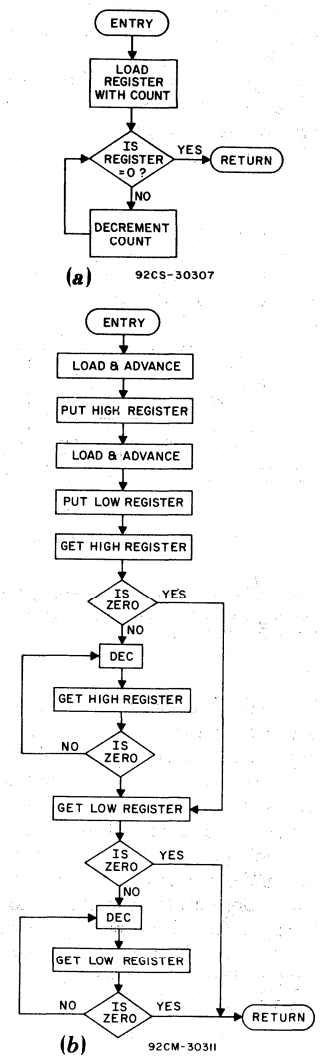


Fig. 23 - (a) Basic flowchart of improved technique for pulse generation. (b) Specific instruction sequence for improved pulse-generation technique.

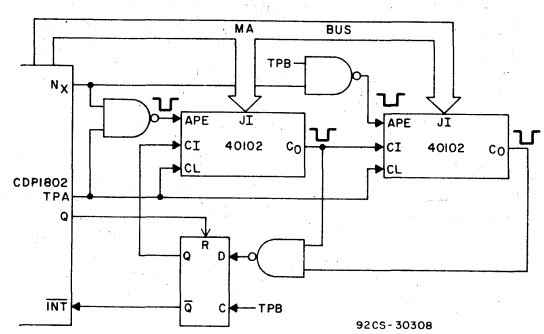


Fig. 24 - System for pulse generation using an external counter.

An interval timer can readily be made for the CDP1802 with no external parts by making use of an internal register that can be automatically incremented. General-purpose register R0 is used as a pointer for DMA operations in the CDP1802 and, as such, is automatically incremented on each DMA (in or out) cycle. By connecting the State Code 1 (SC1) line output back to the DMA Out request line ($\overline{DMAO}$), the CDP1802 performs one DMA cycle for each Fetch and Execute cycle, as shown in Fig. 25, thereby providing a built-in timer and instruction counter. With a clock frequency of 1.57 MHz, the most significant bit of R0 will change each 1/2 second, providing a real-time clock. CPU operation is, of course, slowed by 1/3 with this scheme, but with an upper clock frequency of 6.4 MHz the system can be made fast enough for many applications.

With the circuitry of Fig. 26, a general-purpose interval timer can be realized. This circuit will cause an interrupt when the most significant bit of register R0 goes to a "one". Thus by preloading R0 with a desired count, a timing interval with a range of 2^{15} and a resolution of up to 3.75 microseconds (with a clock frequency of 6.4 MHz) can be obtained with a minimum of external hardware and yet leave the processor free to do useful work.

ACKNOWLEDGMENT

The authors wish to acknowledge the contributions of Messrs. K. Karstad and F. Thorley for developing some of the techniques described.

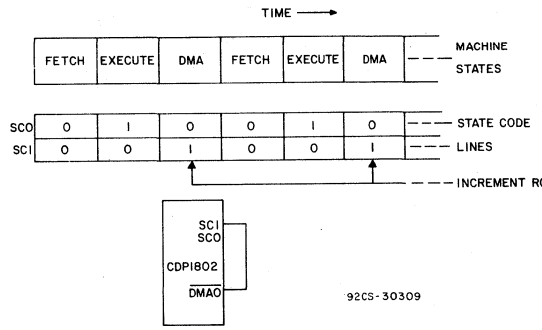


Fig. 25 - Use of DMA-Out line to implement an internal timer.

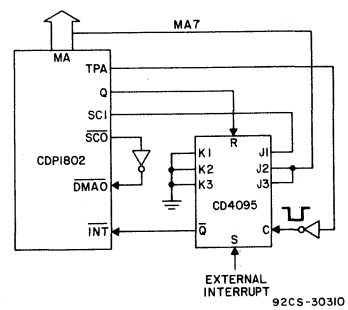
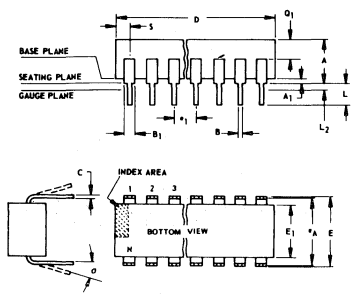


Fig. 26 - Use of interrupt line to implement a general-purpose timer.

Dimensional Outlines

Dual-In-Line Plastic Packages

E SUFFIX



16-Lead
(JEDEC MO-001-AC)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R4

18-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.845	0.885		21.47	22.47
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2,3	7.62 TP	
L	0.125	0.150		3.18	3.81
α	0°	15°	4	0°	15°
N	18		5	18	
N_1	0		6	0	
S	0.015	0.060		0.39	1.52

92CS-30630

22-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.015	0.020		0.381	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D		1.120			28.44
E	0.390	0.420		9.91	10.66
E_1	0.345	0.355		8.77	9.01
e_1	0.100 TP		2	2.54 TP	
e_A	0.400 TP		2, 3	10.16 TP	
L	0.125	0.150		3.18	3.81
L_2	0	0.030		0	0.762
α	2°	15°	4	2°	15°
N	22		5	22	
N_1	0		6	0	
Q_1	0.055	0.085		1.40	2.15
S	0.015	0.060		0.381	1.27

92CS-30830

24-Lead
(JEDEC MO-015-AA)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

92CS26938R3

28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.400	1.490		35.56	37.85
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	28		5	28	
N_1	0		6	0	
Q_1	0.045	0.080		1.14	2.03
S	0.040	0.100		1.02	2.54

92CS-31862

40-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070		0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	2.000	2.090		50.80	53.09
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	40		5	40	
N_1	0		6	0	
Q_1	0.065	0.095		1.66	2.41
S	0.040	0.100		1.02	2.54

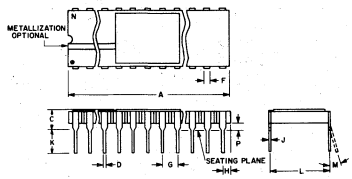
92CS-30959

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dual-In-Line Side-Brazed Ceramic Packages

D SUFFIX



16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	–	0.830		–	21.08
C	–	0.200		–	5.08
D	0.015	0.021		0.381	0.533
F	0.045	0.070	1	1.143	1.778
G	0.100 BSC		1	2.54 BSC	
H	0.015	0.090		0.381	2.286
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.020	–		0.508	–
N	16			16	

92CS-31130

18-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.890	0.915		22.606	23.241
C	–	0.200		–	5.080
D	0.015	0.021		0.381	0.533
F	0.054 REF.		1	1.371 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.035	0.065		0.889	1.651
J	0.008	0.012	3	0.203	0.304
K	0.125	0.150		3.175	3.810
L	0.290	0.310	2	7.366	7.874
M	0°	15°		0°	15°
P	0.025	0.045		0.635	1.143
N	18			18	

92CS-27231R1

22-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.065	1.100		27.05	27.94
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.56
F	0.040 REF.		1	1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.380	0.420	2	9.65	10.67
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	22			22	

92CS-25186R2

24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.180	1.220		29.98	30.98
C	0.085	0.145		2.16	3.68
D	0.015	0.023		0.39	0.56
F	0.040 REF.			1.02 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	24			24	

92CS-30986

28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.380	1.420		35.06	36.06
C	0.085	0.145		2.16	3.68
D	0.017	0.023		0.43	0.56
F	0.050 REF.		1	1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	28			28	

92CM-26419R1

40-Lead

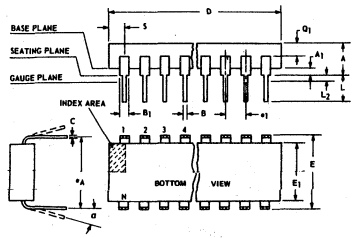
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	1.980	2.020		50.30	51.30
C	0.095	0.155		2.43	3.93
D	0.017	0.023		0.43	0.56
F	0.050 REF.			1.27 REF.	
G	0.100 BSC		1	2.54 BSC	
H	0.030	0.070		0.76	1.78
J	0.008	0.012	3	0.20	0.30
K	0.125	0.175		3.18	4.45
L	0.580	0.620	2	14.74	15.74
M	–	7°		–	7°
P	0.025	0.050		0.64	1.27
N	40			40	

92CM-27029R2

NOTES:
1. Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.
2. Center to center of leads when formed parallel.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

Dual-In-Line Ceramic Package

D SUFFIX



NOTES:
Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
3. e_1 and e_A apply in zone L_2 when unit is installed.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R5

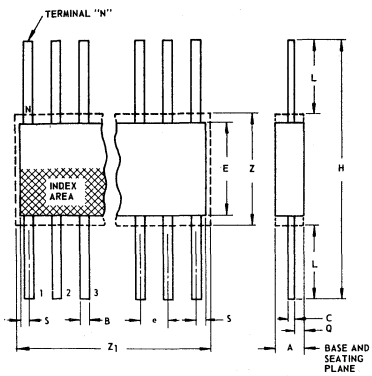
24-Lead (JEDEC MO-015-AG)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.200		2.29	5.08
A_1	0.020	0.070		0.51	1.78
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		2	2.54 TP	
e_A	0.600 TP		2,3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030		0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948R4

Ceramic Flat Pack

K SUFFIX*



92CS-19949R2

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

NOTES:
1. Refer to JEDEC Publication No. 95 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

*This package is used for CD4036AK and CD4039AK types only.

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